TEXAS INSTRUMENTS

TTL

Advanced Low-Power Schottky, Advanced Schottky

Data Book

Volume 2

1993

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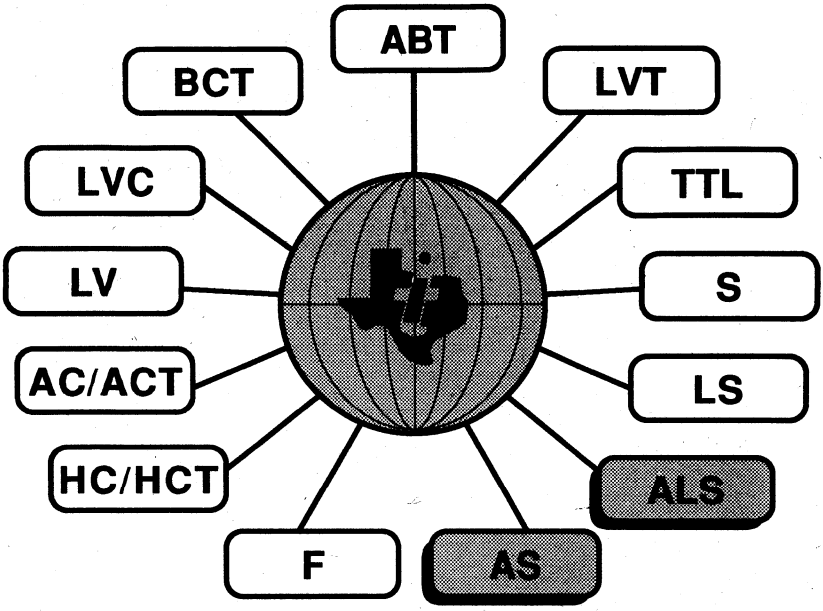
Information contained herein supersedes data published in the TTL Data Book Volume 2, 1991.

Digital Logic Spectrum



The TTL Data Book

Volume 2

INTRODUCTION

The ALS/AS Logic Data Book presents pertinent technical information on Texas Instruments advanced families of TTL integrated circuits, Advanced Low-Power Schottky† (ALS), and Advanced Schottky† (AS). TI's ALS or AS functions provide the system design engineer with management tools to optimize system performace. Aggressive design goals can be achieved by utilizing ALS in noncritical paths and high-performance AS in speed critical paths.

The use of pin-for-pin compatible devices with the most popular LSTTL and STTL functions, existing TTL-based systems may be easily upgraded to ALS/AS to reduce system power requirements, enhance system performance, and improve overall system reliability. New system designs can capitalize on both the improved efficiency of the pin-compatible devices and the higher densities of the MSI/LSI series of devices unique to the ALS/AS family.

ALS and AS devices utilize an advanced wafer fabrication process that includes walled emitters, ion-implanted transistors, oxide isolations, and composed masks. This process is coupled with circuit design techniques to implement the following:

- improve input threshold and noise margins
- improve line driving and receiving
- maintain or increase drive capability
- tolerate ± 10% supply voltage swings
- take advantage of new packaging
  - 24-pin 300-mil DIP
  - plastic "Small Outline"
- specify ac parameters over the full operating termperature range

This data book provides a functional index of all bipolar digital. Package dimensions given in the Mechanical Data section of this book are in metric measurement, which should simplify board layout for designers involved in new designs. The General Information section includes an explanation of the function tables, parameter measurement information, thermal information, D flip-flop and latch signal conventions, and typical characteristics related to the products listed in this volume.

Complete technical data for any Texas Instruments semiconductor/component product is available from your nearest TI field sales office or local authorized TI distributor.

We sincerely believe that you will find the new ALS/AS Logic Data Book a meaningfull addition to your technical library.

- All ALS and AS Devices are included in TTL-Data Book Volume 2 (this book)
- All STD TTL, LS and Schottky Devices are included in TTL-Data Book Volume 1

† Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

PART I — OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

f_{max} **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} **Supply current**
The current into* the V_{CC} supply terminal of an integrated circuit.

I_{CCH} **Supply current, outputs high**
The current into* the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the high level.

I_{CCL} **Supply current, outputs low**
The current into* the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the low level.

I_{IH} **High-level input current**
The current into* an input when a high-level voltage is applied to that input.

I_{IL} **Low-level input current**
The current into* an input when a low-level voltage is applied to that input.

I_{OH} **High-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} **Low-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

I_{OS} **Short-circuit output current**
The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{OZH} **Off-state (high-impedance-state) output current (of a three-state output) with high-level voltage applied**
The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a high-level voltage applied to the output.
NOTE: This parameter is measured with other input conditions established that would cause the output to be at a low level if it were enabled.

*Current out of a terminal is given as a negative value.

I_{OZL} **Off-state (high-impedance-state) output current (of a three-state output) with low-level voltage applied**
The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a low-level voltage applied to the output.
NOTE: This parameter is measured with other input conditions established that would cause the output to be at a high level if it were enabled.

t_a **Access time**
The time interval between the application of a specific input pulse and the availability of valid signals at an output.

t_{dis} **Disable time (of a three-state output)**
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state. (t_{dis} = t_{PHZ} or t_{PLZ}).

t_{en} **Enable time (of a three-state output)**
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low). (t_{en} = t_{PZH} or t_{PZL}).

t_f **Fall time**
The time interval between two reference points (90% and 10% unless otherwise specified) on a waveform that is changing from the defined high level to the defined low level.

t_h **Hold time**
The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.
NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

t_{pd} **Propagation delay time**
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. (t_{pd} = t_{PHL} or t_{PLH}).

t_{PHL} **Propagation delay time, high-to-low-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PHZ} **Disable time (of a three-state output) from high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

*Current out of a terminal is given as a negative value.

t_{PLH} **Propagation delay time, low-to-high-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PLZ} **Disable time (of a three-state output) from low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PZH} **Enable time (of a three-state output) to high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL} **Enable time (of a three-state output) to low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

t_r **Rise time**
The time interval between two reference points (10% and 90% unless otherwise specified) on a waveform that is changing from the defined low level to the defined high level.

t_{sr} **Sense recovery time**
The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.

t_{su} **Setup time**
The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_w **Pulse duration (width)**
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

V_{IH} **High-level input voltage**
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IK} **Input clamp voltage**
An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

V_{IL} **Low-level input voltage**
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} **High-level output voltage**
The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**
The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

PART II — STRESS

Stress beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state-output
a . . h	=	the level of steady-state inputs at inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎎	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎎, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

EXPLANATION OF FUNCTION TABLES

Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74AS194.

FUNCTION TABLE

INPUTS											OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL								
	S1	S0		LEFT	RIGHT	A	B	C	D		Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X		L	L	L	L
H	X	X	L	X	X	X	X	X	X		Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d		a	b	c	d
H	L	H	↑	X	H	X	X	X	X		H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X		L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X		Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X		Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X		Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

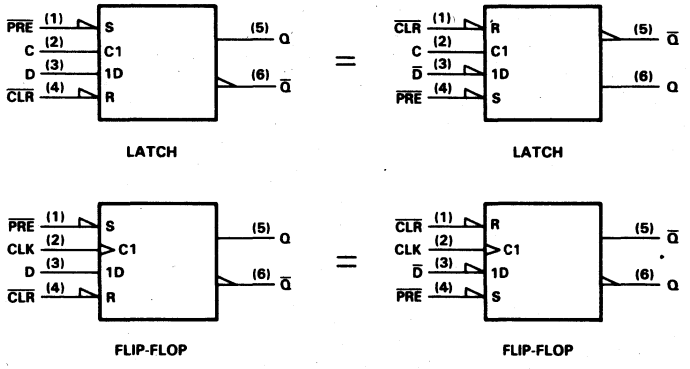
The last line shows that as long as both mode inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

D flip-flop and latch signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset (PRE). An input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active-low.

The devices on several data sheets are second-source designs, and the pin-name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits $\overline{D}$ and Q.

In some applications, it may be advantageous to redesignate the data input from D to $\overline{D}$ or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown in parentheses.



The figures show that when Q and $\overline{Q}$ exchange names, the Preset and Clear pins also exchange names. The polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain, as these inputs are still active-low, but the presence or absence of the polarity indicator changes at D (or $\overline{D}$), Q, and $\overline{Q}$. Pin 5 (Q or $\overline{Q}$) is still in phase with the data input (D or $\overline{D}$); their active levels change together.

In digital system design, consideration must be given to thermal management of components. The small size of the "small outline" package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures for the Advanced Low-Power Schottky (ALS) and Advanced Schottky (AS) families. In general, junction temperature for any device can be calculated using Equation 1.

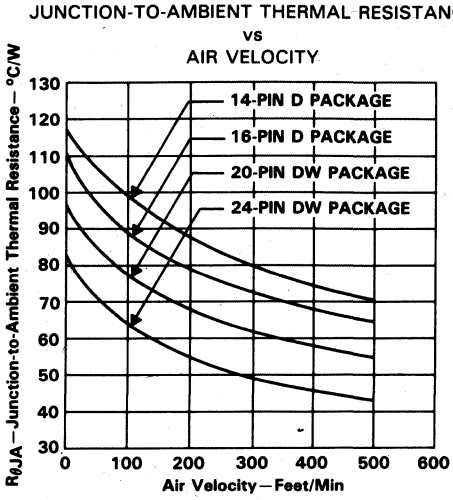


FIGURE 1

$$T_J = R_{\theta JA}(V_{CC} \cdot I_{CC} + N \cdot I_{OL} \cdot V_{OL}) + T_A \quad (1)$$

where

T_J = virtual junction temperature
$R_{\theta JA}$ = thermal resistance, junction to ambient air
V_{CC} = supply voltage (5 V for typical, 5.5 V for maximum)
I_{CC} = supply current
N = the number of outputs
I_{OL} = the low-level output current
V_{OL} = the low-level output voltage
T_A = the ambient air temperature

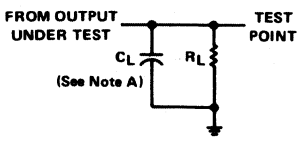
Typical junction temperature can be calculated using Equation 1 directly with typical values of I_{CC} taken from the data sheets and V_{CC} = 5 volts. To calculate maximum junction temperature, it is necessary to take into account the spread of I_{CC} values for a population. Due to different specification practices that have been followed, it is sometimes useful to use slightly different calculation procedures for the ALS and AS families.

Maximum junction temperature for all 54ALS, 54AS, and some 74ALS parts can be calculated using Equation 1 with I_{CC} being the maximum value specified on the data sheet and V_{CC} = 5.5 volts. In fact, I_{CC} for Series 54 devices at the temperature extremes of −55°C to 125°C will be higher than for a Series 74 device at the temperature extremes of 0°C to 70°C. This is reflected in the limits specified for some 74ALS devices, which are less than those specified for 54ALS devices. The AS family and most ALS family data sheets give a single maximum value for I_{CC}. If that value is used to calculate maximum junction temperature for series 74 devices, an unrealistically high value will result. Instead, Equation 2 can be used. This uses the factor 1.31 to scale the typical value of I_{CC} up to a practical maximum value for process variations and thermal effects.

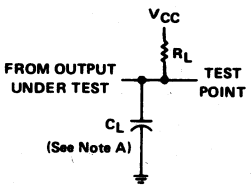
Thus, for 74AS and 74ALS devices if a lowered maximum I_{CC} has not been specified:

$$T_{Jmax} = R_{\theta JA}(5.5 \cdot 1.31 \cdot I_{CCtyp} + N \cdot I_{OL} \cdot V_{OL}) + T_A \quad (2)$$

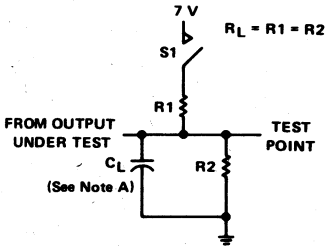
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS

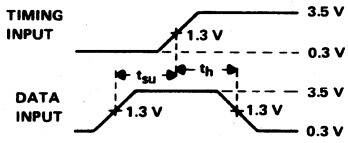


LOAD CIRCUIT FOR
OPEN-COLLECTOR OUTPUTS

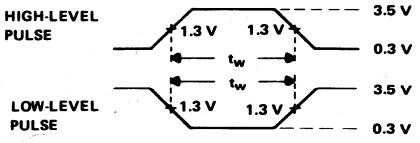


LOAD CIRCUIT FOR
THREE-STATE OUTPUTS

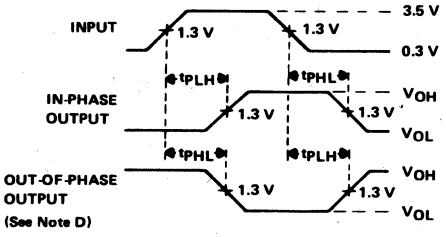
NOTE A: C_L includes probe and jig capacitance.



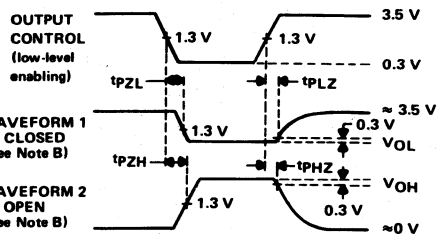
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. When measuring propagation delay items of 3-state outputs, switch S1 is open.
E. The outputs are measured one at a time with one input transition per measurement.

- All ALS and AS Devices are included in TTL-Data Book Volume 2 (this book).
- All STD TTL, LS and Schottky Devices are included in TTL-Data Book Volume 1.

GATES AND INVERTERS

NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Hex 2-Input Gates	'804		●	●		
Hex Inverters	'04	●	●	●	●	●
	'1004		●	●		
Quadruple 2-Input Gates	'00	●	●	●	●	●
	'1000			●		
Triple 3-Input Gates	'10		●	●	●	●
Dual 4-Input Gates	'20		●	●	●	●
8-Input Gates	'30	●	●	●	●	●
13-Input Gates	'133		●			●

NAND GATES AND INVERTERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Hex Inverters	'05	●	●		●	●
	'1005		●			
Quadruple 2-Input Gates	'01		●		●	
	'03		●		●	●

AND GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Quadruple 2-Input Gates	'09	●	●		●	●

AND GATES

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Hex 2-Input Gates	'808			●		
Quadruple 2-Input Gates	'08	●	●	●	●	●
	'1008			●		
Triple 3-Input Gates	'11		●	●	●	●
Dual 4-Input Gates	'21		●	●	●	

OR GATES

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Hex 2-Input Gates	'832		●	●		
Quadruple 2-Input Gates	'32	●	●	●	●	●
	'1032			●		

NOR GATES

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Hex 2-Input Gates	'805		●	●		
Quadruple 2-Input Gates	'02	●	●	●	●	●
Triple 3-Input Gates	'27		●	●	●	
Dual 4-Input Gates with Strobe	'25	●				
Dual 5-Input Gates	'260					●

EXCLUSIVE OR/NOR GATES

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Quad 2-Input Exclusive-OR Gates with Totem-Pole Outputs	'86	●	●	●	●	●
Quad 2-Input Exclusive-OR Gates with Open-Collector Outputs	'136			●	●	
Quad 2-Input Exclusive-NOR Gates	'810		●	●		
Quad 2-Input Exclusive-NOR Gates with Open-Collector Outputs	'811			●		
Quad Exclusive OR/NOR Gates	'135					●

SCHMITT-TRIGGER NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Hex Inverters	'14	●			●	
	'19				●	
Quadruple 2-Input Positive-NAND	'24				●	
	'132	●			●	●

DELAY ELEMENTS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Inverting and Noninverting Elements, 2-Input NAND Buffers	'31				●	

GATES, BUFFERS, DRIVERS, AND TRANSCEIVERS

AND-OR-INVERT GATES

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
4-Wide 4-2-3-2-Input	'64					●
4-Wide 2-3-3-2-Input	'54				●	
Dual 2-Wide 2-Input	'51				●	●

BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Hex	'07	●			●	
	'17	●				
	'35		●			
	'1035		●			
Hex Inverter	'06	●			●	
	'16	●				
	'1005		●			
Quad 2-Input Positive-NAND	'26				●	
	'38	●	●		●	●
Quad 2-Input Positive-NOR	'33		●		●	

BUFFERS, DRIVERS, AND BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Noninverting Octal Buffers/Drivers	'757			●		
	'760		●	●		
Inverting Octal Buffers/Drivers	'756		●	●		
Inverting and Noninverting Octal Buffers/Drivers	'762		●			
Inverting Quad Transceivers	'758		●			

GATES, BUFFERS, DRIVERS, AND TRANSCEIVERS

GATES, BUFFERS, DRIVERS, AND BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Noninverting Octal Buffers/Drivers	'241		●	●	●	●
	'244		●	●	●	●
	'465		●		●	
	'541		●		●	
	'1244*		●			
Inverting Octal Buffers/Drivers	'240		●	●	●	●
	'466				●	
	'540		●		●	
Octal Transceivers	'245		●	●	●	
	'1245		●			
Noninverting Hex Buffers/Drivers	'365				●	
	'367	●			●	
Inverting Hex Buffers/Drivers	'366				●	
	'368	●			●	
Quad Buffers/Drivers with Independent Output Controls	'125				●	
	'126				●	
Noninverting Quad Transceivers	'243			●	●	

* Denotes very low power.

GATES, BUFFERS, DRIVERS, AND TRANSCEIVERS

BUFFERS,DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Hex 2-Input Positive-NAND	'804		●	●		
Hex 2-Input Positive-NOR	'805		●	●		
Hex 2-Input Positive-AND	'808			●		
Hex 2-Input Positive-OR	'832		●	●		
Hex Inverter	'1004		●	●		
Hex Buffer	'1034		●	●		
Quad 2-Input Positive NAND	'37	●	●		●	●
	'1000			●		
Quad 2-Input Positive NOR	'128	●				
Quad 2-Input Positive AND	'1008			●		
Quad 2-Input Positive OR	'1032			●		
Dual 4-Input Positive-NAND	'140					●

OCTAL BI-/TRI-DIRECTIONAL BUS TRANSCEIVERS

DESCRIPTION		TYPE OF OUTPUT	TECHNOLOGY				
			TYPE	ALS	AS	LS	S
12 mA, 24 mA, 48 mA, 64 mA Sink, True Outputs	Low Power	3-State	'245	●	●	●	
		OC	'621	●		●	
		3-State	'623	●	●	●	
		OC,3-State	'639	●	●	●	
		3-State	'652	●	●	●	
		OC,3-State	'654	●			
12 mA, 24 mA, 48 mA, 64 mA Sink, Inverting Outputs	Low Power	3-State	'620	●			
		OC,3-State	'638	●			
		3-State	'651	●	●		
		OC,3-State	'653	●			
12 mA, 24 mA, 48 mA, 64 mA Sink, True Outputs	Low Power	OC	'641	●	●	●	
		3-State	'645	●	●	●	
	Very Low Power	3-State	'1645	●			
12 mA, 24 mA, 48 mA, 64 mA Sink, Inverting Outputs	Low Power	3-State	'640	●	●	●	
		OC	'642			●	
	Very Low Power	3-State	'1640	●			
Registered with Multiplexed 12 mA, 24 mA, 48 mA, 64 mA, True Outputs		3-State	'646	●	●	●	
		OC	'647			●	
Registered with Multiplexed 12 mA, 24 mA, 48 mA, 64 mA, Inverting Outputs		3-State	'648	●	●	●	

BI-/TRI-DIRECTIONAL BUS TRANSCEIVERS AND DRIVERS

DESCRIPTION	TYPE OF OUTPUT	TECHNOLOGY				
		TYPE	ALS	AS	LS	S
Controls	3-State	'449			●	
Quad Tridirection	3-State	'442			●	

OCTAL BUS TRANSCEIVERS / MOS DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
True Outputs, 3-State	'2645			●		
Input Resistors, Inverting Outputs	'746		●			
Output Resistors, Noninverting Outputs	'2541		●			

FLIP-FLOPS

DUAL AND SINGLE FLIP-FLOPS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Dual J-K Edge Triggered	'73				●	
	'76	●			●	
	'107	●			●	
	'109		●	●	●	
	'112		●		●	●
Dual Pulse Triggered	'73	●				
	'76	●				
	'107	●				
Dual D Type	'74	●	●	●	●	●

QUAD AND HEX FLIP-FLOPS

DESCRIPTION	NO. OF FFs	OUTPUTS	TYPE	TECHNOLOGY				
				STD TTL	ALS	AS	LS	S
D-Type	6	Q	'174		●	●	●	●
			'378				●	
	4	Q, $\overline{Q}$	'175	●	●	●	●	●
			'379				●	
J-K	4	Q	'276	●				
			'376	●				

OCTAL, 9-BIT, AND 10-BIT D-TYPE FLIP-FLOPS

DESCRIPTION	NO. OF BITS	OUTPUTS	TYPE	TECHNOLOGY				
				STD TTL	ALS	AS	LS	S
True Data	Octal	3-State	'374		●	●	●	●
		3-State	'574		●	●		
True Data with Clear	Octal	2-State	'273	●	●		●	
		3-State	'575		●	●		
		3-State	'874		●	●		
		3-State	'878		●			
True with Enable	Octal	2-State	'377				●	
Inverting	Octal	3-State	'534		●	●		
		3-State	'564		●			
		3-State	'576		●	●		
Inverting with Clear	Octal	3-State	'577		●			
		3-State	'879		●			
Inverting with Preset	Octal	3-State	'876		●			
True	Octal	3-State	'825			●		
True	9-Bit	3-State	'823			●		
Inverting	9-Bit	3-State	'824			●		
True	10-Bit	3-State	'821			●		
Inverting	10-Bit	3-State	'822			●		

LATCHES AND MULTIVIBRATORS

QUAD LATCHES

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY				
			STD TTL	ALS	AS	LS	S
DUAL 2-Bit Transparent	2-State	'75				●	
	2-State	'77	●				
	2-State	'375				●	
S-R	2-State	'279	●			●	

MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Single	'121	●				
Dual	'221	●			●	

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
SINGLE	'122				●	
DUAL	'123	●			●	
	'423				●	

D-TYPE 8-BIT, 9-BIT, AND 10-BIT READ BACK LATCHES

DESCRIPTION	NO. OF BITS	TYPE	TECHNOLOGY				
			STD TTL	ALS	AS	LS	S
Edge Triggered Inverting and Noninverting	Octal	'996		● ●			
Transparent True	Octal	'990		●			
	9-Bit	'992		●			
	10-Bit	'994		●			
Transparent with Clear True Outputs	Octal	'666		● ●			
Transparent with Clear Inverting Outputs	Octal	'667		● ●			

8-BIT, 9-BIT, AND 10-BIT LATCHES

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY				
				STD TTL	ALS	AS	LS	S
Transparent	Octal	3-State	'373		●	●	●	●
		3-State	'573		●	●		
Dual 4-Bit Transparent	Octal							
		3-State	'873		●	●		
Inverting Transparent	Octal	3-State	'533		●	●		
		3-State	'563		●			
		3-State	'580		●	●		
Addressable	Octal	2-State	'259	●	●		●	
True	10-Bit	3-State	'841		●	●		
True, AMD comp.	10-Bit	3-State	'29841		●			

REGISTERS

SHIFT REGISTERS

DESCRIPTION	NO. OF BITS	MODES				TYPE	TECHNOLOGY				
		S-R	S-L	LOAD	HOLD		STD TTL	ALS	AS	LS	S
Sign Protected		X		X	X	'322				●	
Parallel In, Parallel Out Bidirectional	8	X	X	X	X	'299		●	●	●	●
		X	X	X	X	'323		●	●	●	
	4	X	X	X	X	'194			●	●	●
Parallel In Parallel Out	5	X		X		'96				●	
	4	X		X		'195			●	●	●
		X		X		'395				●	
Serial In Parallel Out	16	X		X	X	'673				●	
	8	X				'164	●	●		●	
Parallel In, Serial Out	16	X		X	X	'674				●	
	8	X		X	X	'165		●		●	
		X		X	X	'166		●		●	

SHIFT REGISTERS WITH LATCHES

DESCRIPTION	NO. OF BITS	OUTPUTS	TYPE	TECHNOLOGY				
				STD TTL	ALS	AS	LS	S
Serial In, Parallel Out, with Output Latches	8	2-State	'673				●	
		Buffered	'594				●	
		3-State	'595				●	
		OC	'596				●	
		OC	'599				●	
Parallel In, Serial Out with Input Latches	8	2-State	'597				●	
Parallel I/O Ports with Input Latches, Multiplexed Serial Inputs	8	3-State	'598				●	

REGISTER FILES

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY				
			STD TTL	ALS	AS	LS	S
4 Words x 4 Bits	3-State	'670				●	
Dual 16 Words x 4 Bits	3-State	'870		●	●		

OTHER REGISTERS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Quadruple Multiplexers with Storage	'298			●	●	
	'399				●	
8-Bit Universal Shift Registers	'299		●	●	●	●
Quadruple Bus Buffer Registers	'173				●	
Octal Storage Register	'396				●	

COUNTERS

SYNCHRONOUS COUNTERS – POSITIVE-EDGE TRIGGERED

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY				
			STD TTL	ALS	AS	LS	S
Decade	Sync	'160		●			
Decade Up/Down	Sync	'568		●			●
4-Bit Binary		'161	●	●	●	●	
		'163		●	●	●	●
		'561		●			
		'669				●	
		'691				●	
4-Bit Binary Up/Down	Sync	'169		●	●	●	●
	Async	'191		●		●	
	Async	'193	●	●		●	
	Sync	'569		●			
	Sync	'697				●	
	Sync	'699				●	
6-Bit Binary Rate Multiplier $\frac{1}{N2}$ 8-Bit Up/Down		'97	●				
	Async CLR	'867		●	●		
	Sync CLR	'869		●	●		

ASYNCHRONOUS COUNTERS (RIPPLE CLOCK) – NEGATIVE EDGE TRIGGERED

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY				
			STD TTL	ALS	AS	LS	S
Decade	Set-to-9	'90	●			●	
	Yes	'196					●
4-Bit Binary	None	'93				●	
	None	'293				●	
Divide by 12	None	'92				●	
Dual Decode	None	'390				●	
Dual 4-Bit Binary	None	'393	●			●	

8-BIT BINARY COUNTERS WITH REGISTERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY				
			STD TTL	ALS	AS	LS	S
Parallel Register Outputs	3-State	'590				●	
Parallel Register Inputs	2-State	'592				●	
Parallel I/O	3-State	'593				●	

FREQUENCY DIVIDERS, RATE MULTIPLIERS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
50-to-1 Frequency Divider	'56				●	
60-to-1 Frequency Divider	'57				●	
6-Bit Binary Rate Multiplier	'97	●				
Decade Rate Multiplier	'167	●				
Programmable Frequency Dividers Digital Timers	'292				●	
	'294				●	

DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS AND SHIFTERS

DATA SELECTORS MULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY				
			STD TTL	ALS	AS	LS	S
16-to-1	2-State	'150	●				
	3-State	'250			●		
8-to-1	2-State	'151	●	●	●	●	●
	3-State	'251		●	●	●	●
Dual 4-to-1	2-State	'153		●	●	●	●
	3-State	'253		●	●	●	
	2-State	'352				●	
	3-State	'353			●		
Quad 2-to-1 with Storage	2-State	'298			●	●	
	2-State	'399				●	
Quad 2-to-1	2-State	'157	●	●	●	●	●
	2-State	'158		●	●	●	●
	3-State	'257		●	●	●	●
	3-State	'258		●	●	●	●
6-to-1 Universal Multiplexer	3-State	'857		●			

DECODERS/DEMULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY				
			STD TTL	ALS	AS	LS	S
4-to-16	3-State	'154	●				
	OC	'159	●				
4-to-10 BCD-to-Decimal	2-State	'42				●	
3-to-8 with Address Latches	2-State	'137		●	●		
3-to-8	2-State	'138		●	●	●	●
Dual 2-to-4	2-State	'139		●	●	●	●
	2-State	'155	●			●	
	OC	'156	●	●		●	

PRIORITY ENCODERS/REGISTERS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Casadable Octal	'148	●			●	
Casadable Octal with 3-State Outputs	'348				●	

DISPLAY DECODERS/DRIVERS AND VOLTAGE-CONTROLLED OSCILLATORS

OPEN-COLLECTOR DISPLAY DECODERS/DRIVERS

DESCRIPTION	OFF-STATE OUTPUT VOLTAGE	TYPE	TECHNOLOGY				
			STD TTL	ALS	AS	LS	S
BCD to Decimal	30 V	'45	●				
	15 V	'145	●			●	
BCD-to-Seven-Segment	15 V	'47	●			●	
	15 V	'247				●	

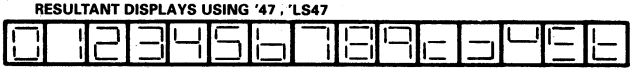
VOLTAGE-CONTROLLED OSCILLATORS

DESCRIPTION						TYPE	TECHNOLOGY	
No. VCOs	COMP'L Z_{OUT}	ENABLE	RANGE INPUT	R_{ext}	f_{max} MHz		LS	S
Single	Yes	Yes	Yes	No	20	'624	●	
Single	Yes	Yes	Yes	Yes	20	'628	●	
Dual	No	Yes	Yes	No	60	'124		●
Dual	Yes	Yes	No	No	20	'626	●	
Dual	No	Yes	Yes	No	20	'629	●	

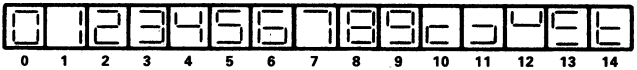
CLOCK GENERATOR CIRCUITS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Crystal Controlled Oscillators	'321				●	

RESULTANT DISPLAYS USING '47, 'LS47



RESULTANT DISPLAYS USING 'LS247



COMPARATORS AND ERROR DETECTION CIRCUITS

4-BIT COMPARATORS

DESCRIPTION					TYPE	TECHNOLOGY		
P=Q	P>Q	P<Q	OUTPUT	OUTPUT ENABLE		AS	LS	S
Yes	Yes	No	2-State	No	'85		●	●

8-BIT COMPARATORS

DESCRIPTION							TYPE	TECHNOLOGY		
INPUTS	P=Q	$\overline{P=Q}$	P>Q	P<Q	OUTPUT	OUTPUT ENABLE		ALS	AS	LS
20 kΩ	Yes	No	No	No	OC	Yes	'518	●		
Pull	No	Yes	No	No	2-State	Yes	'520	●		
up	Yes	No	Yes	No	2-State	No	'682			●
	Yes	No	No	No	OC	Yes	'519	●		
	No	Yes	No	No	2-State	Yes	'521	●		
Standard	Yes	No	Yes	No	2-State	No	'684			●
	Yes	No	Yes	No	2-State	Yes	'686			●
	No	Yes	No	Yes	2-State	Yes	'688	●		●
Latched P	No	No	Yes	Yes	2-State	Yes	'885		●	

ADDRESS COMPARATORS

DESCRIPTION	OUTPUT ENABLE	LATCHED OUTPUT	TYPE	TECHNOLOGY				
				STD TTL	ALS	AS	LS	S
16-Bit to 4-Bit	Yes	No	'677		●			
12-Bit to 4-Bit	Yes	No	'679		●			

PARITY GENERATORS/CHECKERS, ERROR DETECTION AND CORRECTION CIRCUITS

DESCRIPTION		NO. OF BITS	TYPE	TECHNOLOGY				
				STD TTL	ALS	AS	LS	S
Odd Even Parity		8	'180	●				
Generators		9	'280		●	●	●	●
Checkers		9	'286			●		
Parallel Error Detection and Correction Circuits	3-State	8	'636				●	

ARITHMETIC ELEMENTS

PARALLEL BINARY ADDERS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
4-Bit	'283				●	●

ACCUMULATORS, ARITHMETIC LOGIC UNITS, LOOK-AHEAD CARRY GENERATORS

DESCRIPTION		TYPE	TECHNOLOGY				
			STD TTL	ALS	AS	LS	S
4-Bit Arithmetic Logic Units/ Function Generators		'181			●	●	●
		'381				●	●
		'881			●		
4-Bit Arithmetic Logic Unit with Ripple Carry		'382				●	
Look-Ahead Carry Generators	16 Bit	'182					●

SPECIAL CLOCK FUNCTIONS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Quadruple Complementary-Output Logic Elements	'265	●				
Digital Phase-Locked Loop	'297				●	

BUS TERMINATION ARRAYS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
8-Bit Schottky Diode	'1056					●
12-Bit Schottky Diode	'1050					●
12-Bit Schottky Diode	'1051					●
16-Bit Schottky Diode	'1052					●
16-Bit Schottky Diode	'1053					●

FIRST-IN FIRST-OUT MEMORIES (FIFO's)

ORGANIZATION	TYPE OF OUTPUT	TYPE	TECHNOLOGY				
			STD TTL	ALS	AS	LS	S
16 x 4 Bit	3-State	'222				●	
	3-State	'224				●	
	3-State	'232		●			
	Open Coll.	'228				●	
16 x 5 Bit	3-State	'225					●
	3-State	'233		●			
	3-State	'229		●			
32 x 9 Bit, Bidirectional	3-State	'2238		●			
64 x 4 Bit	3-State	'234		●			
	Totem Pole	'236		●			
64 x 5 Bit, Half Full Flag	3-State	'235		●			
64 x 8 Bit	3-State	'2232		●			
64 x 9 Bit, Half Full Flag	3-State	'2233		●			

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ALS and AS Devices 2

3

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D2661, APRIL 1982 – REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

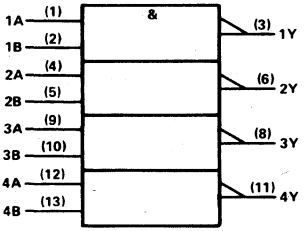
These devices contain four independent 2-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS00A and SN54AS00 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS00A and SN74AS00 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

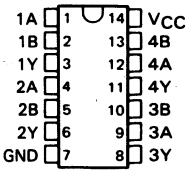
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

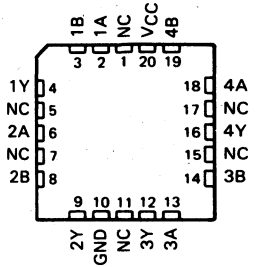


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS00A, SN54AS00 . . . J PACKAGE
SN74ALS00A, SN74AS00 . . . D OR N PACKAGE
(TOP VIEW)

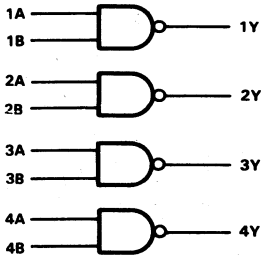


SN54ALS00A, SN54AS00 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS00A . . . . . −55°C to 125°C
SN74ALS00A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS00A			SN74ALS00A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS00A			SN74ALS00A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.5	0.85		0.5	0.85	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.5	3		1.5	3	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS00A	SN54ALS00A		SN74ALS00A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	7	3	16	3	11	ns
t_{PHL}	A or B	Y	5	2	13	2	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS00 . . . . . −55°C to 125°C
SN74AS00 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS00			SN74AS00			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS00			SN74AS00			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		2	3.2		2	3.2	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		10.8	17.4		10.8	17.4	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 50 Ω, T_A = MIN to MAX				UNIT
			SN54AS00		SN74AS00		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	5	1	4.5	ns
t_{PHL}	A or B	Y	1	5	1	4	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982 – REVISED JANUARY 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

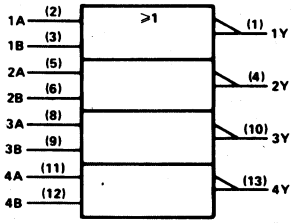
These devices contain four independent 2-input NOR gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A + B}$ in positive logic.

The SN54ALS02A and SN54AS02 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS02A and SN74AS02 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

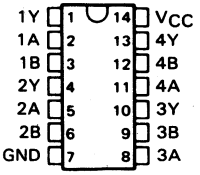
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†

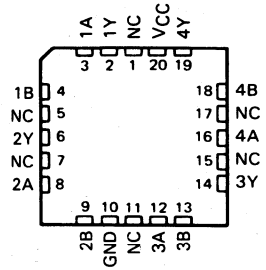


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS02A, SN54AS02 . . . J PACKAGE
SN74ALS02A, SN74AS02 . . . D OR N PACKAGE
(TOP VIEW)

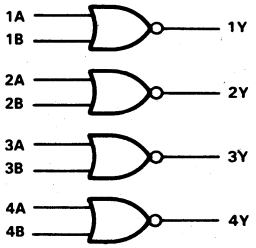


SN54ALS02A, SN54AS02 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS02A . . . . . −55°C to 125°C
SN74ALS02A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operation conditions

		SN54ALS02A			SN74ALS02A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS02A			SN74ALS02A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4,5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	V_I = 0 V		0.86	2.2		0.86	2.2	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.16	4		2.16	4	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS02	SN54ALS02A		SN74ALS02A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	7	1	18	1	12	ns
t_{PHL}	A or B	Y	5	1	11	1	10	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS02 . . . . . −55°C to 125°C
SN74AS02 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS02			SN74AS02			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS02			SN74AS02			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		3.7	5.9		3.7	5.9	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		12.5	20.1		12.5	20.1	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS02		SN74AS02		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	5	1	4.5	ns
t_{PHL}	A or B	Y	1	5	1	4.5	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

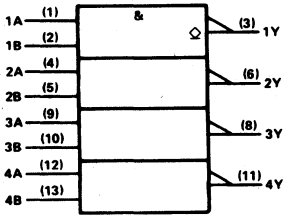
These devices contain four independent 2-input NAND buffers. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS03B is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS03B is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

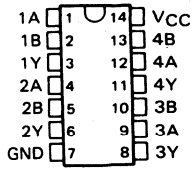
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

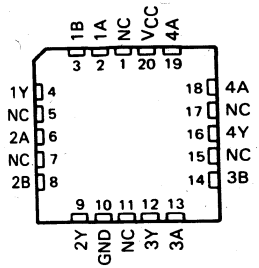


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS03B . . . J PACKAGE
SN74ALS03B . . . D OR N PACKAGE
(TOP VIEW)

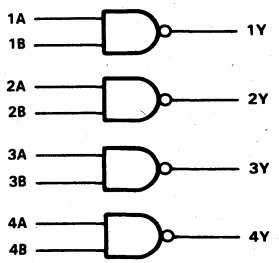


SN54ALS03B . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS03B . . . . . −55°C to 125°C
SN74ALS03B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS03B			SN74ALS03B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS03B			SN74ALS03B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.43	0.85		0.43	0.85	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.62	3		1.62	4	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			'ALS03B	SN54ALS03B		SN74ALS03B		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	35	20	59	20	50	ns
t_{PHL}	A or B	Y	8	3	23	3	13	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982 – REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

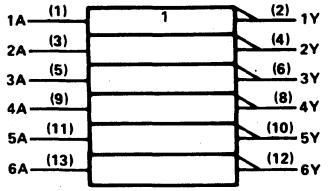
These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$.

The SN54ALS04B and SN54AS04 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS04B and SN74AS04 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each inverter)

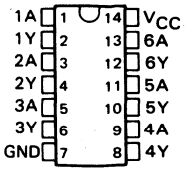
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†

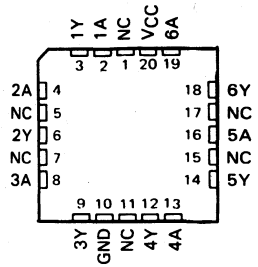


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS04B, SN54AS04 . . . J PACKAGE
SN74ALS04B, SN74AS04 . . . D OR N PACKAGE
(TOP VIEW)

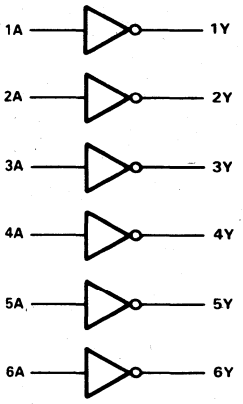


SN54ALS04B, SN54AS04 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS04B . . . . . −55°C to 125°C
SN74ALS04B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS04B			SN74ALS04B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS04B			SN74ALS04B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.65	1.1		0.65	1.1	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.9	4.2		2.9	4.2	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS04B		SN74ALS04B		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	14	3	11	ns
t_{PHL}	A	Y	2	12	2	8	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS04 . . . . . −55°C to 125°C
SN74AS04 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS04			SN74AS04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS04			SN74AS04			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		3	4.8		3	4.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		14	26.3		14	26.3	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS04		SN74AS04		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	6	1	5	ns
t_{PHL}	A	Y	1	4.5	1	4	ns

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

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- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

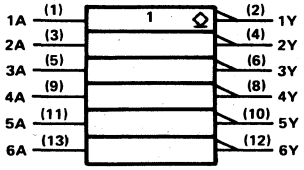
These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS05A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS05A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each inverter)

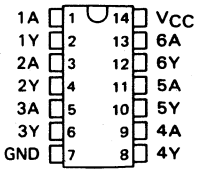
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†

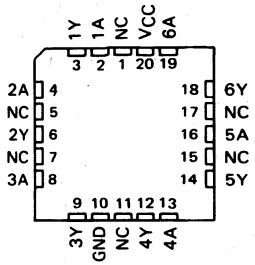


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS05A . . . J PACKAGE
SN74ALS05A . . . D OR N PACKAGE
(TOP VIEW)

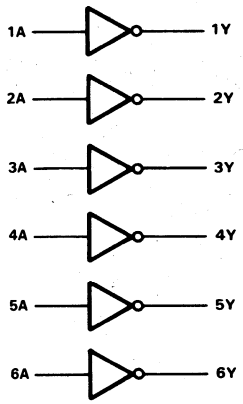


SN54ALS05A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS05A . . . . . −55°C to 125°C
SN74ALS05A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS05A			SN74ALS05A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS05A			SN74ALS05A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.65	1.1		0.65	1.1	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.9	4.2		2.9	4.2	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			'ALS05A	SN54ALS05A		SN74ALS05A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	45	23	84	23	54	ns
t_{PHL}	A	Y	9	4	24	4	14	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982 – REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

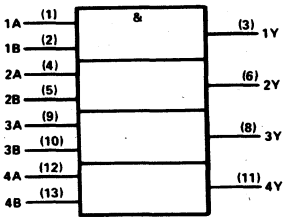
These devices contain four independent 2-input AND gates. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The SN54ALS08 and SN54AS08 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS08 and SN74AS08 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each gate)

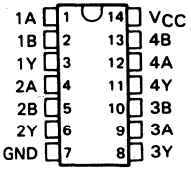
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†

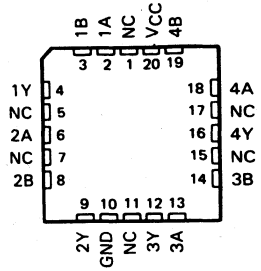


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS08, SN54AS08 . . . J PACKAGE
SN74ALS08, SN74AS08 . . . D OR N PACKAGE
(TOP VIEW)

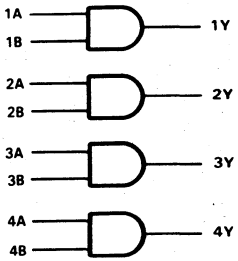


SN54ALS08, SN54AS08 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS08 . . . . . −55°C to 125°C
SN74ALS08 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS08			SN74ALS08			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	mA
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS08			SN74ALS08			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2						V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.3	2.4		1.3	2.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		2.2	4		2.2	4	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS08	SN54ALS08		SN74ALS08		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	8	4	18	4	14	ns
t_{PHL}	A or B	Y	6.5	3	15	3	10	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS08 . . . . . −55°C to 125°C
SN74AS08 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS08			SN74AS08			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	mA
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS08			SN74AS08			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		5.8	9.3		5.8	9.3	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		14.9	24		14.9	24	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions hav been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 50 Ω, T_A = MIN to MAX				UNIT
			SN54AS08		SN74AS08		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	6.5	1	5.5	ns
t_{PHL}	A or B	Y	1	6.5	1	5.5	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

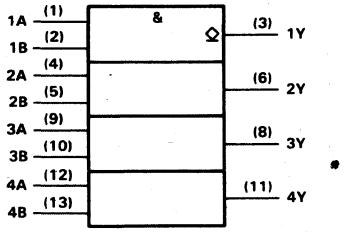
These devices contain four independent 2-input AND gates. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS09 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS09 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

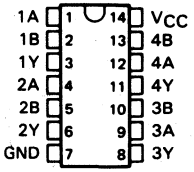
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†

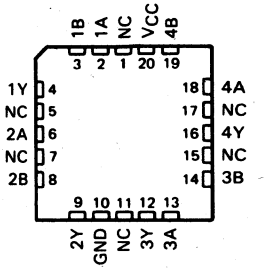


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS09 . . . J PACKAGE
SN74ALS09 . . . D OR N PACKAGE
(TOP VIEW)

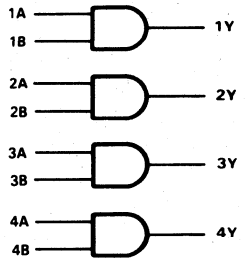


SN54ALS09 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS09 . . . . . −55°C to 125°C
SN74ALS09 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS09			SN74ALS09			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS09			SN74ALS09			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.35	2.4		1.35	2.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		2.2	4		2.2	4	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			SN54ALS09		SN74ALS09		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	20	69	23	54	ns
t_{PHL}	A or B	Y	5	23	5	15	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

MARCH 1984 – REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

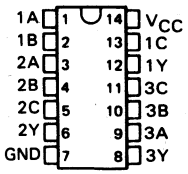
These devices contain three independent 3-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The SN54ALS10A and SN54AS10 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS10A and SN74AS10 are characterized for operation from 0°C to 70°C.

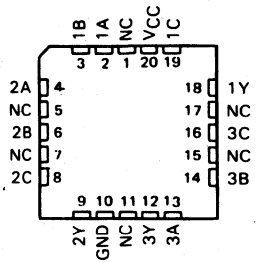
FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

SN54ALS10A, SN54AS10 . . . J PACKAGE
SN74ALS10A, SN74AS10 . . . D OR N PACKAGE
(TOP VIEW)

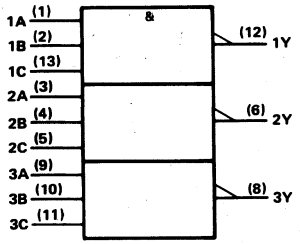


SN54ALS10A, SN54AS10 . . . FK PACKAGE
(TOP VIEW)



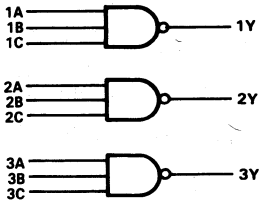
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS10A . . . . . −55 °C to 125 °C
SN74ALS10A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS10A			SN74ALS10A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS10A			SN74ALS10A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.32	0.6		0.32	0.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.2	2.2		1.2	2.2	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS10A		SN74ALS10A		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	2	16	2	11	ns
t_{PHL}	Any	Y	2	12	2	10	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS10 . . . . . −55 °C to 125 °C
SN74AS10 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS10			SN74AS10			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS10			SN74AS10			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		1.5	2.4		1.5	2.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		8.1	13		8.1	13	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS10		SN74AS10		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1	5	1	4.5	ns
t_{PHL}	Any	Y	1	5	1	4.5	ns

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

MARCH 1984 – REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

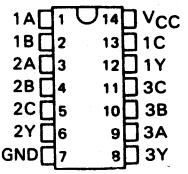
These devices contain three independent 3-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{\overline{A}+\overline{B}+\overline{C}}$ in positive logic.

The SN54ALS11A and SN54AS11 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS11A and SN74AS11 are characterized for operation from 0°C to 70°C.

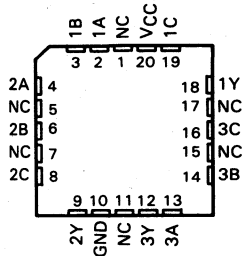
FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

SN54ALS11A, SN54AS11 . . . J PACKAGE
SN74ALS11A, SN74AS11 . . . D OR N PACKAGE
(TOP VIEW)

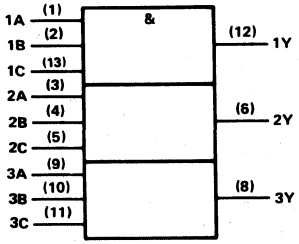


SN54ALS11A, SN54AS11 . . . FK PACKAGE
(TOP VIEW)



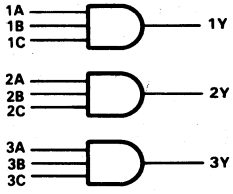
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS11A . . . . . −55 °C to 125 °C
SN74ALS11A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS11A			SN74ALS11A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS11A			SN74ALS11A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1	1.8		1	1.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		1.6	3		1.6	3	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS11A		SN74ALS11A		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	2	17	2	13	ns
t_{PHL}	Any	Y	2	14	2	10	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS11 . . . . . −55 °C to 125 °C
SN74AS11 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS11			SN74AS11			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS11			SN74AS11			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		4.3	7		4.3	7	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		11.2	18		11.2	18	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS11		SN74AS11		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1	6.5	1	6	ns
t_{PHL}	Any	Y	1	6.5	1	5.5	ns

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982 – REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

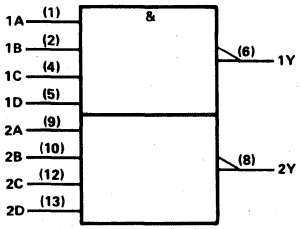
These devices contain two independent 4-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The SN54ALS20A and SN54AS20 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS20A and SN74AS20 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

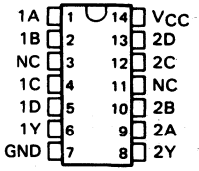
logic symbol†



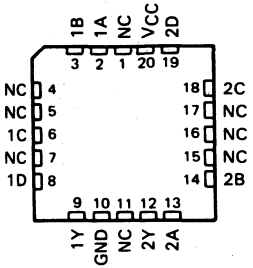
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

SN54ALS20A, SN54AS20 . . . J PACKAGE
SN74ALS20A, SN74AS20 . . . D OR N PACKAGE
(TOP VIEW)

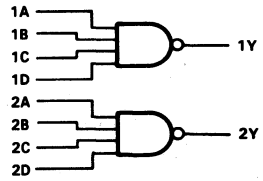


SN54ALS20A, SN54AS20 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS20A . . . . . −55°C to 125°C
SN74ALS20A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS20A			SN74ALS20A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS20A			SN74ALS20A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.22	0.4		0.22	0.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.81	1.5		0.81	1.5	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS20A	SN54ALS20A		SN74ALS20A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	7	1	18	3	11	ns
t_{PHL}	Any	Y	6	1	15	3	10	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS20 . . . . . −55°C to 125°C
SN74AS20 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS20			SN74AS20			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS20			SN74AS20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		1	1.6		1	1.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		5.4	8.7		5.4	8.7	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS20		SN74AS20		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1	5.5	1	5	ns
t_{PHL}	Any	Y	1	5	1	4.5	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982 – REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

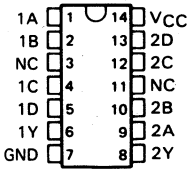
These devices contain two independent 4-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C \cdot D$ or $Y = \overline{\overline{A}+\overline{B}+\overline{C}+\overline{D}}$ in positive logic.

The SN54ALS21A and SN54AS21 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS21A and SN74AS21 are characterized for operation from 0°C to 70°C.

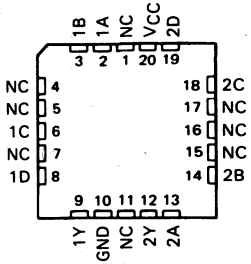
FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

SN54ALS21A, SN54AS21 . . . J PACKAGE
SN74ALS21A, SN74AS21 . . . D OR N PACKAGE
(TOP VIEW)

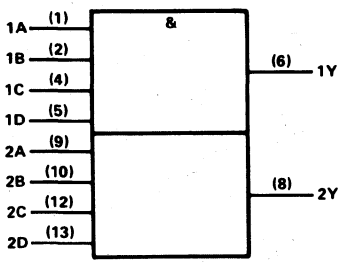


SN54ALS21A, SN54AS21 . . . FK PACKAGE
(TOP VIEW)



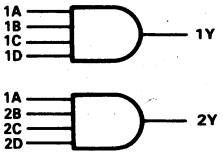
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS21A . . . . . −55°C to 125°C
SN74ALS21A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS21A			SN74ALS21A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS21A			SN74ALS21A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.85	1.4		0.85	1.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		1.4	2.3		1.4	2.3	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX			UNIT
			'ALS21A	SN54ALS21A		SN74ALS21A	
			TYP	MIN	MAX	MIN	MAX
t_{PLH}	Any	Y	8.3	4	18	4	15	ns
t_{PHL}			6.5	2	12	2	10	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS21 . . . . . −55°C to 125°C
SN74AS21 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS21			SN74AS21			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS21			SN74AS21			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA,	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.9	4.6		2.9	4.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		7.4	12		7.4	12	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS21		SN74AS21		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1	6.5	1	6	ns
t_{PHL}	Any	Y	1	6.5	1	6	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982 – REVISED JANUARY 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

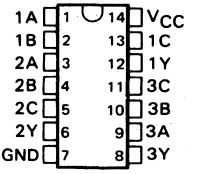
These devices contain three independent 3-input NOR gates. They perform the Boolean functions $Y = \overline{A+B+C}$ or $Y = \overline{A} \cdot \overline{B} \cdot \overline{C}$ in positive logic.

The SN54ALS27 and SN54AS27 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS27 and SN74AS27 are characterized for operation from 0°C to 70°C.

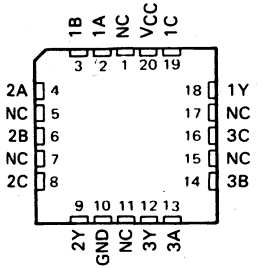
FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

SN54ALS27, SN54AS27 . . . J PACKAGE
SN74ALS27, SN74AS27 . . . D OR N PACKAGE
(TOP VIEW)

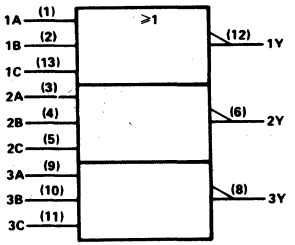


SN54ALS27, SN54AS27 . . . FK PACKAGE
(TOP VIEW)



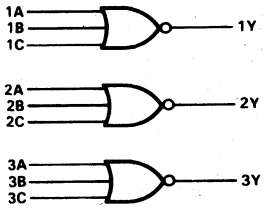
NC No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS27 . . . . . −55 °C to 125 °C
SN74ALS27 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS27			SN74ALS27			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS27			SN74ALS27			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.97	1.8		0.97	1.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		2	4		2	4	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS27		SN74ALS27		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	4	26	4	15	ns
t_{PHL}	Any	Y	1	8	3	8	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS27 . . . . . −55 °C to 125 °C
SN74AS27 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS27			SN74AS27			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS27			SN74AS27			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		4	6.4		4	6.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		10.6	17.1		10.6	17.1	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS27		SN74AS27		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1	6.5	1	5.5	ns
t_{PHL}	Any	Y	1	5	1	4.5	ns

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

MARCH 1984 – REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain a single 8-input NAND gate and perform the following Boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} \text{ OR}$$

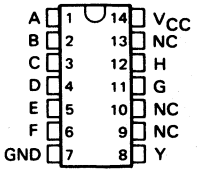
$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

The SN54ALS30A and SN54AS30 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS30A and SN74AS30 are characterized for operation from 0°C to 70°C.

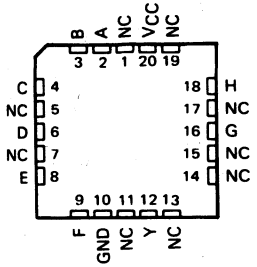
FUNCTION TABLE

INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	H

SN54ALS30A, SN54AS30 . . . J PACKAGE
SN74ALS30A, SN74AS30 . . . D OR N PACKAGE
(TOP VIEW)

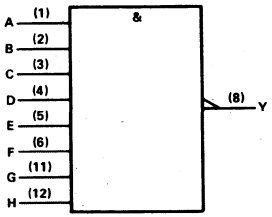


SN54ALS30A, SN54AS30 . . . FK PACKAGE
(TOP VIEW)



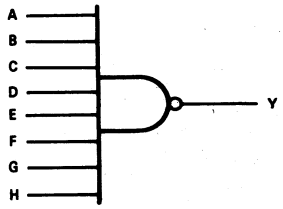
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS30A . . . . . −55 °C to 125 °C
SN74ALS30A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS30A			SN74ALS30A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS30A			SN74ALS30A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.22	0.36		0.22	0.36	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.54	0.9		0.54	0.9	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS30A		SN74ALS30A		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	3	15	3	10	ns
t_{PHL}	Any	Y	3	15	3	12	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS30 . . . . . −55 °C to 125 °C
SN74AS30 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS30			SN74AS30			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS30			SN74AS30			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.9	1.5		0.9	1.5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		3	4.9		3	4.9	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS30		SN74AS30		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1	5.5	1	5	ns
t_{PHL}	Any	Y	1	5	1	4.5	ns

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982 – REVISED JANUARY 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

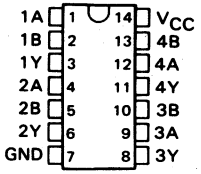
These devices contain four independent 2-input OR gates. They perform the Boolean functions $Y = A+B$ or $Y = \overline{\overline{A}\cdot\overline{B}}$ in positive logic.

The SN54ALS32 and SN54AS32 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS32 and SN74AS32 are characterized for operation from 0°C to 70°C.

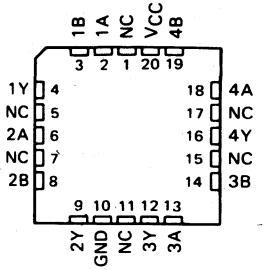
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

SN54ALS32, SN54AS32 . . . J PACKAGE
SN74ALS32, SN74AS32 . . . D OR N PACKAGE
(TOP VIEW)

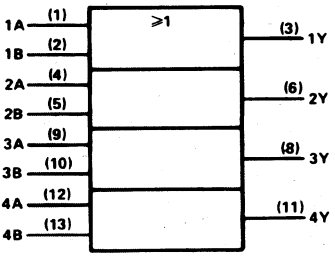


SN54ALS32, SN54AS32 . . . FK PACKAGE
(TOP VIEW)



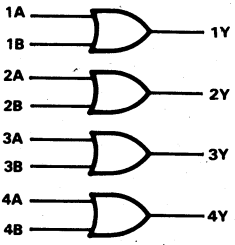
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS32 . . . . . −55°C to 125°C
SN74ALS32 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS32			SN74ALS32			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	mA
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low--level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS32			SN74ALS32			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.9	4		1.9	4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		2.6	4.9		2.6	4.9	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS32	SN54ALS32		SN74ALS32		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	8.8	3	13.5	3	13.5	ns
t_{PHL}	A or B	Y	6.8	3	16	3	12	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS32 . . . . . −55°C to 125°C
SN74AS32 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS32			SN74AS32			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	mA
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS32			SN74AS32			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		7.3	12		7.3	12	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		16.5	26.6		16.5	26.6	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 50 Ω, T_A = MIN to MAX				UNIT
			SN54AS32		SN74AS32		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	7.5	1	5.8	ns
t_{PHL}	A or B	Y	1	6.5	1	5.8	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

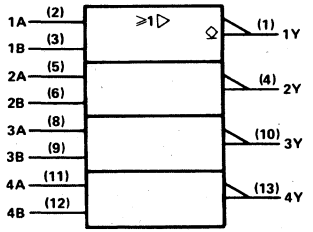
These devices contain four independent 2-input NOR buffer gates with open-collector outputs. Open-collector outputs require resistive pull-up to perform logically but can deliver higher V_{OH} levels and are commonly used in wired-AND applications. These devices perform the Boolean functions $Y = A + B$ or $Y = A \cdot B$ in positive logic.

The SN54ALS33A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS33A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

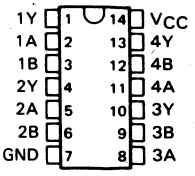
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†

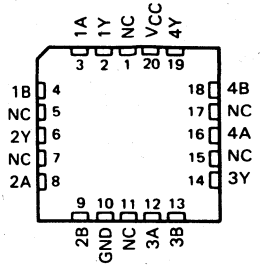


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS33A . . . J PACKAGE
SN74ALS33A . . . D OR N PACKAGE
(TOP VIEW)

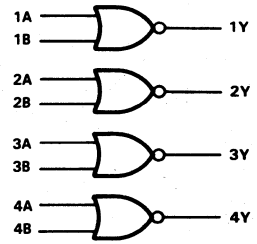


SN54ALS33A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS33A . . . . . −55°C to 125°C
SN74ALS33A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS33A			SN74ALS33A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS33A			SN74ALS33A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		1.7	2.8		1.7	2.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		5.6	9		5.6	9	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 680 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			'ALS33A			SN54ALS33A		SN74ALS33A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y		18	24	10	59	10	33	ns
t_{PHL}	A or B	Y		7	10	2	18	2	12	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982 – REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

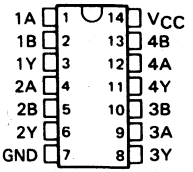
These devices contain four independent 2-input NAND buffer gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS37A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS37A is characterized for operation from 0°C to 70°C.

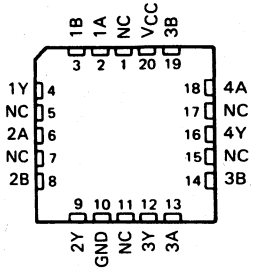
FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

SN54ALS37A . . . J PACKAGE
SN74ALS37A . . . D OR N PACKAGE
(TOP VIEW)

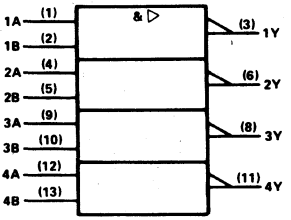


SN54ALS37A . . . FK PACKAGE
(TOP VIEW)



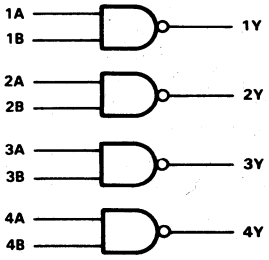
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS37A . . . . . −55°C to 125°C
SN74ALS37A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS37A			SN74ALS37A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS37A			SN74ALS37A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.86	1.6		0.86	1.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		4.8	7.8		4.8	7.8	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS37A	SN54ALS37A		SN74ALS37A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	4	2	17	2	8	ns
t_{PHL}	A or B	Y	5	2	10	2	7	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

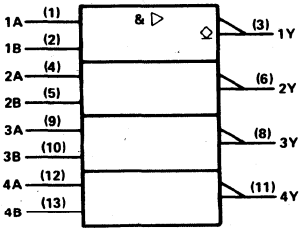
These devices contain four independent 2-input NAND buffer gates with open-collector outputs. These NAND buffers perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS38A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS38A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

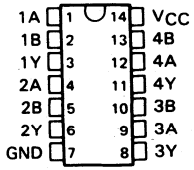
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

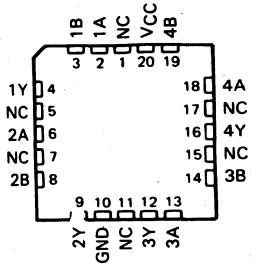


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS38A . . . J PACKAGE
SN74ALS38A . . . D OR N PACKAGE
(TOP VIEW)

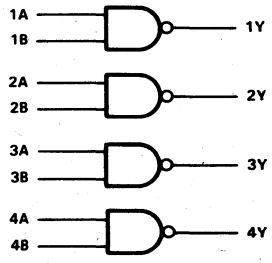


SN54ALS38A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS38A . . . . . −55°C to 125°C
SN74ALS38A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS38A			SN74ALS38A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS38A			SN74ALS38A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.86	1.6		0.86	1.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		4.8	7.8		4.8	7.8	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 680 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			'ALS38A	SN54ALS38A		SN74ALS38A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	18	10	59	10	33	ns
t_{PHL}	A or B	Y	7	2	18	2	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY (C_L = 50 pF)	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS74A	50 MHz	6 mW
'AS74	134 MHz	26 mW

description

These devices contain two independent D-type positive-edge triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

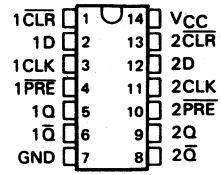
The SN54ALS74A and SN54AS74 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS74A and SN74AS74 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

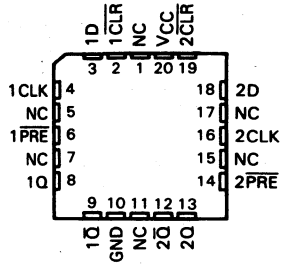
INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

†The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when Preset or Clear; returns to their inactive (high) level.

SN54ALS74A, SN54AS74 . . . J PACKAGE
SN74ALS74A, SN74AS74 . . . D OR N PACKAGE
(TOP VIEW)

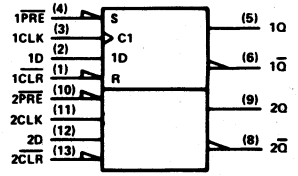


SN54ALS74A, SN54AS74 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol‡



‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS74A, SN54AS74 . . . . . −55°C to 125°C
SN74ALS74A, SN74AS74 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS74A			SN74ALS74A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage							0.8	V
					0.8†				
					0.7‡				
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		34	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	15			15			ns
		CLK high	16.5			14.5			
		CLK low	16.5			14.5			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	10			10			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

† Tested at −55°C to 70°C.
‡ Tested at 70°C to 125°C, per MIL-STD-883, method 5005, sub-group 1, 2, and 3. Static tests are performed at 25°C, 125°C, and −55°C.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS74A			SN74ALS74A			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	CLK or D	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$ or $\overline{CLR}$					0.2			0.2	
I_{IH}	CLK or D	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	CLK or D	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	$\overline{PRE}$ or $\overline{CLR}$					−0.4			−0.4	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.4	4		2.4	4	mA

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with D, CLK, and $\overline{PRE}$ grounded, then with D, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN TO MAX				UNIT
			SN54ALS74A		SN74ALS74A		
			MIN	MAX	MIN	MAX	
f_{max}			25		34		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	13.5	3	13	ns
t_{PHL}			5	17	5	15	
t_{PLH}	CLK	Q or $\overline{Q}$	5	17	5	16	ns
t_{PHL}			5	18	5	18	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

			SN54AS74			SN74AS74			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		90	0		105	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4			4			ns
		CLK high	4			4			
		CLK low	5.5			5.5			
t_{su}	Setup time before CLK↑	Data	4.5			4.5			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2			2			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS74			SN74AS74			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	CLK or D	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	CLK or D	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	$\overline{PRE}$ or $\overline{CLR}$					−1.8			−1.8	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		10.5	16		10.5	16	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with D, CLK, and $\overline{PRE}$ grounded, then with D, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN TO MAX				UNIT
			SN54AS74A		SN74AS74A		
			MIN	MAX	MIN	MAX	
f_{max}			90		105		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	8.5	3	7.5	ns
t_{PHL}			3.5	11.5	3.5	10.5	
t_{PLH}	CLK	Q or $\overline{Q}$	3.5	9	3.5	8	ns
t_{PHL}			4.5	10.5	4.5	9	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982 – REVISED AUGUST 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions $Y = A \oplus B = \overline{A}B + A\overline{B}$ in positive logic.

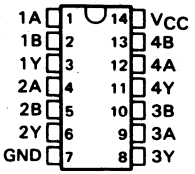
A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN54ALS86 and SN54AS86A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS86 and SN74AS86A are characterized for operation from 0°C to 70°C.

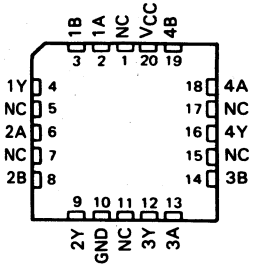
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

SN54ALS86, SN54AS86A . . . J PACKAGE
SN74ALS86, SN74AS86A . . . D OR N PACKAGE
(TOP VIEW)

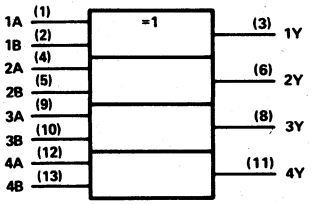


SN54ALS86, SN54AS86A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-OR

These are five equivalent Exclusive-OR symbols valid for an 'ALS86 or 'AS86A gate in positive logic; negation may be shown at any two ports.

LOGIC IDENTITY ELEMENT

The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY

The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT

The output is active (high) if an odd number of inputs only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS86 . . . . . −55°C to 125°C
SN74ALS86 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS86			SN74ALS86			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over-recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS86			SN74ALS86			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	All inputs at 4.5 V		3.9	5.9		3.9	5.9	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS86		SN74ALS86		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B (other input low)	Y	3	22	3	17	ns
t_{PHL}			2	14	2	12	
t_{PLH}	A or B (other input high)	Y	3	22	3	17	ns
t_{PHL}			2	12	2	10	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS86A . . . . . −55°C to 125°C
SN74AS86A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stress beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS86A			SN74AS86A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over-recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS86A			SN74AS86A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V, $V_{I(B)}$ = 0	$V_{I(A)}$ = 4.5 V,		11	18		11	18	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		20	38		20	38	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

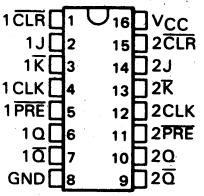
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS86A		SN74AS86A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2	8.5	2	7.5	ns
t_{PHL}	(other input low)		2	8	2	6.5	
t_{PLH}	A or B	Y	1	8	1	6.5	ns
t_{PHL}	(other input high)		1	9	1	7	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

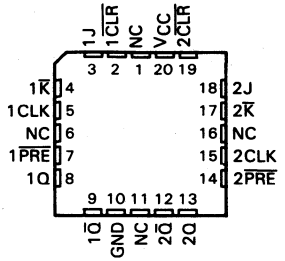
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS109A	50 MHz	6 mW
'AS109	129 MHz	29 mW

SN54ALS109A, SN54AS109 . . . J PACKAGE
SN74ALS109A, SN74AS109 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS109A, SN54AS109 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These devices contain two independent J-$\overline{K}$ positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and $\overline{K}$ input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and $\overline{K}$ inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{K}$ and trying J high. They also can perform as D-type flip-flops if J and $\overline{K}$ are tied together.

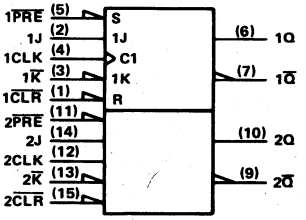
The SN54ALS109A and SN54AS109 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS109A and SN74AS109 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

* The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS109A, SN54AS109 . . . . . −55°C to 125°C
SN74ALS109A, SN74AS109 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS109A			SN74ALS109A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		30	0		34	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	15			15			ns
		CLK high	16.5			14.5			
		CLK low	16.5			14.5			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	10			10			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS109A			SN74ALS109A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	CLK, J, or $\overline{K}$	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$ or $\overline{CLR}$					0.2			0.2	
I_{IH}	CLK, J, or $\overline{K}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	CLK, J or $\overline{K}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	$\overline{PRE}$ or $\overline{CLR}$					−0.4			−0.4	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.4	4		2.4	4	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, $\overline{K}$, CLK, and $\overline{PRE}$ grounded, then with J, $\overline{K}$, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS109A		SN74ALS109A		
			MIN	MAX	MIN	MAX	
f_{max}			30		34		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	17	3	13	ns
t_{PHL}			5	17	5	15	
t_{PLH}	CLK	Q or $\overline{Q}$	5	21	5	16	ns
t_{PHL}			5	20	5	18	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

			SN54AS109			SN74AS109			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		90	0		105	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4			4			ns
		CLK high	4			4			
		CLK low	5.5			5.5			
t_{su}	Setup time before CLK↑	Data	5.5			5.5			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2			2			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS109			SN74AS109			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	CLK, J or $\overline{K}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	CLK, J or $\overline{K}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			0.5	mA
	$\overline{PRE}$ or $\overline{CLR}$					−1.8			−1.8	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		11.5	17		11.5	17	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, $\overline{K}$, CLK, and $\overline{PRE}$ grounded, then with J, $\overline{K}$, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS109		SN74AS109		
			MIN	MAX	MIN	MAX	
f_{max}			90		105		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	9	3	8	ns
t_{PHL}			3.5	11.5	3.5	10.5	
t_{PLH}	CLK	Q or $\overline{Q}$	3.5	10	3.5	9	ns
t_{PHL}			4.5	10.5	4.5	9	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

- **Fully Buffered to Offer Maximum Isolation from External Disturbance**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS112A	50 MHz	6 mW

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

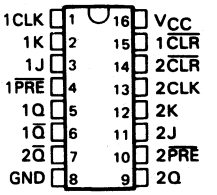
The SN54ALS112A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS112A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

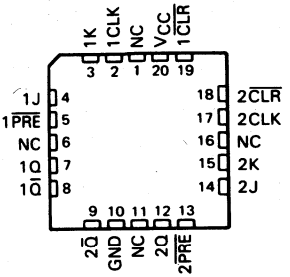
INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

†The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH}. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

SN54ALS112A . . . J PACKAGE
SN74ALS112A . . . D OR N PACKAGE
(TOP VIEW)

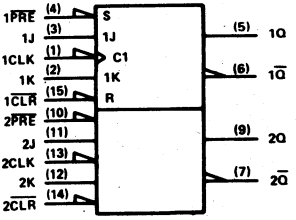


SN54ALS112A . . . FK PACKAGE
(TOP VIEW)



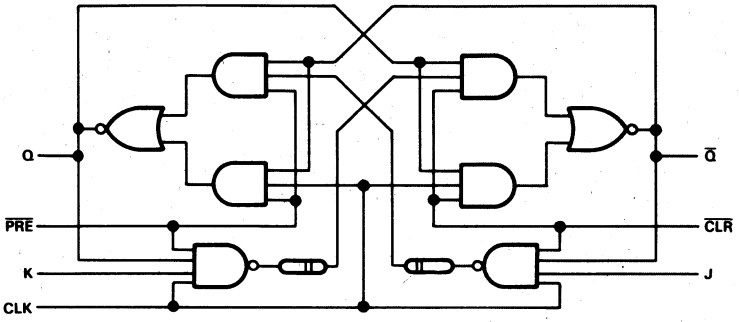
NC – No internal connection

logic symbol‡



‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS112A . . . . . −55°C to 125°C
SN74ALS112A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS112A			SN74ALS112A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		30	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	15			10			ns
		CLK high	20			16.5			
		CLK low	20			16.5			
t_{su}	Setup time before CLK↓	Data	25			22			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	22			20			
t_h	Hold time, data after CLK↓		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristice over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS112A			SN74ALS112A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 7 V			0			0.1	mA
	$\overline{PRE}$ or $\overline{CLR}$					0.2			0.2	
I_{IH}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	J, K, or CLK	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	$\overline{PRE}$ or $\overline{CLR}$					−0.4			−0.4	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.5	4.5		2.5	4.5	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, K, CLK, and $\overline{PRE}$ grounded, then with J, K, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS112A		SN74ALS112A		
			MIN	MAX	MIN	MAX	
f_{max}			25		30		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	26	3	15	ns
t_{PHL}			4	23	4	18	
t_{PLH}	CLK	Q or $\overline{Q}$	3	23	3	15	ns
t_{PHL}			5	24	5	19	

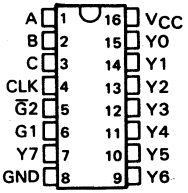
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS REGISTERS

D2661, APRIL 1982 – REVISED MAY 1986

- **Combines Decoder and 3-Bit Address Register**
- **Incorporates 2 Enable Inputs to Simplify Cascading**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

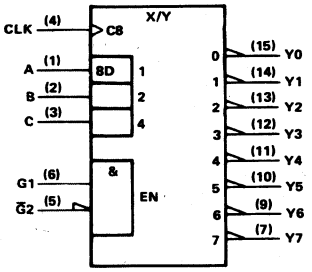
SN74AS131A . . . D OR N PACKAGE
(TOP VIEW)

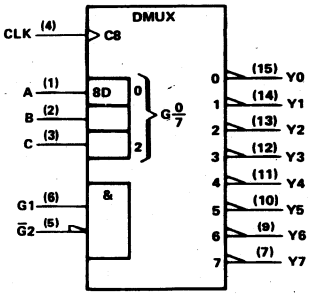


description

The 'AS131A is a three-line to eight-line decoder/demultiplexer with registers on the three address inputs. When the clock input (CLK) goes from low to high, the 'AS131A acts as decoder/demultiplexer and the address present at the select inputs (A, B, and C) is stored in the registers. Further address changes are ignored until the next rising transition of CLK. The output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or CLK inputs. All of the outputs are high unless G1 is high and $\overline{G2}$ is low. The 'AS131A is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

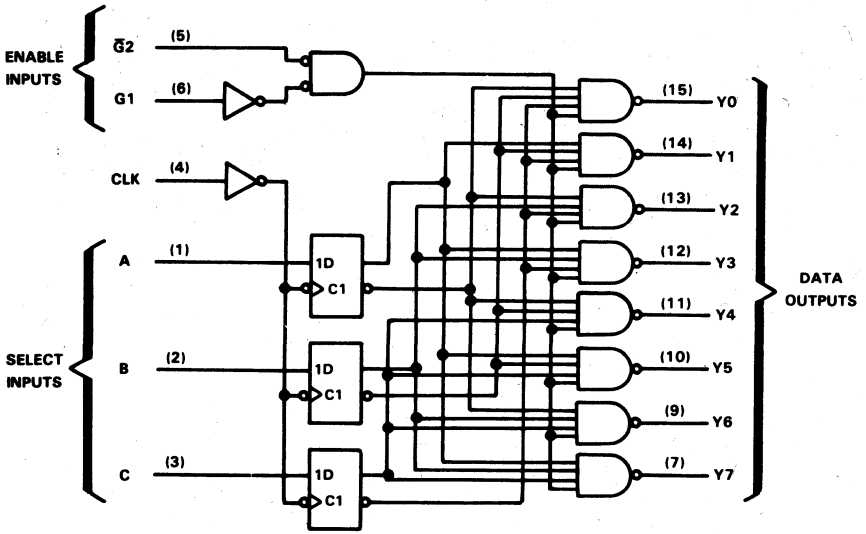
The SN74AS131A is characterized for operation from 0°C to 70°C.





†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D and N packages.

FUNCTION TABLE

INPUTS						OUTPUTS							
CLK	ENABLE		SELECT										
	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
↑	H	L	L	L	L	L	H	H	H	H	H	H	H
↑	H	L	L	L	H	H	L	H	H	H	H	H	H
↑	H	L	L	H	L	H	H	L	H	H	H	H	H
↑	H	L	L	H	H	H	H	H	L	H	H	H	H
↑	H	L	H	L	L	H	H	H	H	L	H	H	H
↑	H	L	H	L	H	H	H	H	H	H	L	H	H
↑	H	L	H	H	L	H	H	H	H	H	H	L	H
↑	H	L	H	H	H	H	H	H	H	H	H	H	L
L or H	H	L	X	X	X	OUTPUTS CORRESPONDING TO STORED ADDRESS, L; ALL OTHERS, H							

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN74AS131A . . . . . −0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN74AS131A			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				20	mA
f_{clock}	Clock frequency		0		100	MHz
t_w	Pulse duration	CLK high	5			ns
		CLK low	5			
t_{su}	Setup time at A, B, and C before CLK ↑		3.5			ns
t_h	Hold time at A, B, and C after CLK↑		0			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74AS131A			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V			15	29	mA
I_{CCL}	V_{CC} = 5.5 V			16	30	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half on the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX		UNIT
			SN74AS131A		
			MIN	MAX	
f_{max}			100		MHz
t_{PLH}	CLK	Y	2	14.5	ns
t_{PHL}			2	9.5	
t_{PLH}	G1	Y	2	10	ns
t_{PHL}			2	9	
t_{PLH}	$\overline{G2}$	Y	2	7	ns
t_{PHL}			2	8.5	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982 – REVISED MAY 1986

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain a single 13-input NAND gate. They perform the Boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M}$$

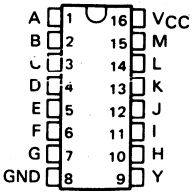
$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H} + \overline{I} + \overline{J} + \overline{K} + \overline{L} + \overline{M}$$

The SN54ALS133 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS133 is characterized for operation from 0°C to 70°C.

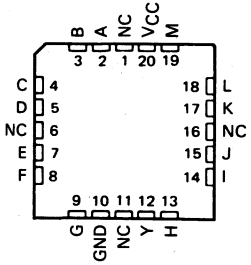
FUNCTION TABLE

INPUTS A THRU M	OUTPUT Y
All inputs H	L
One or more inputs L	H

SN54ALS133 . . . J PACKAGE
SN74ALS133 . . . D OR N PACKAGE
(TOP VIEW)

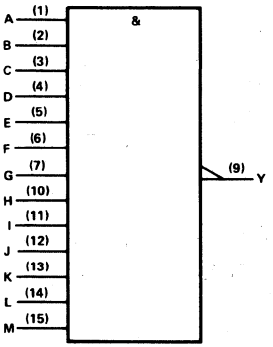


SN54ALS133 . . . FK PACKAGE
(TOP VIEW)



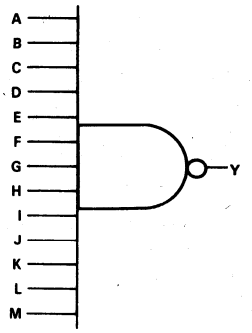
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS133 . . . . . −55°C to 125°C
SN74ALS133 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS133			SN74ALS133			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS133			SN74ALS133			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.24	0.34		0.24	0.34	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.56	0.8		0.56	0.8	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS133	SN54ALS133		SN74ALS133		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	8	1	16	3	11	ns
t_{PHL}	Any	Y	17	5	47	5	25	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

D2661, APRIL 1982 – REVISED MAY 1986

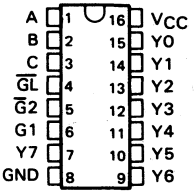
- **Combines Decoder and 3-Bit Address Latch**
- **Incorporates 2 Output Enables to Simplify Cascading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

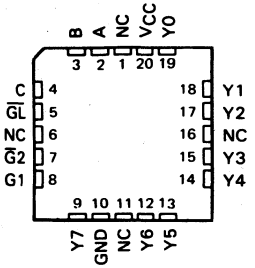
The 'ALS137 is a three-line to eight-line decoder/demultiplexer with latches on the three address inputs. When the latch-enable input ($\overline{GL}$) is low, the 'ALS137 acts as a decoder/demultiplexer. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as $\overline{GL}$ remains high. The output enable controls, G1 and $\overline{G2}$, control the outputs independently of the select ot latch-enable inputs. All of the outputs are forced high if G1 is low or $\overline{G2}$ is high. The 'ALS137 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

The SN54ALS137 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS137 and SN74AS137 are characterized for operation from 0 °C to 70 °C.

SN54ALS137 . . . J PACKAGE
SN74ALS137, SN74AS137 . . . D OR N PACKAGE
(TOP VIEW)

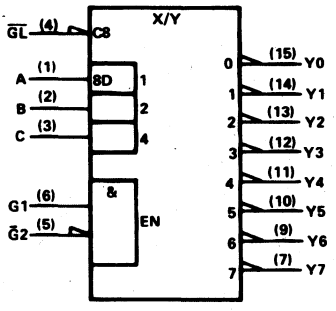


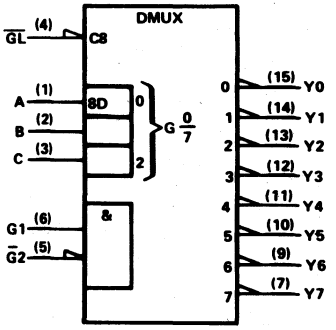
SN54ALS137 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

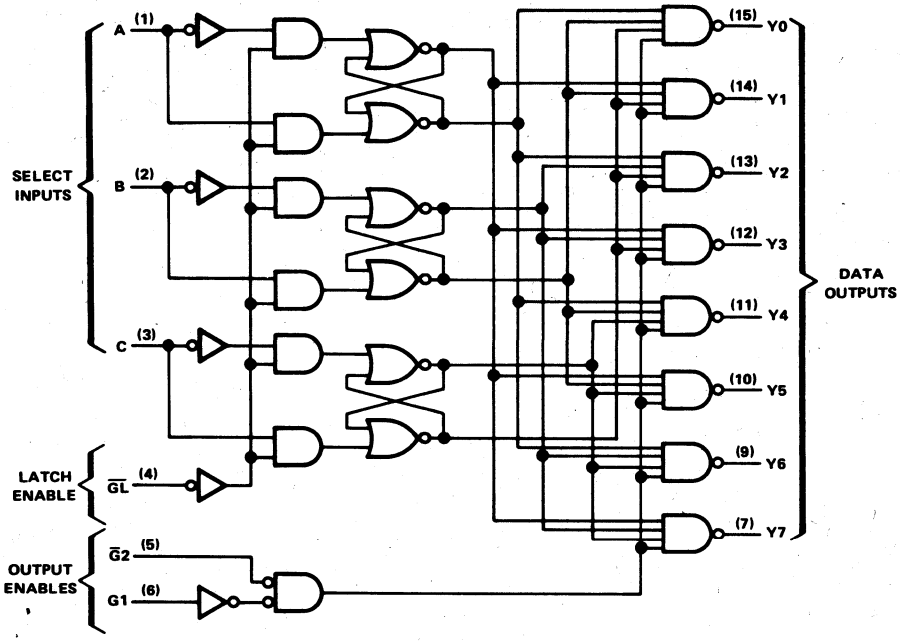
logic symbols (alternatives)†





†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS137 . . . . . −55°C to 125°C
SN74ALS137, SN74AS137 . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 150°C

		SN54ALS137			SN74ALS137			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
t_w	Pulse duration, $\overline{GL}$ low	15			10			ns
t_{su}	Setup time at A, B, and C before $\overline{GL}$↑	15			10			ns
t_h	Hold time at A, B, and C after $\overline{GL}$↑	5			5			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS137			SN74ALS137			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			5	11		5	11	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS137		SN74ALS137		
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Y	5	25	5	20	ns
t_{PHL}			6	25	6	20	
t_{PLH}	$\overline{G2}$	Y	4	15	4	12	ns
t_{PHL}			5	18	5	15	
t_{PLH}	G1	Y	5	21	5	17	ns
t_{PHL}			5	19	5	15	
t_{PLH}	$\overline{GL}$	Y	7	27	7	22	ns
t_{PHL}			7	25	7	20	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN74AS137			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			-2	mA
I_{OL}	Low-level output current			20	mA
t_w	Pulse duration, $\overline{GL}$ low	4.5			ns
t_{su}	Setup times at A, B, and C before $\overline{GL}$↑	4			ns
t_h	Hold time at A, B, and C after $\overline{GL}$↑	1			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74AS137			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = -18 mA			-1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = -2 mA	V_{CC}-2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			-1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	-30		-112	mA
I_{CC}	V_{CC} = 5.5 V			15	24	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half on the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

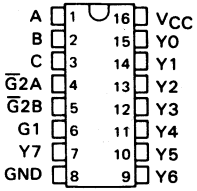
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX		UNIT
			SN74AS137		
			MIN	MAX	
t_{PLH}	A, B, C	Y	2	12.5	ns
t_{PHL}			2	12.5	
t_{PLH}	$\overline{G2}$	Y	2	8	ns
t_{PHL}			2	8.5	
t_{PLH}	G1	Y	2	10	ns
t_{PHL}			2	9	
t_{PLH}	$\overline{GL}$	Y	3	13.5	ns
t_{PHL}			3	14	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

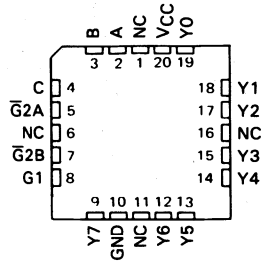
D2661, APRIL 1982 – REVISED MAY 1986

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates 3 Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS138, SN54AS138 . . . J PACKAGE
SN74ALS138, SN74AS138 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS138, SN54AS138 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

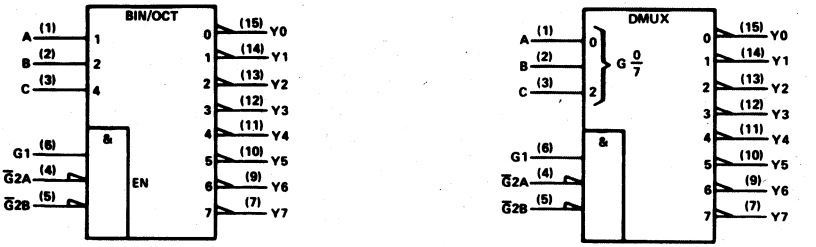
description

The 'ALS138 and 'AS138 circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

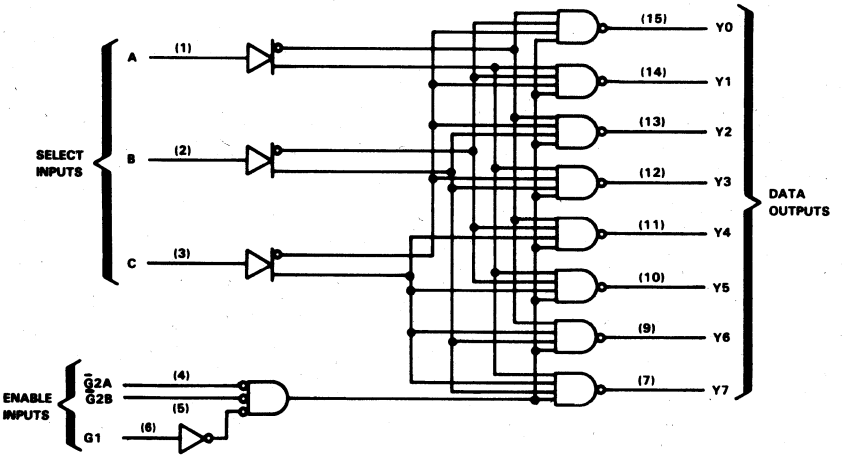
The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN54ALS138 and SN54AS138 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS138 and SN74AS138 are characterized for operation from 0°C to 70°C.

logic symbols (alternatives)†



logic diagram (positive logic)



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range; SN54ALS138, SN54AS138 . . . . . −55°C to 125°C
SN74ALS138, SN74AS138 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS138			SN74ALS138			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS138			SN74ALS138			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			5	10		5	10	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS138		SN74ALS138		
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Any Y	2	28	6	22	ns
t_{PHL}			6	22	6	18	
t_{PLH}	Enable	Any Y	2	22	4	17	ns
t_{PHL}			4	21	5	17	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54AS138			SN74AS138			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS138			SN74AS138			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V			12	17.5		12	17.5	mA
I_{CCL}	V_{CC} = 5.5 V			14	20		14	20	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

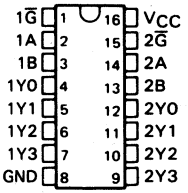
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS138		SN74AS138		
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Any Y	2	11	2	10	ns
t_{PHL}			2	11	2	9.5	
t_{PLH}	G1	Any Y	2	11.5	2	10	ns
t_{PHL}			2	11	2	10	
t_{PLH}	$\overline{G2}$	Any Y	2	9	2	7.5	
t_{PHL}			2	10	2	8.5	

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

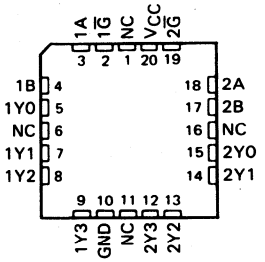
D2661, APRIL 1982 – REVISED MAY 1986

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates 2 Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS139 . . . . J PACKAGE
SN74ALS139 . . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS139 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'ALS139 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

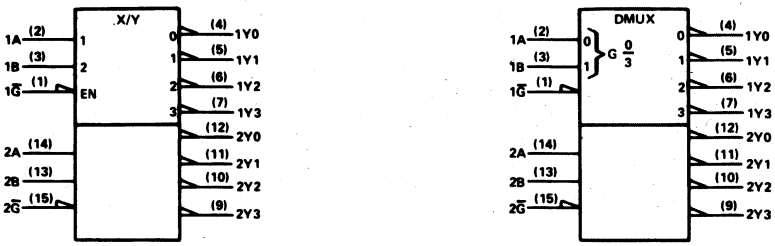
The 'ALS139 is comprised of two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

The SN54ALS139 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS139 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

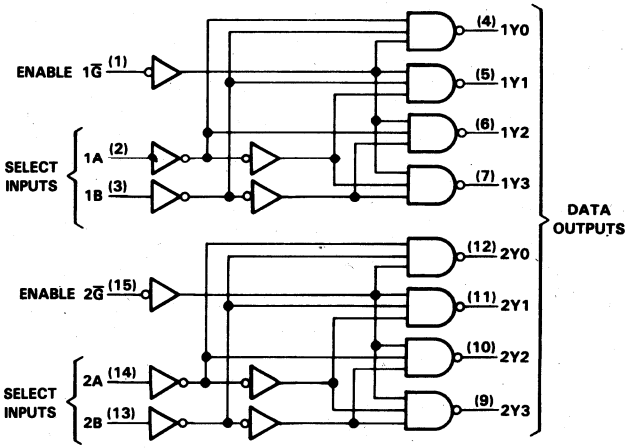
INPUTS			OUTPUTS			
ENABLE	SELECT					
$\overline{G}$	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

logic symbols† (alternatives)



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pins numbers shown are for D, J, and N packages.

functional block diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS139 . . . . . −55°C to 125°C
SN74ALS139 . . . . . −0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS139			SN74ALS139			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS139			SN74ALS139			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			8	13		8	13	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

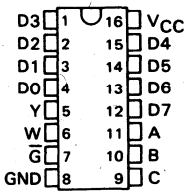
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS139	SN54ALS139		SN74ALS139		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	9	3	17	3	14	ns
t_{PHL}			9	3	17	3	14	
t_{PLH}	$\overline{G}$	Y	9	3	17	3	14	ns
t_{PHL}			9	3	18	3	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982 – REVISED MAY 1986

- **8-Line to 1-Line Multiplexers Can Perform As:**
  - **Boolean Function Generators**
  - **Parallel-to-Serial Converters**
  - **Data Source Selectors**
- **Input Clamping Diodes Simplify System Design**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS151 . . . J PACKAGE
SN74ALS151, SN74AS151 . . . D OR N PACKAGE
(TOP VIEW)

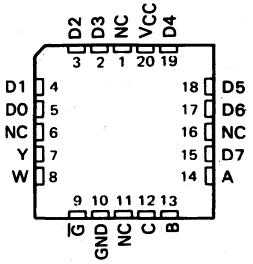


description

These monolithic data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe input ($\overline{G}$) must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

The SN54ALS151 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS151 and SN74AS151 are characterized for operation from 0°C to 70°C.

SN54ALS151 . . . FK PACKAGE
(TOP VIEW)



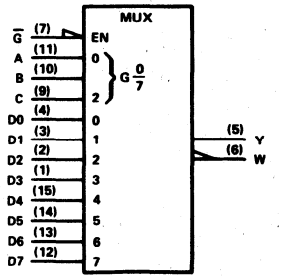
NC – No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	$\overline{G}$	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level, L = low level, X = irrelevant
D0, D1 . . . D7 = the level of the D respective input

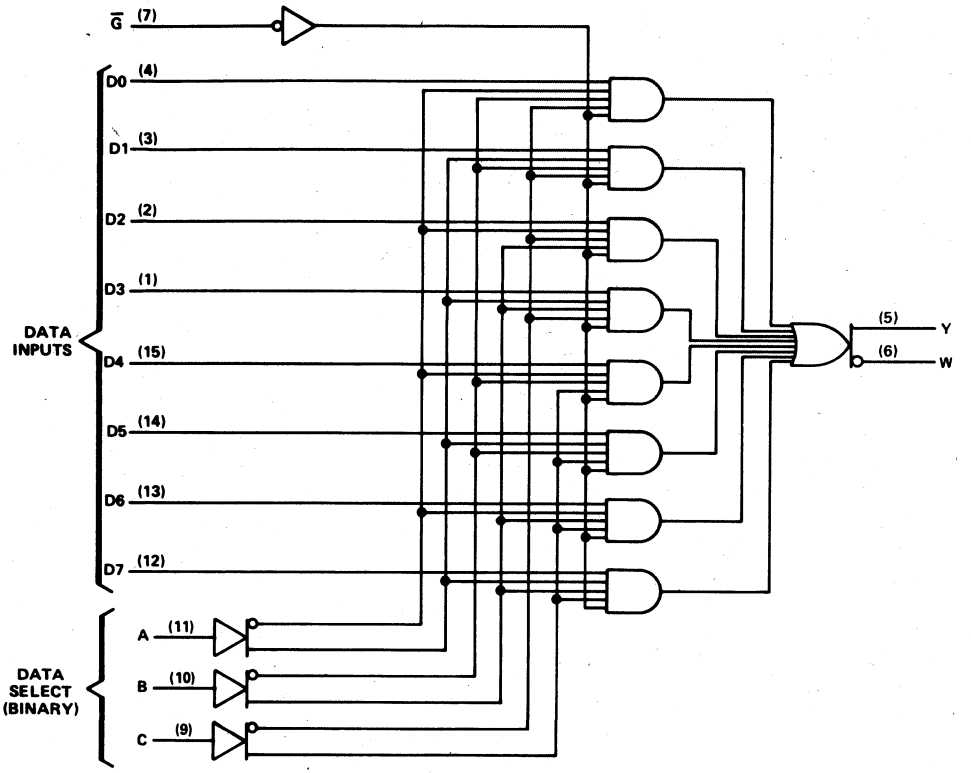
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

TEXAS INSTRUMENTS

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS151 . . . . . −55°C to 125°C
SN74ALS151, SN74AS151 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS151			SN74ALS151			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS151			SN74ALS151			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	Inputs at 4.5 V		7.5	12		7.5	12	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS151		SN74ALS151		
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, or C	Y	4	21	4	18	ns
t_{PHL}			8	35	8	24	
t_{PLH}	A, B, or C	W	7	36	7	24	ns
t_{PHL}			7	26	7	23	
t_{PLH}	Any D	Y	3	14	3	10	ns
t_{PHL}			5	21	5	15	
t_{PLH}	Any D	W	3	23	3	15	ns
t_{PHL}			4	20	4	15	
t_{PLH}	$\overline{G}$	Y	4	21	4	18	ns
t_{PHL}			4	25	4	19	
t_{PLH}	$\overline{G}$	W	5	27	5	19	ns
t_{PHL}			5	26	5	23	

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN74AS151			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74AS151			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA				
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	
I_I	A, B, or C	V_{CC} = 5.5 V,	V_I = 7 V			0.2	mA
	All others					0.1	
I_{IH}	A, B, or C	V_{CC} = 5.5 V,	V_I = 2.7 V			40	μA
	All others					20	
I_{IL}	A, B, or C	V_{CC} = 5.5 V,	V_I = 0.4 V			−1	mA
	All others					−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,			18.6	30	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half on the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

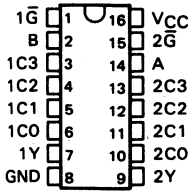
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX		UNIT
			SN74AS151		
			MIN	MAX	
t_{PLH}	A, B, or C	Y	4.5	14.5	ns
t_{PHL}			4.5	15	
t_{PLH}	A, B, or C	W	4	12	ns
t_{PHL}			4	12	
t_{PLH}	Any D	Y	3	10.5	ns
t_{PHL}			3	11	
t_{PLH}	Any D	W	2	6.5	ns
t_{PHL}			1	4.5	
t_{PLH}	$\overline{G}$	Y	4.5	14	ns
t_{PHL}			3	11	
t_{PLH}	$\overline{G}$	W	1.5	6	ns
t_{PHL}			3	10	

Note 1: Load circuit and voltage waveforms are shown in Section 1.

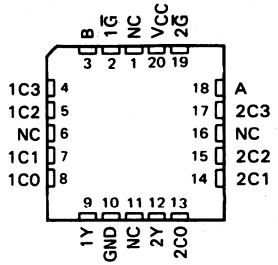
D2661, APRIL 1982 – REVISED MAY 1986

- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Strobe (Enable) Line Provided for Cascading (N lines to n lines)**
- **'ALS253 and 'AS253 Are 3-State Versions of These Parts**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS153 . . . J PACKAGE
SN74ALS153, SN74AS153 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS153 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate strobe inputs (G) are provided for each of the two four-line sections.

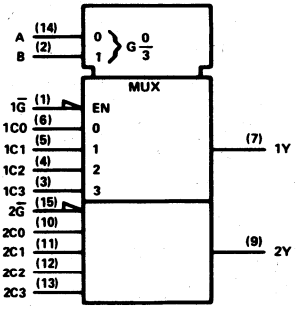
The SN54ALS153 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS153 and SN74AS153 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

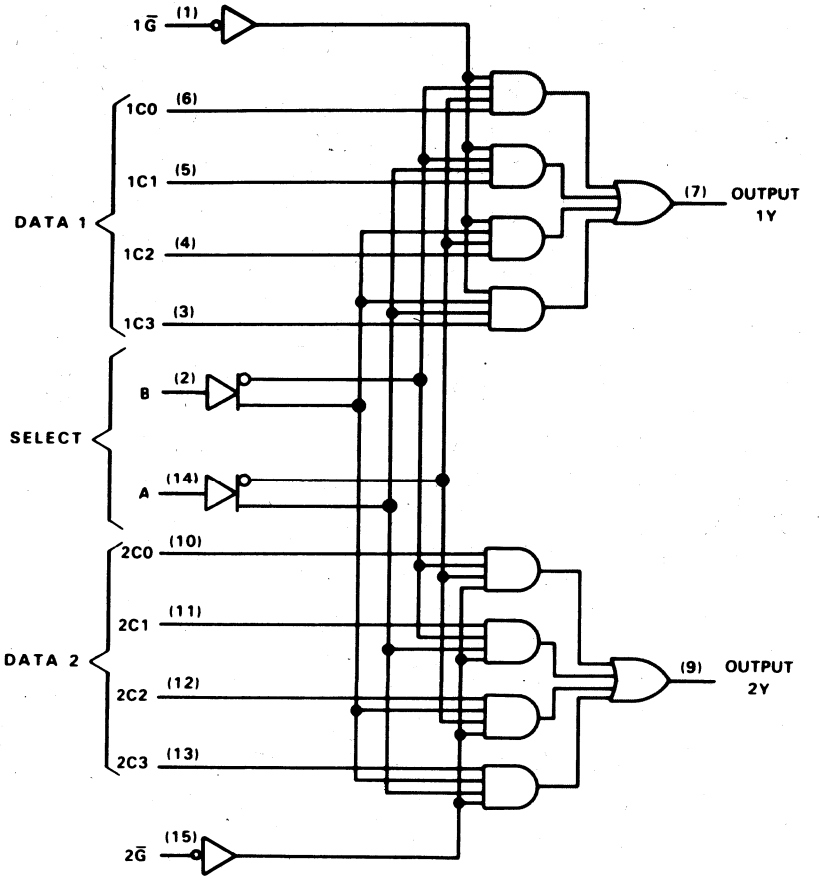
Select inputs A and B are common to both sections.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS153 . . . . . −55°C to 125°C
SN74ALS153, SN74AS153 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS153			SN74ALS153			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS153			SN74ALS153			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	All inputs at 4.5 V		7.5	14		7.5	14	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS153		SN74ALS153		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	5	29	5	21	ns
t_{PHL}			5	27	5	21	
t_{PLH}	Data (Any C)	Y	3	15	3	10	ns
t_{PHL}			2	18	4	15	
t_{PLH}	G	Y	5	27	5	18	ns
t_{PHL}			3	22	5	18	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN74AS153			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74AS153			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA				
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	
I_I	A, B	V_{CC} = 5.5 V,	V_I = 7 V			0.2	mA
	All others					0.1	
I_{IH}	A, B	V_{CC} = 5.5 V,	V_I = 2.7 V			40	μA
	All others					20	
I_{IL}	A, B	V_{CC} = 5.5 V,	V_I = 0.4 V			−1	mA
	All others					−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	Outputs high		16	26	mA
			Outputs low		21	33	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half on the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX		UNIT
			SN74AS153		
			MIN	MAX	
t_{PLH}	A or B	Y	3	12.5	ns
t_{PHL}			3	11	
t_{PLH}	Data (Any C)	Y	2	7	ns
t_{PHL}			2	8	
t_{PLH}	$\overline{G}$	Y	3	11.5	ns
t_{PHL}			2	9	

Note 1: Load circuit and voltage waveforms are shown in Section 1.

- **Applications:**
  - **Dual 2-Line to 4-Line Decoder**
  - **Dual 1-Line to 4-Line Demultiplexer**
  - **3-Line to 8-Line Decoder**
  - **1-Line to 8-Line Demultiplexer**
- **Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words**

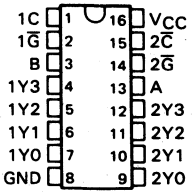
description

The 'ALS156 circuits feature dual 1-line to 4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit enabling or disabling each of the 4-bit sections as desired.

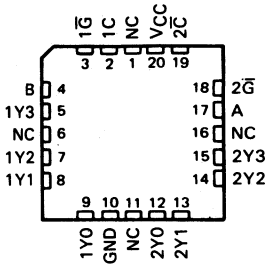
Data applied to input 1C is inverted at its outputs and data applied at input $2\overline{C}$ is not inverted through its outputs. The inverter following the 1C data input permits use of the 'ALS156 as a 3-line to 8-line demultiplexer without external gating. All inputs are clamped with high-performance Schottky diodes to suppress line ringing and simplify system design.

The SN74ALS156 is characterized for operation from 0°C to 70°C.

D OR N PACKAGE
(TOP VIEW)

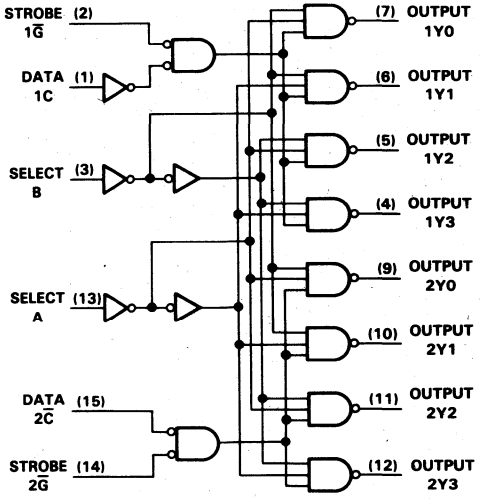


FN PACKAGE
(TOP VIEW)



NC—No internal connection

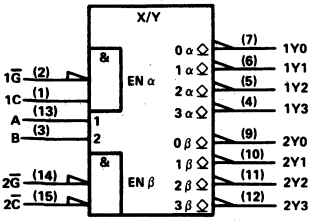
logic diagram (positive logic)



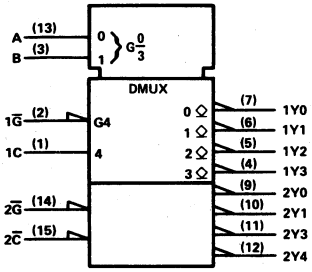
TEXAS INSTRUMENTS

logic symbols† (alternatives)

2-LINE TO 4-LINE DECODER



1-LINE TO 4-LINE DEMULTIPLEXER



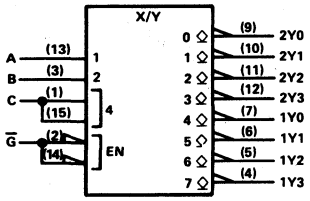
FUNCTION TABLE

2-LINE TO 4-LINE DECODER
OR
1-LINE TO 4-LINE DEMULTIPLEXER

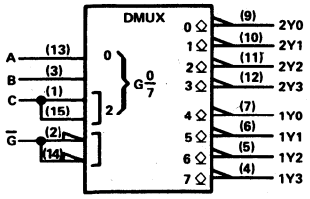
INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1$\overline{G}$	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2$\overline{G}$	2$\overline{C}$	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-LINE TO 8-LINE DECODER



1-LINE TO 8-LINE DEMULTIPLEXER



FUNCTION TABLE

3-LINE TO 8-LINE DECODER
OR
1-LINE TO 8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C‡	B	A	$\overline{G}$§	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

‡ C = inputs 1C and 2$\overline{C}$ connected together
§ $\overline{G}$ = inputs 1$\overline{G}$ and 2$\overline{G}$ connected together

† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown on logic symbols are for D and N packages only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage			5.5	V
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1	mA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	μA
I_{CCL}	V_{CC} = 5.5 V			5	9	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics‡

PARAMETER	FROM	TO	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 0°C to 70°C		UNIT
			TYP	MIN	MAX	
t_{PLH}	A, B	1Y, 2Y	30	13	55	ns
t_{PHL}			12	6	25	
t_{PLH}	1C	1Y	38	18	50	ns
t_{PHL}			12	6	23	
t_{PLH}	$1\overline{G}$	1Y	24	13	38	ns
t_{PHL}			13	6	22	
t_{PLH}	$2\overline{C}$, $2\overline{G}$	2Y	24	13	38	ns
t_{PHL}			13	6	22	

‡ For load circuits and voltage waveforms see Section 1.

- **Buffered Inputs and Outputs**
- **Package Options Include Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

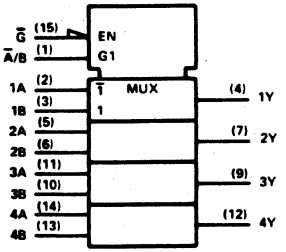
description

These monolithic data selectors/multiplexers contain inverters and drivers to supply full data selection to the four output gates. A separate strobe input ($\overline{G}$) is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The 'ALS157A and 'AS157 present true data whereas the 'ALS158 and 'AS158 present inverted data to minimize propagation delay time.

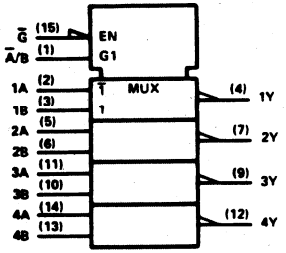
The SN54' family is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74' family is characterized for operation from 0 °C to 70 °C.

logic symbol†

'ALS157A, 'AS157

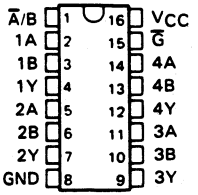


'ALS158, 'AS158

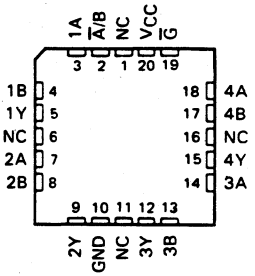


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS', SN54AS' ... J PACKAGE
SN74ALS', SN74AS' ... D OR N PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' ... FK PACKAGE
(TOP VIEW)

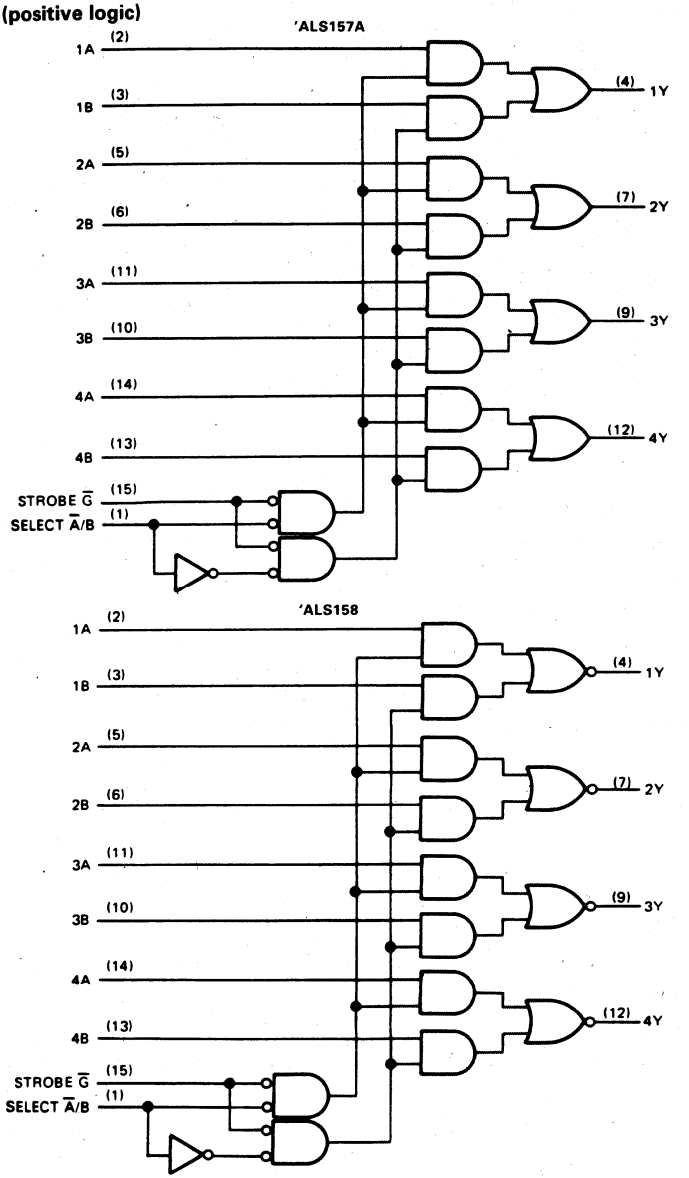


NC – No internal connection

FUNCTION TABLE

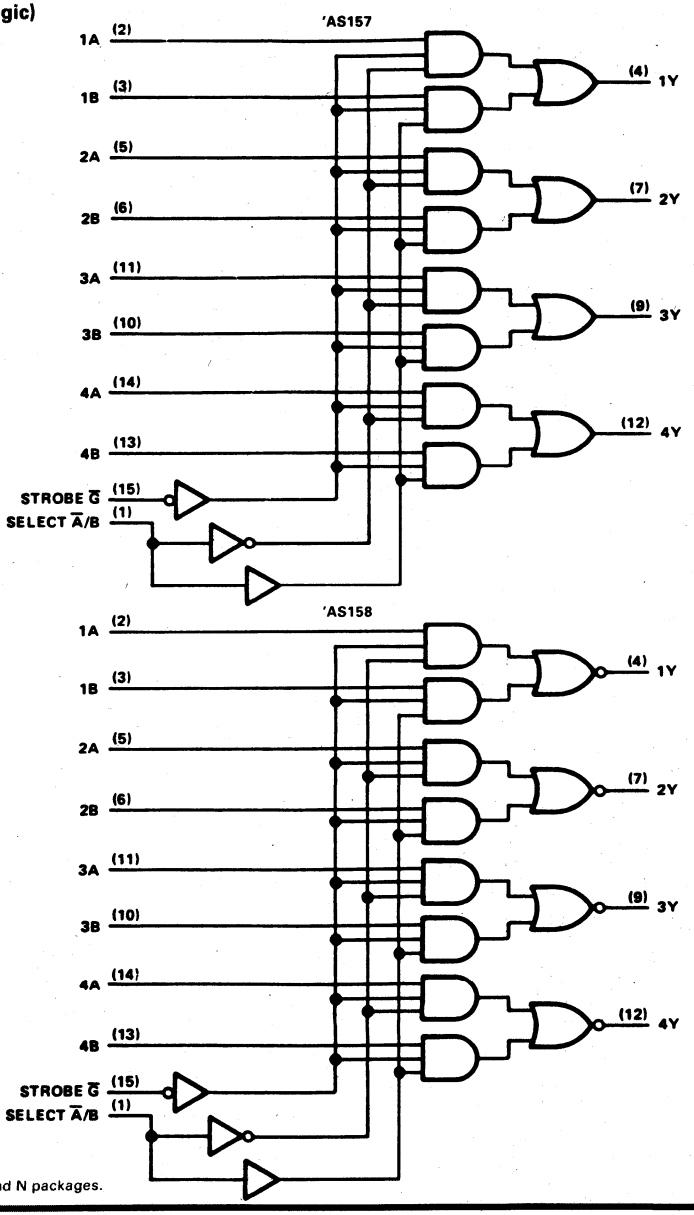
INPUTS				OUTPUT Y	
STROBE	SELECT	DATA		'ALS157A	'ALS158
$\overline{G}$	$\overline{A}$/B	A	B	'AS157	'AS158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

logic diagrams (positive logic)



Pin numbers shown are for D, J, and N packages

logic diagrams (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS157A, SN54ALS158 . . . . . −55 °C to 125 °C
SN74ALS157A, SN74ALS158 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS157A SN54ALS158			SN74ALS157A SN74ALS158			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS157A SN54ALS158			SN74ALS157A SN74ALS158			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O*		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS157A	V_{CC} = 5.5 V,	See Note 1		6	11		6	11	mA
	'ALS158				5	10		5	10	

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
* The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current, I_{OS}.
NOTE 1: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

'ALS157A switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25 °C,	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS157A	SN54ALS157A		SN74ALS157A		
			TYP	MIN	MAX	MIN	MAX	
tPLH	A or B	Y	9	4	17	4	14	ns
tPHL			6	2	15	2	12	
tPLH	$\overline{A}$/B	Y	15	7	28	7	24	ns
tPHL			9	4	20	4	17	
tPLH	$\overline{G}$	Y	14	7	25	7	20	ns
tPHL			10	4	18	4	13	

'ALS158 switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25 °C,	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS158	SN54ALS158		SN74ALS158		
			TYP	MIN	MAX	MIN	MAX	
tPLH	A or B	Y	9	4	18	4	15	ns
tPHL			5	2	12	2	8	
tPLH	$\overline{A}$/B	Y	13	5	22	5	18	ns
tPHL			13	5	22	5	18	
tPLH	$\overline{G}$	Y	13	5	22	5	18	ns
tPHL			13	5	22	5	18	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN74AS157, SN74AS158 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74AS157 SN74AS158			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−2	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74AS157 SN74AS158			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5	V
I_I	$\overline{A}$/B	V_{CC} = 5.5 V,	V_I = 7 V			0.2	mA
	A, B, or $\overline{G}$					0.1	
I_{IH}	$\overline{A}$/B	V_{CC} = 5.5 V,	V_I = 2.7 V			40	µA
	A, B, or $\overline{G}$					20	
I_{IL}	$\overline{A}$/B	V_{CC} = 5.5 V,	V_I = 0.4 V			−1	mA
	A, B, or $\overline{G}$					−0.5	
I_O*		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	'AS157	V_{CC} = 5.5 V			17.5	28	mA
	'AS158				15.6	22.5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
* The output conditions have been chosen to produce a current that closely approximates one half on the true short-circuit output current, I_{OS}.

'AS157 switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX		UNIT
			SN74AS157		
			MIN	MAX	
t_{PLH}	A or B	Y	1	6	ns
t_{PHL}			1	5.5	
t_{PLH}	$\overline{A}$/B	Y	2	11	ns
t_{PHL}			2	10	
t_{PLH}	$\overline{G}$	Y	2	10.5	ns
t_{PHL}			2	7.5	

'AS158 switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX		UNIT
			SN74AS158		
			MIN	MAX	
t_{PLH}	A or B	Y	1	5	ns
t_{PHL}			1	4.5	
t_{PLH}	$\overline{A}$/B	Y	2	9.5	ns
t_{PHL}			2	10.5	
t_{PLH}	$\overline{G}$	Y	2	6.5	ns
t_{PHL}			2	10	

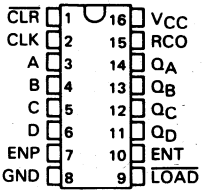
Note 2: Load circuit and voltage waveforms are shown in Section 1.

SYNCHRONOUS 4-BIT BINARY COUNTERS

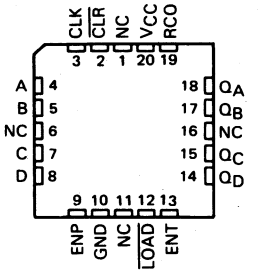
D2661, APRIL 1982 – REVISED MAY 1986

- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'ALS161B, 'ALS163B, 'AS161, and 'AS163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, they may be preset to any number between 0 and 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function for the 'AS161B and 'AS161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs.

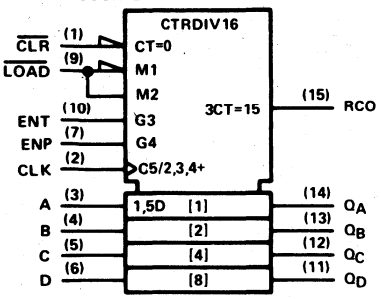
The clear function for the 'ALS163B and 'AS163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding in the Q outputs for the maximum count desired. The active-low output of the gate used for decoding in connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable input and a ripple carry output. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output. The ripple carry output (RCO) thus enabled will produce a high-level pulse while the count is maximum (15 with Q_A high). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

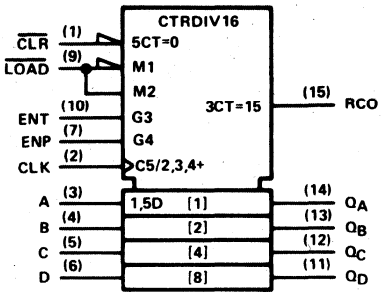
These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, of $\overline{\text{LOAD}}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

logic symbols†

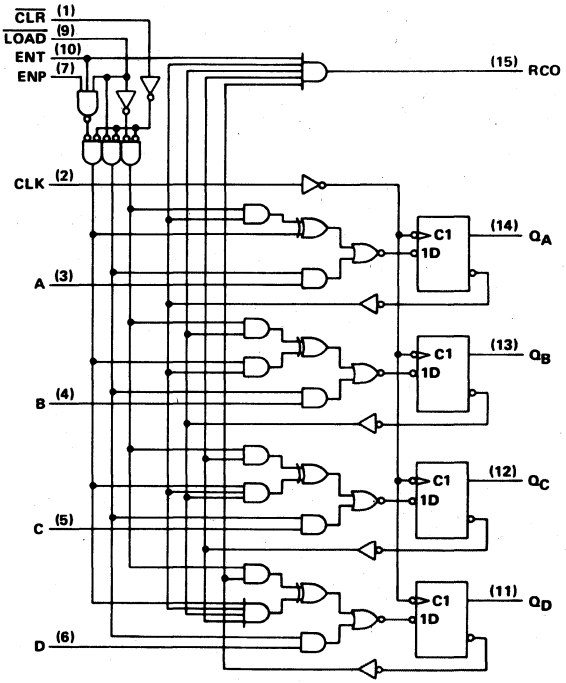
'ALS161B and 'AS161 BINARY COUNTERS WITH DIRECT CLEAR



'ALS163B AND 'AS163 BINARY COUNTERS WITH SYNCHRONOUS CLEAR



'ALS163B and 'AS163 logic diagram (positive logic)



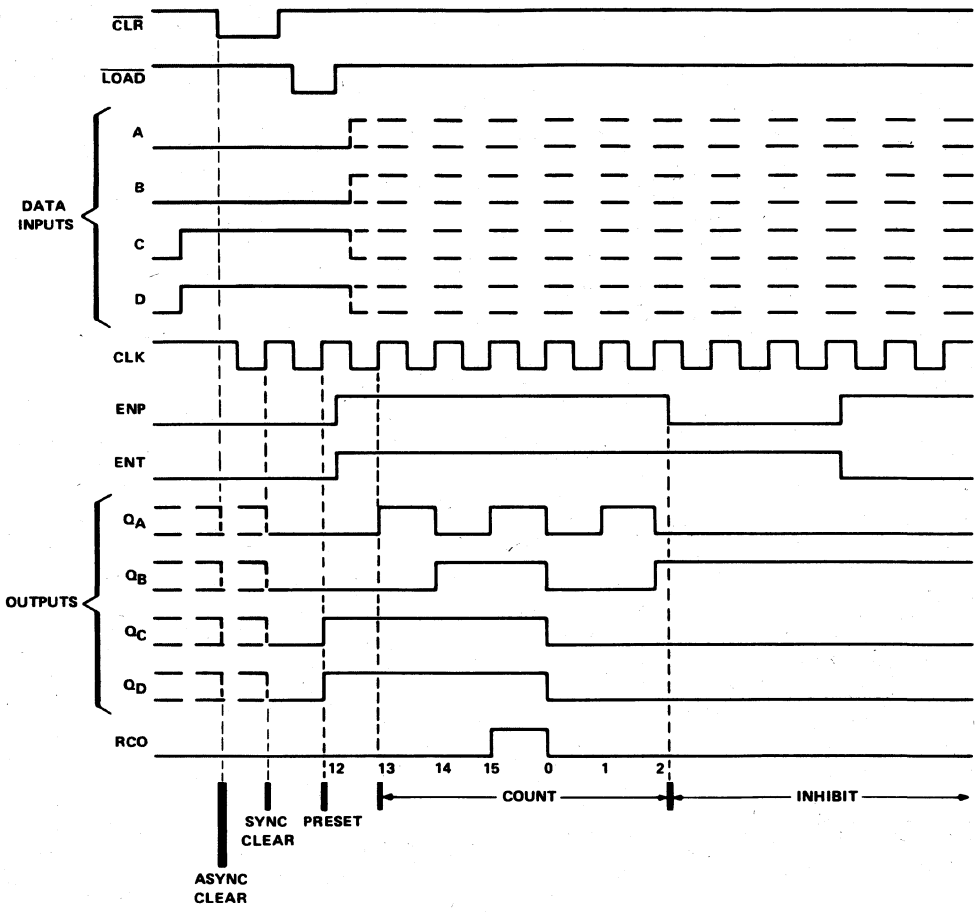
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.
'ALS161B and 'AS161 synchronous binary counters are similar; however the clear is asynchronous.

typical clear, preset, count, and inhibit sequences

'ALS161B, 'AS161, 'ALS163B, 'AS163

Illustrated below is the following sequence:

1. Clear outputs to zero ('ALS161B and 'AS161 are asynchronous; 'ALS163B and 'AS163 are synchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS161B, SN54ALS163B . . . . . −55°C to 125°C
SN74ALS161B, SN74ALS163B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54ALS161B SN54ALS163B			SN74ALS161B SN74ALS163B			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
I_{OH}	High-level output current					−0.4			−0.4	mA
I_{OL}	Low-level output current					4			8	mA
f_{clock}	Clock frequency			0		22	0		40	MHz
t_w	Pulse duration	CLK high or low		20			12.5			ns
		'ALS161B $\overline{CLR}$ low		20			15			
t_{su}	Setup time before CLK↑	A, B, C, D		20			15			ns
		$\overline{LOAD}$		20			15			
		ENP, ENT	'ALS161B	25			15			
			'ALS163B	20			15			
		'ALS161B	$\overline{CLR}$ inactive	10			10			
		'ALS163B	$\overline{CLR}$ low	20			15			
			$\overline{CLR}$ high (inactive)	10			10			
t_h	Hold time, all synchronous inputs after CLK↑			0			0			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS161B SN54ALS163B			SN74ALS161B SN74ALS163B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			12	21		12	21	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS161B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS161B		SN74ALS161B		
			MIN	MAX	MIN	MAX	
f_{max}			22		40		MHz
t_{PLH}	CLK	RCO	5	34	5	20	ns
t_{PHL}			5	27	5	20	
t_{PLH}	CLK	Any Q	4	19	4	15	ns
t_{PHL}			6	25	6	20	
t_{PLH}	ENT	RCO	3	18	3	13	ns
t_{PHL}			3	17	3	13	
t_{PHL}	$\overline{CLR}$	Any Q	8	27	8	24	ns
t_{PHL}	$\overline{CLR}$	RCO	11	32	11	23	ns

'ALS163B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS163B		SN74ALS163B		
			MIN	MAX	MIN	MAX	
f_{max}			35		40		MHz
t_{PLH}	CLK	RCO	5	25	5	20	ns
t_{PHL}			5	25	5	20	
t_{PLH}	CLK	Any Q	4	18	4	15	ns
t_{PHL}			6	25	6	20	
t_{PLH}	ENT	RCO	3	16	3	13	ns
t_{PHL}			3	16	3	13	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS161, SN54ALS163 . . . . . −55°C to 125°C
SN74ALS161, SN74ALS163 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54AS161 SN54AS163			SN74AS161 SN74AS163			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current					−2			−2	mA
I_{OL}	Low-level output current					20			20	mA
f_{clock}	Clock frequency			0		65	0		75	MHz
t_w	Pulse duration	CLK high or low		7.7			6.7			ns
		'AS161 $\overline{CLR}$ low		10			8			
t_{su}	Setup time before CLK↑	A, B, C, D		10			8			ns
		$\overline{LOAD}$		10			8			
		ENP, ENT		10			8			
		'AS161 $\overline{CLR}$ inactive		10			8			
		'AS163	$\overline{CLR}$ low	14			12			
			$\overline{CLR}$ high (inactive)	10			9			
t_h	Hold time, all synchronous inputs after CLK↑			2			0			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS161 SN54AS163			SN74AS161 SN74AS163			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I	$\overline{LOAD}$	V_{CC} = 5.5 V,	V_I = 7 V			0.3			0.3	mA
	ENT					0.2			0.2	
	All other					0.1			0.1	
I_{IH}	$\overline{LOAD}$	V_{CC} = 5.5 V,	V_I = 2.7 V			60			60	μA
	ENT					40			40	
	All other					20			20	
I_{IL}	$\overline{LOAD}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−1.5			−1.5	mA
	ENT					−1			−1	
	All other					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			35	53		35	53	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS161 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS161		SN74AS161		
			MIN	MAX	MIN	MAX	
f_{max}			65		75		MHz
t_{PHL}	CLK	RCO	2	14	2	12.5	ns
t_{PLH}		RCO (with $\overline{LOAD}$ high)	1	8.5	1	8	
t_{PLH}		RCO (with $\overline{LOAD}$ low)	3	17.5	3	16.5	
t_{PLH}	CLK	Any Q	1	7.5	1	7	ns
t_{PHL}			2	14	2	13	
t_{PLH}	ENT	RCO	1.5	10	1.5	9	ns
t_{PHL}			1	9.5	1	8.5	
t_{PHL}	$\overline{CLR}$	Any Q	2	14	2	13	ns
t_{PHL}	$\overline{CLR}$	RCO	2	14	2	12.5	ns

'AS163 switching characteristics (see Note 1)

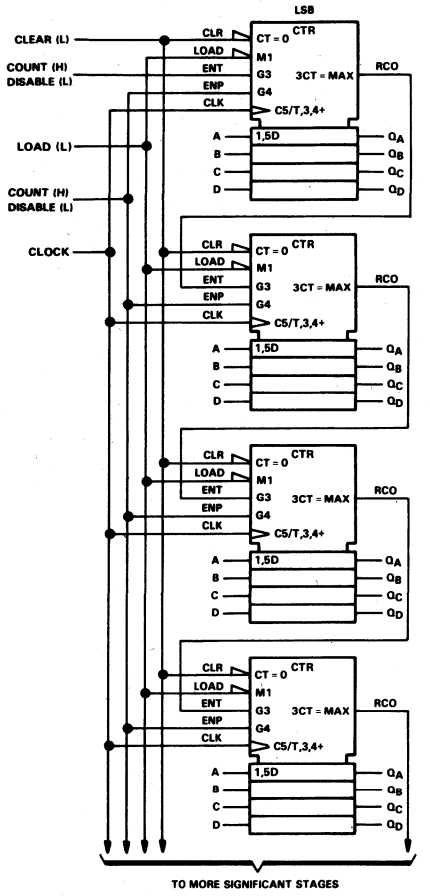
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS163		SN74AS163		
			MIN	MAX	MIN	MAX	
f_{max}			65		75		MHz
t_{PHL}	CLK	RCO	2	14	2	12.5	ns
t_{PLH}		RCO (with $\overline{LOAD}$ high)	1	8.5	1	8	
t_{PLH}		RCO (with $\overline{LOAD}$ low)	3	17.5	3	16.5	
t_{PLH}	CLK	Any Q	1	7.5	1	7	ns
t_{PHL}			2	14	2	13	
t_{PLH}	ENT	RCO	1.5	10	1.5	9	ns
t_{PHL}			1	9.5	1	8.5	

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

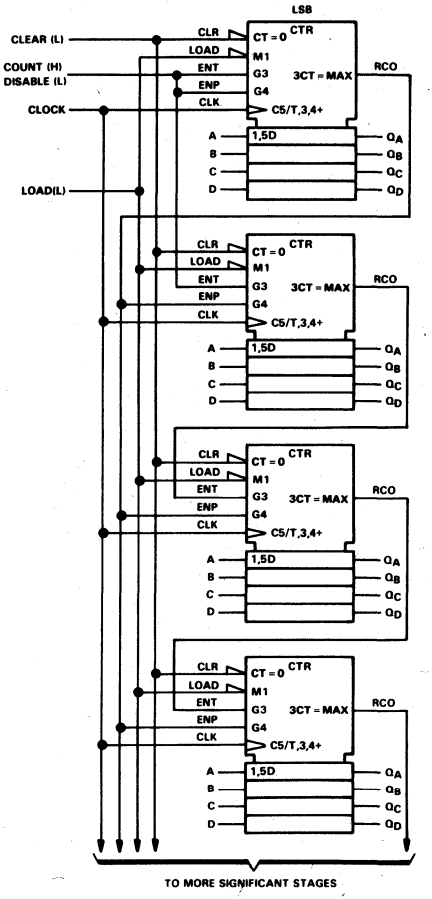
N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the ripple mode carry circuit (Figure 1) and the carry-look-ahead circuit (Figure 2) can be used to implement a high-speed N-bit counter. When additional stages are added, the f_{MAX} decreases in Figure 1, but remains unchanged in Figure 2.



$f_{MAX} = 1/(\text{CLK to RCO } t_{PLH}) + (\text{ENT to RCO } t_{PLH})(N-2) + (\text{ENT } t_{su})$

FIGURE 1



$f_{MAX} = 1/\text{CLK to RCO } t_{PLH}) + (\text{ENP } t_{su})$

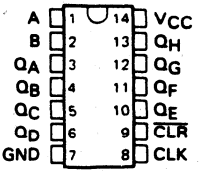
FIGURE 2

TEXAS INSTRUMENTS

D2661, APRIL 1982 – REVISED JANUARY 1989

- **AND-Gated (Enable/Disable) Serial Inputs**
- **Fully Buffered Clock and Serial Inputs**
- **Direct Clear**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS164 . . . D OR N PACKAGE
(TOP VIEW)

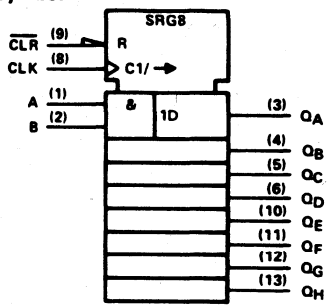


description

These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

The SN74ALS164 is characterized for operation from 0°C to 70°C.

logic symbol†



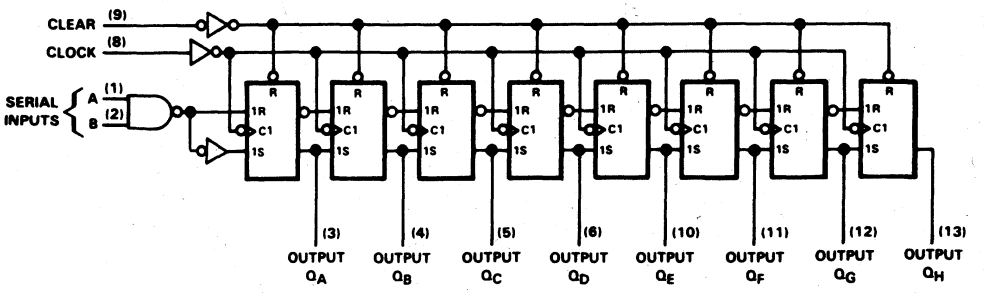
FUNCTION TABLE

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	Q_B . . . Q_H	
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

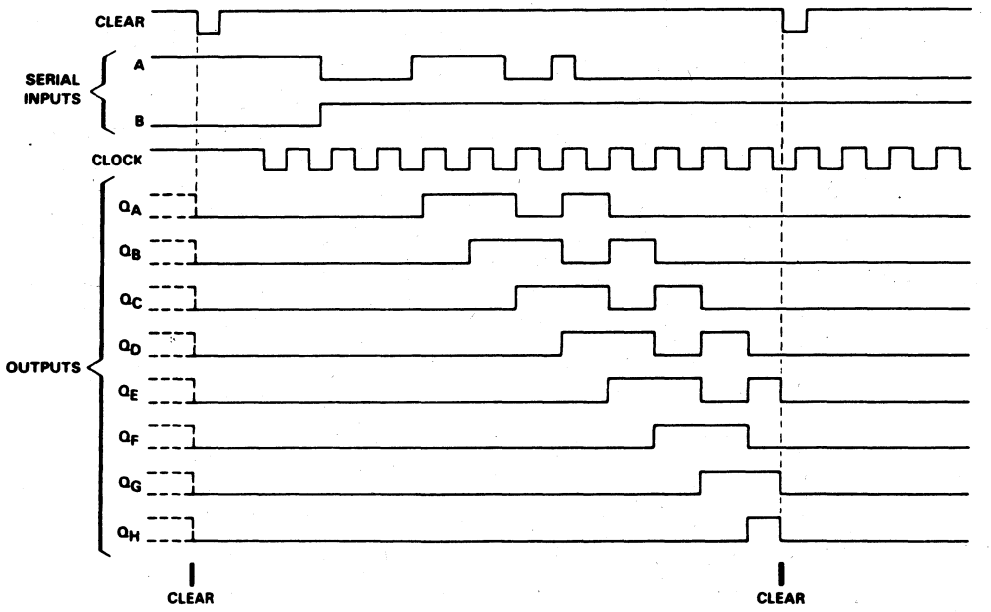
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

typical clear, shift, and clear sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN74ALS164 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN74ALS164			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				-0.4	mA
I_{OL}	Low-level output current				8	mA
f_{clock}	Clock frequency				50	MHz
t_w	Pulse duration	Clock	10			ns
		Clear low	16			
t_{su}	Setup time before CLK ↑	Data	6			ns
		$\overline{CLR}$ inactive	8			
t_h	Hold time, data after CLK↑		2			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS164			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = -18 mA			-1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = -0.4 mA	V_{CC}-2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			-0.1	mA
I_O*	V_{CC} = 5.5 V,	V_O = 2.25 V	-30		-112	mA
I_{CC}	V_{CC} = 5.5 V	See Note 1		14	24	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
* The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: With 4.5 V applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a clock transition from 0 V to 4.5 V.

switching characteristics (see Note 2)

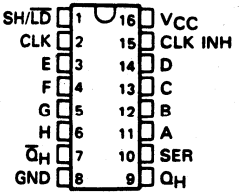
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX			UNIT
			SN74ALS164			
			MIN	TYP†	MAX	
f_{max}			50	75		MHz
t_{PHL}	$\overline{CLR}$	Any Q	6	15	20	ns
t_{PLH}	CLK	Any Q	6	9	16	ns
t_{PHL}			6	11	17	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

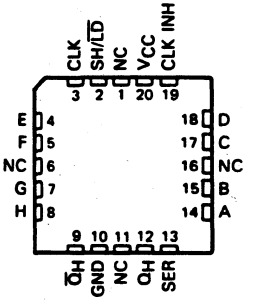
D2661, JUNE 1982 – REVISED SEPTEMBER 1988

- **Complementary Outputs**
- **Direct Overriding Load (Data) Inputs**
- **Gated Clock Inputs**
- **Parallel-to-Serial Data Conversion**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS165 ... J PACKAGE
SN74ALS165 ... D OR N PACKAGE
(TOP VIEW)



SN54ALS165 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'ALS165 is an 8-bit serial shift register that, when clocked, shifts the data toward serial outputs Q_H and $\overline{Q}_H$. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the SH/$\overline{LD}$ (Shift/$\overline{Load}$) input. The 'ALS165 also features a clock inhibit function and complemented serial outputs.

Clocking is accomplished by a low-to-high transition of the CLK input while SH/$\overline{LD}$ is held high and CLK INH (clock inhibit) is held low. The functions of the CLK and CLK INH inputs are interchangeable. Since a low CLK input and a low-to-high transition of CLK INH will also accomplish clocking, CLK INH should be changed to the high level only while the CLK input is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. The parallel inputs to the register are enabled while SH/$\overline{LD}$ is low independently of the levels of CLK, CLK INH, or SER inputs.

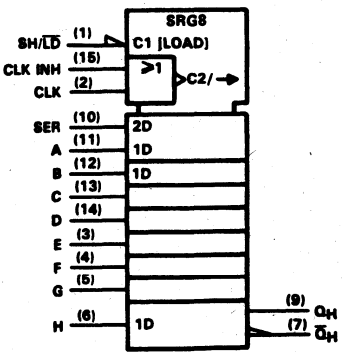
The SN54ALS165 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS165 is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

INPUTS			FUNCTION
SH/$\overline{LD}$	CLK	CLK INH	
L	X	X	PARALLEL LOAD
H	H	X	NO CHANGE
H	X	H	NO CHANGE
H	L	↑	SHIFT
H	↑	L	SHIFT

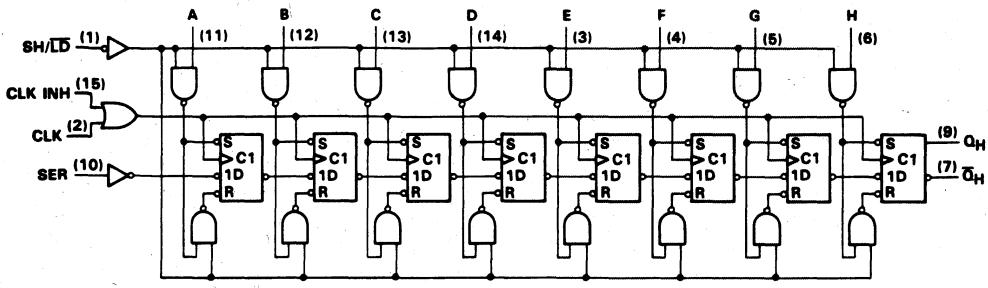
SHIFT – content of each internal register shifts toward serial outputs. Data at serial input is shifted into first register.

logic symbol†



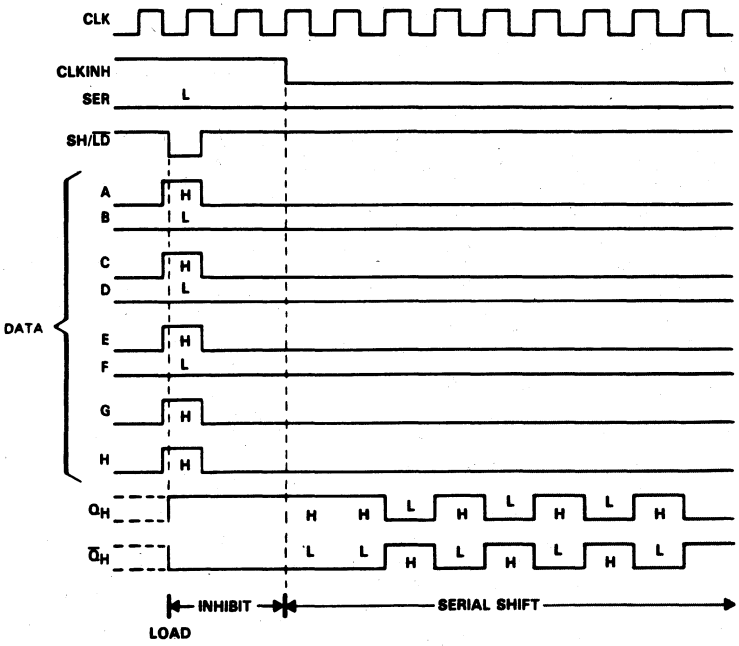
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

typical shift, load, and inhibit sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage ..... 7 V
Operating free-air temperature range: SN54ALS165 ..... −55 °C to 125 °C
SN74ALS165 ..... 0 °C to 70 °C
Storage temperature range ..... −65 °C to 150 °C

recommended operating conditions

			SN54ALS165			SN74ALS165			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		35	0		45	MHz
$t_{w(clock)}$	Duration of clock input pulse (see Figure 1)	clock high	14			11			ns
		clock low	14			11			
$t_{w(load)}$	Duration of load input pulse	clock low	15			12			ns
t_{su}	Clock-enable setup time (see Figure 1)		15			11			ns
t_{su}	Parallel input setup time (see Figure 1)		11			10			ns
t_{su}	Serial input setup time (see Figure 2)		11			10			ns
t_{su}	Shift setup time (see Figure 2)		15			10			ns
t_h	Hold time at any input		4			4			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS165			SN74ALS165			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O*	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		12	24		12	24	mA

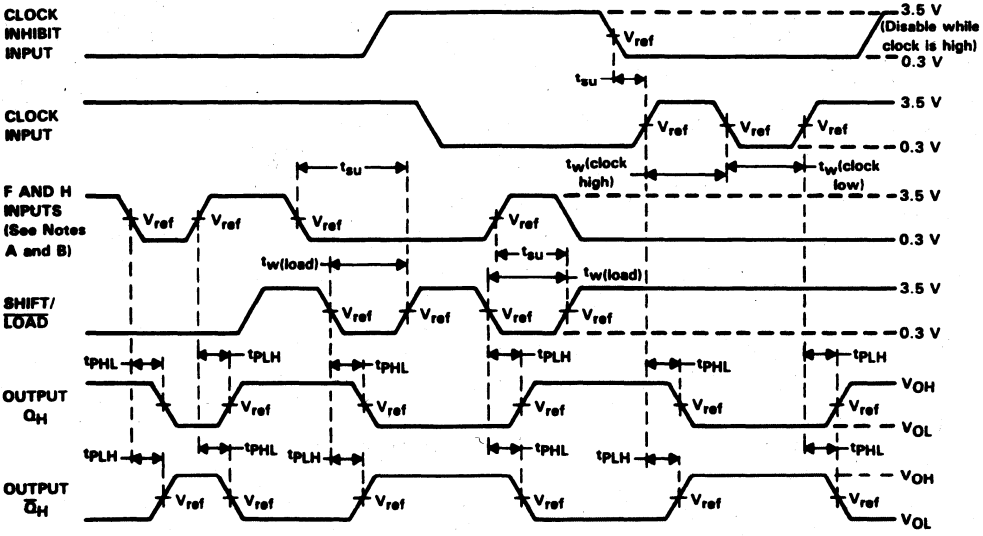
† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
* The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: With the outputs open, CLK INH and CLK at 4.5 V, and a clock pulse applied to the SH/$\overline{LD}$ input, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

switching characteristics (see Figures 1–3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS165			SN74ALS165			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			35			45			MHz
t_{PLH}	SH/$\overline{LD}$	Any	4		23	4		20	ns
t_{PHL}			4		23	4		22	
t_{PLH}	CLK	Any	3		14	3		13	ns
t_{PHL}			3		15	3		14	
t_{PLH}	H	Q_H	3		14	3		13	ns
t_{PHL}			3		18	3		16	
t_{PLH}	H	$\overline{Q}_H$	2		17	2		15	ns
t_{PHL}			3		17	3		16	

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.

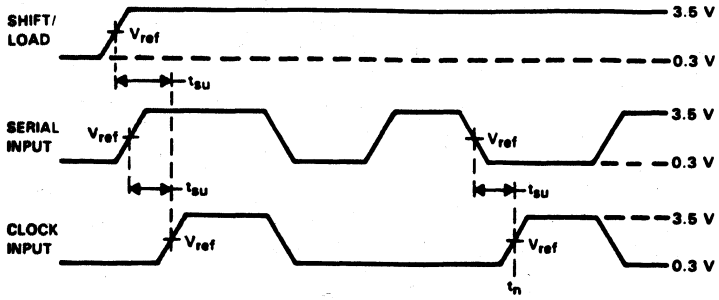
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The remaining six data inputs and the serial input are low.
B. Prior to test, high-level data is loaded into H input.
C. The input pulse generators have the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r = t_f = 2 ns.
D. V_{ref} = 1.3 V.

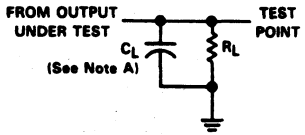
FIGURE 1. VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The eight data inputs and the clock-inhibit input are low. Results are monitored at output Q_H at t_n+7.
B. The input pulse generators have the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r = t_f = 2$ ns.
D. $V_{ref} = 1.3$ V.

FIGURE 2. VOLTAGE WAVEFORMS



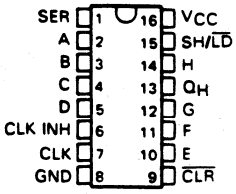
NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. LOAD CIRCUIT FOR SWITCHING TESTS

D2661, APRIL 1982 – REVISED OCTOBER 1988

- **Synchronous Load**
- **Direct Overriding Clear**
- **Parallel to Serial Conversion**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS166 . . . D OR N PACKAGE
(TOP VIEW)



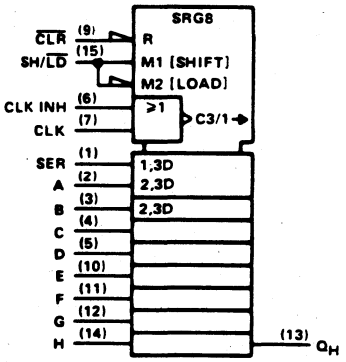
description

These 'ALS166 8-bit register is compatible with most other TTL logic families. All inputs are buffered to lower the drive requirements. Input clamping diodes minimize switching transients and simplify system design.

These parallel-in or serial-in, serial-out registers have a complexity of 77 equivalent gates on a monolithic chip. They feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the SH/$\overline{LD}$ input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the clock input. The clock-inhibit input should be changed to the high level only when the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

The SN74ALS166 is characterized for operation from 0°C to 70°C.

logic symbol†

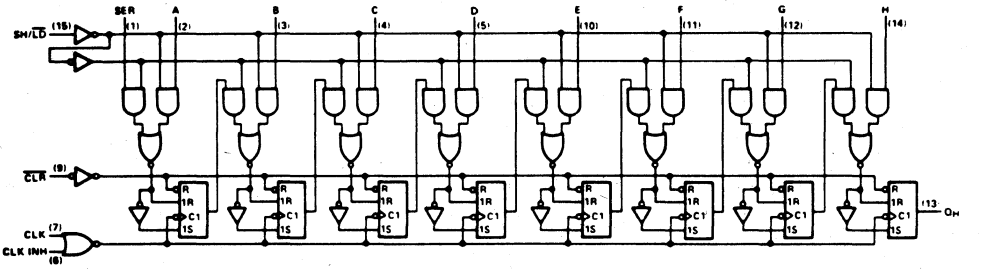


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D and N packages.

FUNCTION TABLE

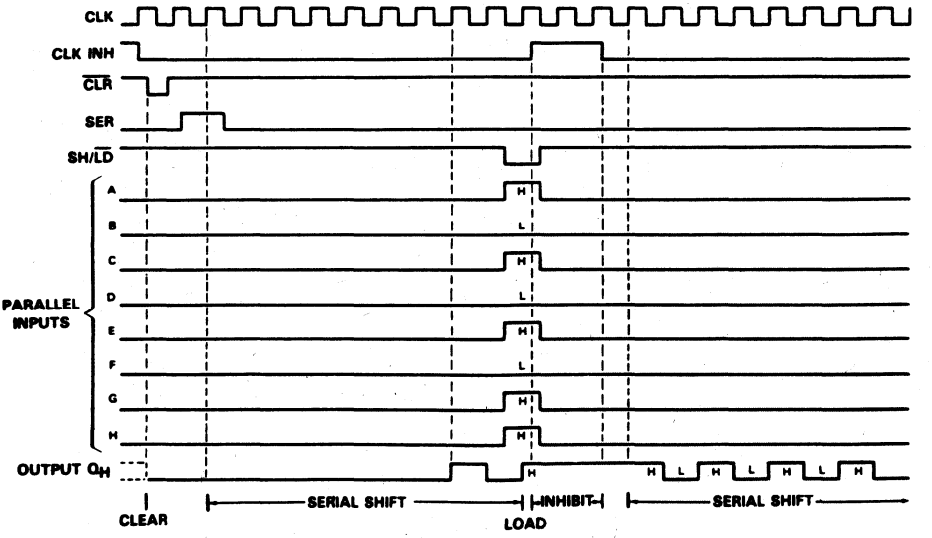
INPUTS						INTERNAL OUTPUTS		OUTPUT
$\overline{CLR}$	SH/$\overline{LD}$	CLK INH	CLK	SER	PARALLEL A ... H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a ... h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

logic diagram (positive logic)



Pin numbers are for D, J, and N packages.

typical clear, shift, load, inhibit, and shift sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN74ALS166 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operation conditions

			SN74ALS166			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−0.4	mA
I_{OL}	Low-level output current				8	mA
f_{clock}	Clock frequency				45	MHz
t_w	Pulse duration	$\overline{CLR}$ low	9			ns
		CLK high	10			
		CLK low	10			
t_{su}	Setup time before CLK↑	SH/$\overline{LD}$	16			ns
		Data	7			
		$\overline{CLR}$ inactive	11			
t_h	Hold time, data after CLK↑		3			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS166			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_O*	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	See Note 1		14	28	mA

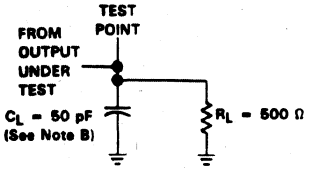
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
* The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: With 4.5 V applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a clock transition from 0 V to 4.5 V.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX			UNIT
			SN74ALS166			
			MIN	TYP†	MAX	
f_{max}			45			MHz
t_{PHL}	$\overline{CLR}$	Q_H	4	9	14	ns
t_{PLH}	CLK	Q_H	2	7	12	ns
t_{PHL}			2	9	13	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

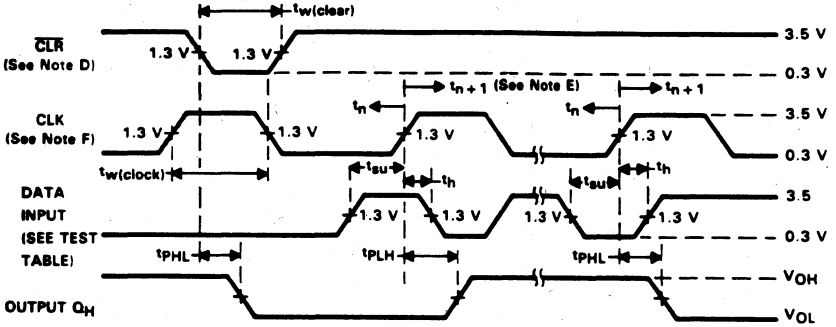
PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SH/$\overline{LD}$	OUTPUT TESTED (SEE NOTE C)
H	0 V	Q_H at t_{n+1}
Serial Input	4.5 V	Q_H at t_{n+8}



VOLTAGE WAVEFORMS

NOTES: A. All pulse generators have the following characteristics: $Z_{out} \approx 50\,\Omega$; $t_r = t_f = 2$ ns. Duty cycle = 50% when testing f_{max}.
B. C_L includes probe and jig capacitance.
C. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+8} with a functional test.
D. A clear pulse is applied prior to each test.
E. t_n = bit time before clocking transition, t_{n+1} = bit time after one clocking transition, and t_{n+8} = bit time after eight clocking transitions.
F. The clock pulse has the following characteristics: $t_{w(clock)} \leq 20$ ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(clear)} \leq 20$ ns.

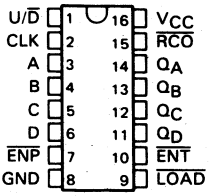
FIGURE 1

SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

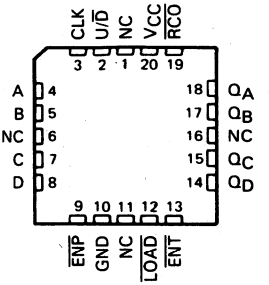
MARCH 1984, REVISED OCTOBER 1991

- **Fully Synchronous Operation for Counting and Programming**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Fully Independent Clock Circuit**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These synchronous, presettable 4-bit binary counters feature an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive going) edge of the clock input waveform.

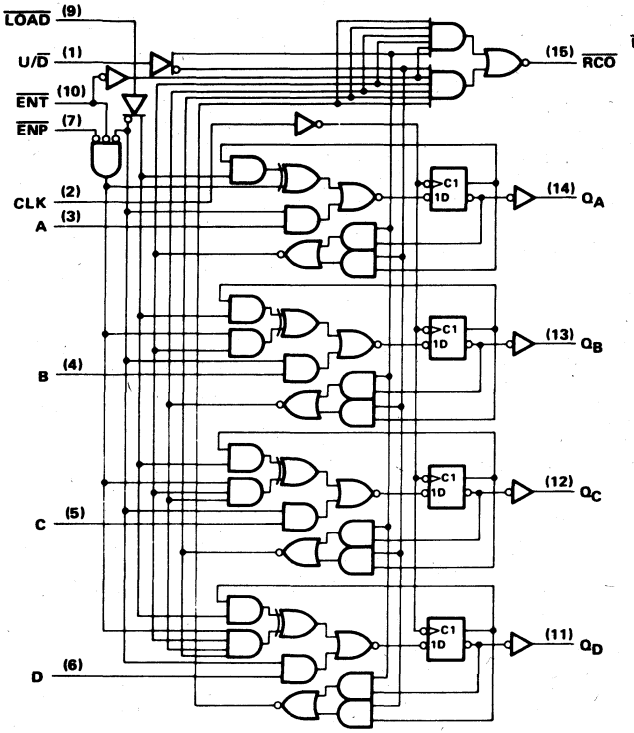
These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs ($\overline{ENP}$ and $\overline{ENT}$) must be low to count. The direction of the count is determined by the level of the U/$\overline{D}$ input. When U/$\overline{D}$ is high, the counter counts up; when low, it counts down. Input $\overline{ENT}$ is fed forward to enable the carry output. The ripple carry output ($\overline{RCO}$) thus enabled will produce a low-level pulse while the count is zero (all inputs low) counting down or maximum (15) counting up. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transistions at $\overline{ENP}$ or $\overline{ENT}$ are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

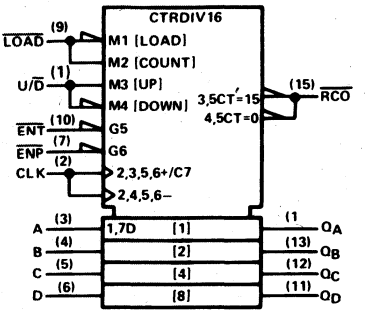
These counters feature a fully independent clock circuit. Changes at control inputs ($\overline{ENP}$, $\overline{ENT}$, $\overline{LOAD}$, U/$\overline{D}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The SN54ALS169B and SN54AS169A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS169B and SN74AS169A are characterized for operation from 0°C to 70°C.

'ALS169B, 'AS169A logic diagram (positive logic)



'ALS169B, 'AS169A logic symbol†

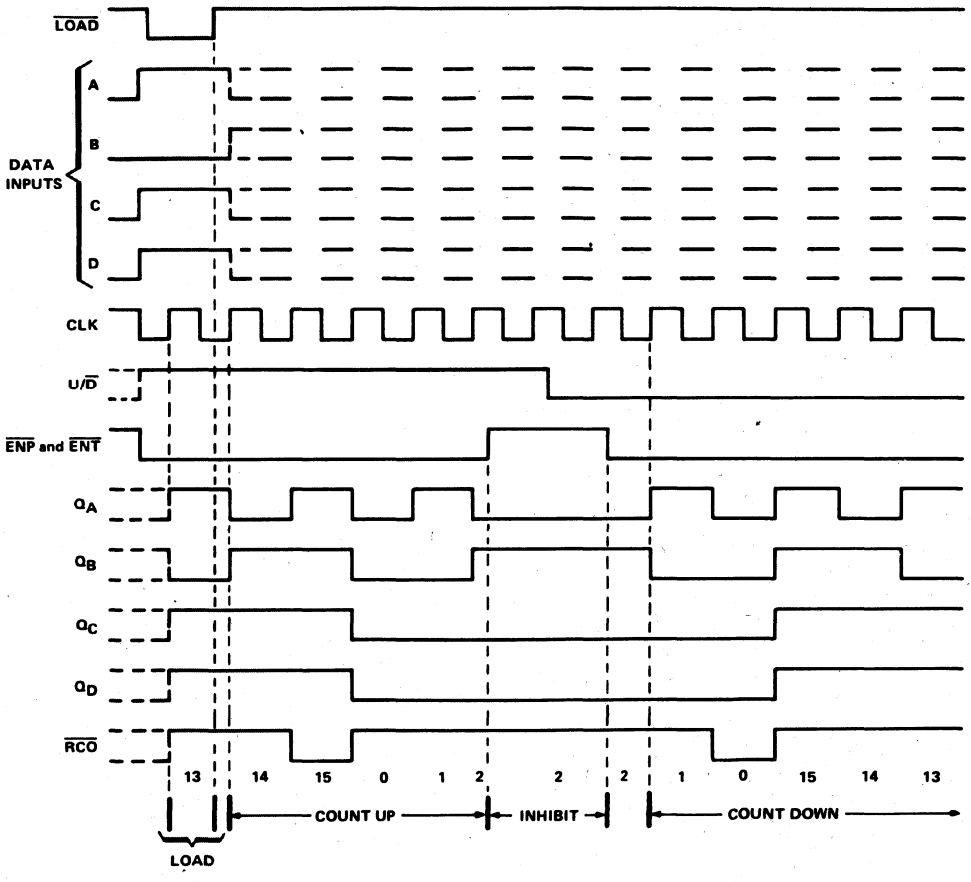


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

'ALS169B, 'AS169A typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS169B . . . . . −55°C to 125°C
SN74ALS169B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS169B			SN74ALS169B			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		22	0		40	MHz
t_w	Pulse duration	CLK high or low	14			12.5			ns
t_{su}	Setup time before CLK↑	A, B, C, or D	20			15			ns
		$\overline{ENP}$ or $\overline{ENT}$	25			15			
		$\overline{LOAD}$	20			15			
		U/$\overline{D}$	28			15			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS169B			SN74ALS169B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			15	25		15	25	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS169B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, RL = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS169B		SN74ALS169B		
			MIN	MAX	MIN	MAX	
f_{max}			22		40		MHz
t_{PLH}	CLK	$\overline{RCO}$	3	25	3	20	ns
t_{PHL}			6	25	6	20	
t_{PLH}	CLK	Any Q	2	20	2	15	ns
t_{PHL}			5	25	5	20	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	2	16	2	13	ns
t_{PHL}			3	19	3	16	
t_{PLH}	U/$\overline{D}$	$\overline{RCO}$	5	22	5	19	ns
t_{PHL}			5	22	5	19	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS169A . . . . . −55 °C to 125 °C
SN74AS169A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54AS169A			SN74AS169A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		65	0		75	MHz
t_w	Pulse duration	CLK high or low	7.7			6.7			ns
t_{su}	Setup time before CLK↑	A, B, C, or D	10			8			ns
		$\overline{ENP}$ or $\overline{ENT}$	10			8			
		$\overline{LOAD}$	10			8			
		U/$\overline{D}$	14			11			
t_h	Hold time, data after CLK↑		2			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS169A			SN74AS169A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I	$\overline{LOAD}$, $\overline{ENT}$, U/$\overline{D}$	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	$\overline{LOAD}$, $\overline{ENT}$, U/$\overline{D}$	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	$\overline{LOAD}$, $\overline{ENT}$, U/$\overline{D}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others,					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			41	63		41	63	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS169A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, RL = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS169A		SN74AS169A		
			MIN	MAX	MIN	MAX	
f_{max}			65		75		MHz
t_{PLH}	CLK	$\overline{RCO}$ ($\overline{LOAD}$ high or low)	3	17.5	3	16.5	ns
t_{PHL}			2	14	2	13	
t_{PLH}	CLK	Any Q	1	7.5	1	13	ns
t_{PHL}			2	14	2	13	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	1.5	10	1.5	9	ns
t_{PHL}			1.5	10	1.5	9	
t_{PLH}	U/$\overline{D}$	$\overline{RCO}$	2	14	2	12	ns
t_{PHL}			2	14.5	2	13	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

D2661, APRIL 1982 – REVISED MAY 1986

- **'ALS174 and 'AS174 Contain Six Flip-Flops with Single-Rail Outputs**
- **'ALS175 and 'AS175A Contain Four Flip-Flops with Double-Rail Outputs**
- **Buffered Clock and Direct Clear Inputs**
- **Applications Include:**
  Buffer/Storage Registers
  Shift Registers
  Pattern Generators
- **Fully Buffered Outputs for Maximum Isolation from External Disturbances ('AS only)**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input and the 'ALS175 and 'AS175A feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL circuits.

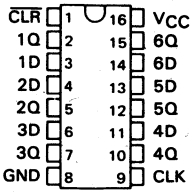
The SN54ALS174, SN54ALS175, SN54AS174, and SN54AS175A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS174, SN74ALS175, SN74AS174, and SN74AS175A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

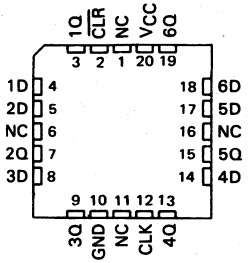
INPUTS			OUTPUTS	
$\overline{CLR}$	CLK	D	Q	$\overline{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

†'ALS175 and 'AS175A only

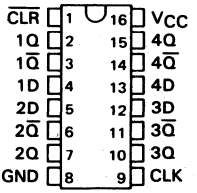
SN54ALS174, SN54AS174 . . . J PACKAGE
SN74ALS174, SN74AS174 . . . D OR N PACKAGE
(TOP VIEW)



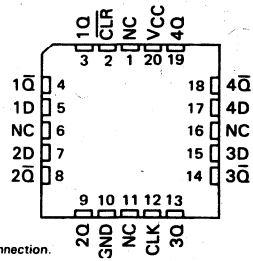
SN54ALS174, SN54AS174 . . . FK PACKAGE
(TOP VIEW)



SN54ALS175, SN54AS175A . . . J PACKAGE
SN74ALS175, SN74AS175A . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS175, SN54AS175A . . . FK PACKAGE
(TOP VIEW)

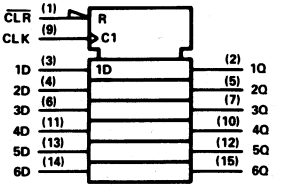


NC – No internal connection.

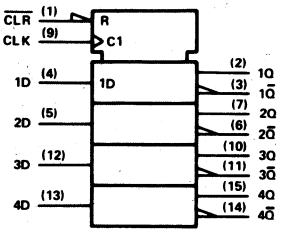
TEXAS INSTRUMENTS

logic symbols†

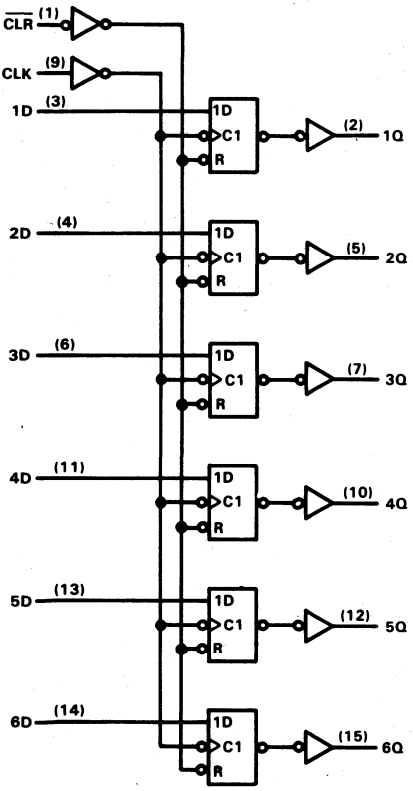
'ALS174, 'AS174

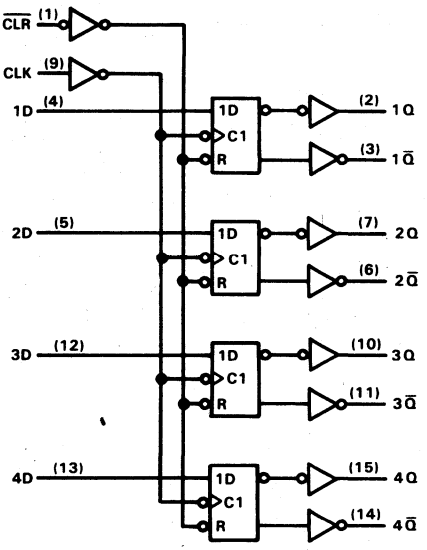


'ALS175, 'AS175A



logic diagrams (positive logic)





†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS174, SN54ALS175 . . . . . −55°C to 125°C
SN74ALS174, SN74ALS175 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS174 SN54ALS175			SN74ALS174 SN74ALS175			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		40	0		50	MHz
t_w	Pulse duration	$\overline{CLR}$ low	15			10			ns
		CLK high	12.5			10			
		CLK low	12.5			10			
t_{su}	Setup time before CLK↑	Data	15			10			ns
		$\overline{CLR}$ inactive	8			6			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS174 SN54ALS175			SN74ALS174 SN74ALS175			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS174	V_{CC} = 5.5 V,	See Note 1		11	19		11	19	mA
	'ALS175				8	14		9	14	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with D inputs and $\overline{CLR}$ grounded, and CLK at 4.5 V.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS174 SN54ALS175		SN74ALS174 SN74ALS175		
			MIN	MAX	MIN	MAX	
f_{max}			40		50		MHz
t_{PLH}	$\overline{CLR}$	Any $\overline{Q}$ ('ALS175)	5	20	5	18	ns
t_{PHL}		Any Q	8	30	8	23	
t_{PLH}	CLK	Any Q (or $\overline{Q}$, 'ALS175)	3	20	3	15	ns
t_{PHL}			5	24	5	17	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS174, SN54AS175A . . . . . −55°C to 125°C
SN74AS174, SN74AS175A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54AS174 SN54AS175A			SN74AS174 SN74AS175A			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current					−2			−2	mA
I_{OL}	Low-level output current					20			20	mA
f_{clock}	Clock frequency			0		100	0		100	MHz
t_w	Pulse duration	$\overline{CLR}$ low		5.5			5			ns
		CLK high		4			4			
		CLK low	'AS174	6			6			
			'AS175A	5			5			
t_{su}	Setup time before CLK↑	Data	'AS174	4			4			ns
			'AS175A	3			3			
		$\overline{CLR}$ inactive		6			6			
t_h	Hold time, data after CLK↑			1			1			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS174 SN54AS175A			SN74AS174 SN74AS175A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS174	V_{CC} = 5.5 V,	See Note 1		30	45		30	45	mA
	'AS175				22.5	34		22.5	34	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with D inputs and $\overline{CLR}$ grounded, and CLK at 4.5 V.

'AS174 switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS174		SN74AS174		
			MIN	MAX	MIN	MAX	
f_{max}			100		100		MHz
t_{PHL}	$\overline{CLR}$	Any Q	5	15	5	14	ns
t_{PLH}	CLK	Any Q	3.5	9.5	3.5	8	ns
t_{PHL}			4.5	11.5	4.5	10	

'AS175A switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS175A		SN74AS175A		
			MIN	MAX	MIN	MAX	
f_{max}			100		100		MHz
t_{PLH}	$\overline{CLR}$	Any Q or $\overline{Q}$	4	10	4	9	ns
t_{PHL}			4.5	15	4.5	13	
t_{PLH}	CLK	Any Q or $\overline{Q}$	4	8.5	4	7.5	ns
t_{PHL}			4	11	4	10	

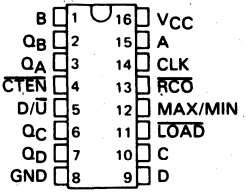
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

SN74ALS191, SN54ALS191
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

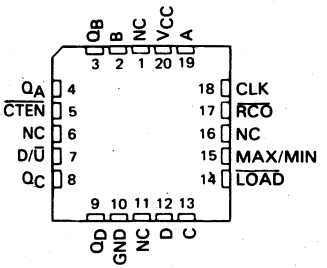
D2661, DECEMBER 1982 – REVISED MAY 1986

- **Single Down/Up Count Control Line**
- **Look-Ahead Circuitry Enhances Speed of Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Asynchronously Presettable with Load Control**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS191 . . . J PACKAGE
SN74ALS191 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS191 . . . FK PACKAGE
(TOP VIEW)



NC – no internal connection.

descriptions

The 'ALS191 is a synchronous, reversible, 4-bit binary up/down counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input ($\overline{CTEN}$) is low. A high at $\overline{CTEN}$ inhibits counting. The direction of the count is determined by the level of the down/up ($D/\overline{U}$) input. When $D/\overline{U}$ is low, the counter counts up and when $D/\overline{U}$ is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs ($\overline{CTEN}$ and $D/\overline{U}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

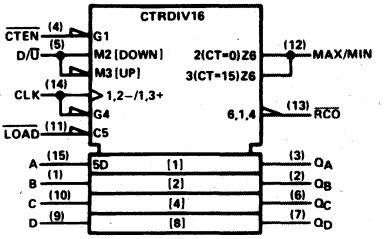
These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The CLK, $D/\overline{U}$, and LOAD inputs are buffered to lower the drive requirement, which significantly reduces the loading on, or current required by, clock drivers, etc., for long parallel words.

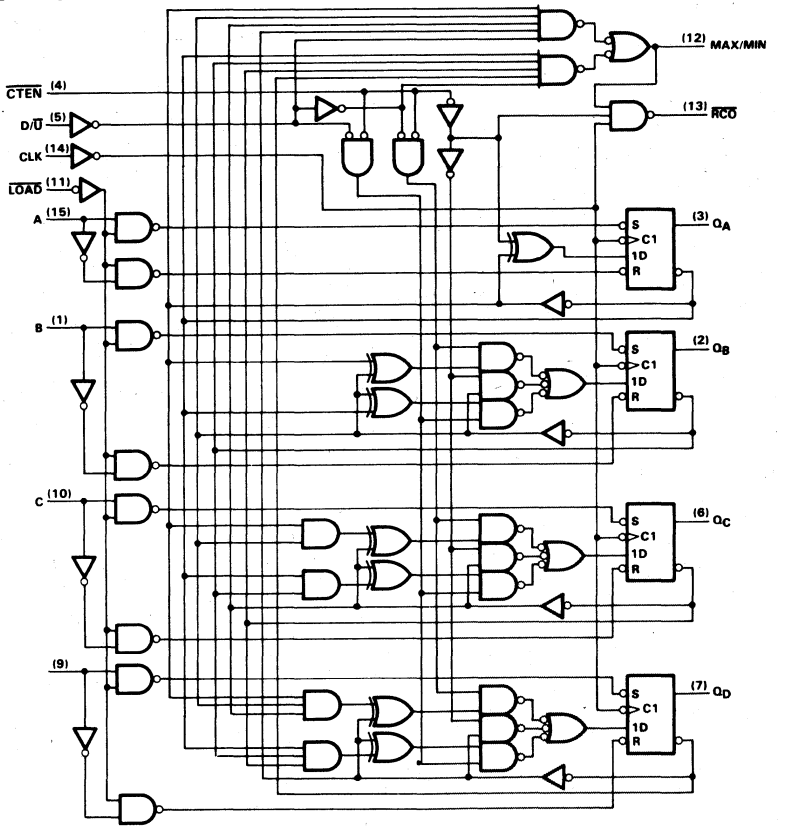
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock input is low. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

The SN54ALS191 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS191 is characterized for operation from 0°C to 70°C.

'ALS191 logic symbol†



'ALS191 logic diagram (positive logic)



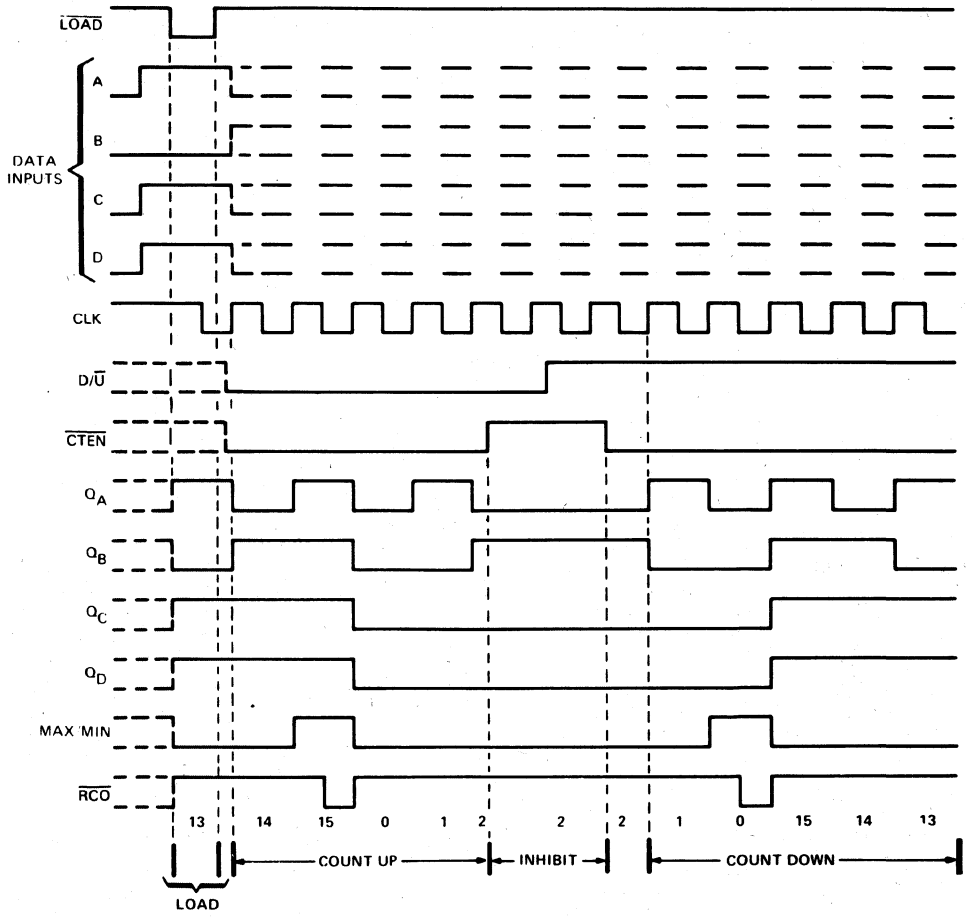
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

typical load, count, and inhibit sequences

'ALS191

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS191 . . . . . −55°C to 125°C
SN74ALS191 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS191			SN74ALS191			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		20	0		30	MHz
t_w	Pulse duration	CLK high or low	20			16.5			ns
		$\overline{LOAD}$ low	25			20			
t_{su}	Setup time	Data before $\overline{LOAD}$↑	25			20			ns
		$\overline{CTEN}$ before CLK↑	45			20			
		D/$\overline{U}$ before CLK↑	45			20			
		$\overline{LOAD}$ inactive before CLK↑	20			20			
t_h	Hold time	Data after $\overline{LOAD}$↑	5			5			ns
		$\overline{CTEN}$ after CLK↑	0			0			
		D/$\overline{U}$ after CLK↑	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS191			SN74ALS191			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	$\overline{CTEN}$ or CLK	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	All others					−0.1			−0.1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	All inputs at 0 V		12	22		12	22	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS191		SN74ALS191		
			MIN	MAX	MIN	MAX	
f_{max}			20		30		MHz
t_{PLH}	$\overline{LOAD}$	Any Q	7	37	8	30	ns
t_{PHL}			8	34	8	30	
t_{PLH}	A, B, C, D	Any Q	4	25	4	21	ns
t_{PHL}			4	25	4	21	
t_{PLH}	CLK	$\overline{RCO}$	5	24	5	20	ns
t_{PHL}			5	25	5	20	
t_{PLH}	CLK	Any Q	3	26	3	18	ns
t_{PHL}			3	22	3	18	
t_{PLH}	CLK	MAX/MIN	8	37	8	31	ns
t_{PHL}			8	34	8	31	
t_{PLH}	D/$\overline{U}$	$\overline{RCO}$	12	45	15	37	ns
t_{PHL}			10	36	10	28	
t_{PLH}	D/$\overline{U}$	MAX/MIN	8	35	8	25	ns
t_{PHL}			8	30	8	25	
t_{PLH}	$\overline{CTEN}$	$\overline{RCO}$	4	21	4	18	ns
t_{PHL}			4	23	4	18	

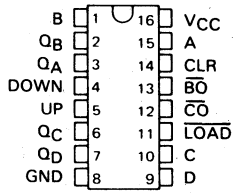
Note 1: Load circuit and voltage waveforms are shown in Section 1.

SN74ALS193, SN54ALS193
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

D2661, DECEMBER 1982 – REVISED MAY 1986

- Look-Ahead Circuitry Enhances Cascaded Counters
- Fully Synchronous in Count Modes
- Parallel Asynchronous Load for Modulo-N Count Lengths
- Asynchronous Clear
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54AS193 . . . J PACKAGE
SN74ALS193 . . . D OR N PACKAGE
(TOP VIEW)



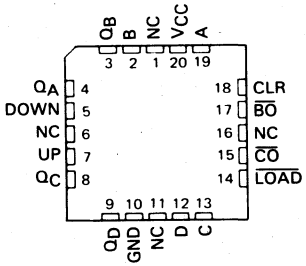
description

The 'ALS193 is a synchronous, reversible, 4-bit binary up/down counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggerd by a low-to-high-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

SN54ALS192, SN54ALS193 . . . FK PACKAGE
(TOP VIEW)



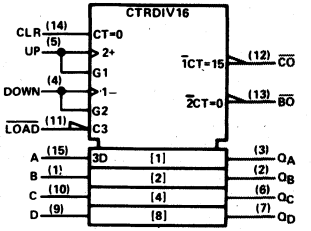
NC – no internal connection.

A clear has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs. The clock, count, and load inputs are buffered to lower the drive requirements. This significantly reduces the loading on clock drivers, etc., for long parallel words.

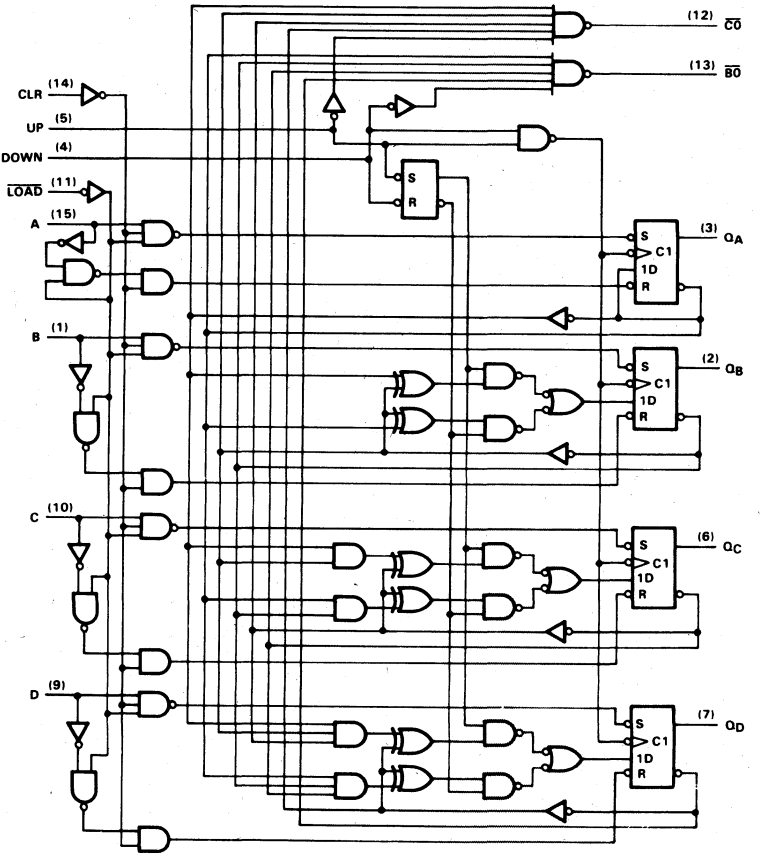
These counters were designed to be cascaded without the need for external circuitry. The bottow output (BO) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output ($\overline{CO}$) produces a low-level pulse while the count is maximum (15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

The SN54ALS193 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS193 is characterized for operation form 0°C to 70°C.

'ALS193 logic symbol†



'ALS193 logic diagrams (positive logic)



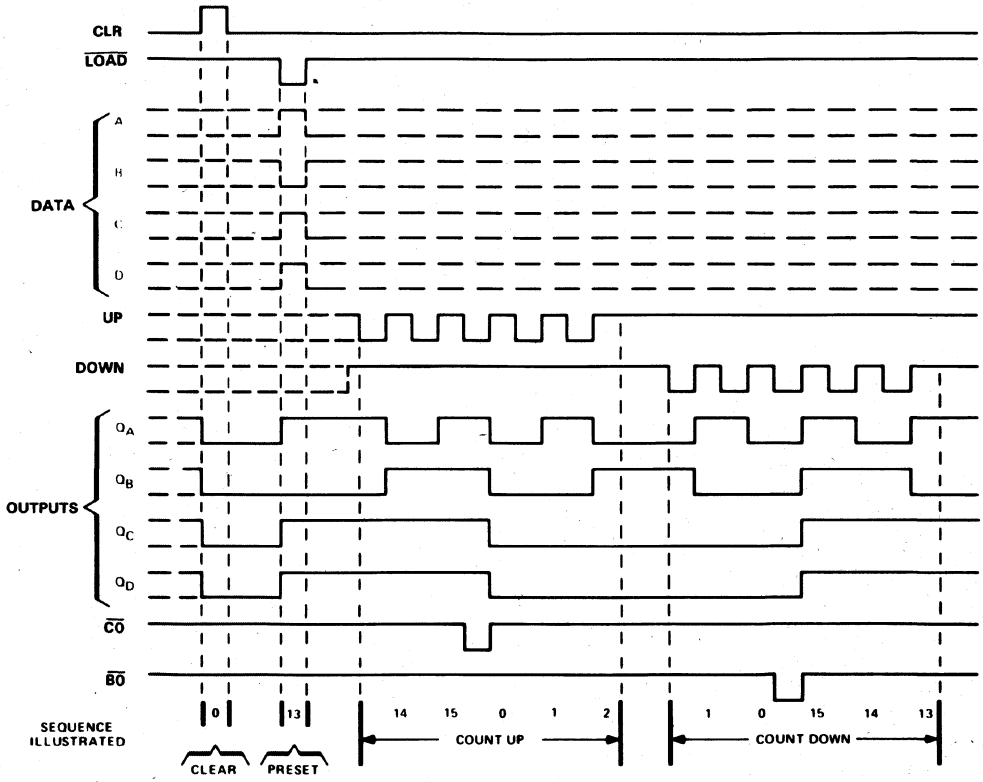
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

typical clear, load, and count sequences

'ALS193

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS193 . . . . . −55°C to 125°C
SN74ALS193. . . . . .0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS193			SN74ALS193			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		20	0		30	MHz
t_w	Pulse duration	CLR high	10			10			ns
		$\overline{LOAD}$ low	25			20			
		UP or DOWN high or low	30			16.5			
t_{su}	Setup time	Data before $\overline{LOAD}$↑	25			20			ns
		CLR inactive before UP↑ or DOWN↑	20			20			
		$\overline{LOAD}$ inactive before UP↑ or DOWN↑	20			20			
		UP high before DOWN↑	17			17			
		DOWN high before UP↑	15			15			
t_h	Hold time	Data after $\overline{LOAD}$↑	5			5			ns
		Up high after DOWN↑	5			5			
		DOWN high after UP↑	8			8			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS193			SN74ALS193			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	UP, DOWN	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	All others					−0.1			−0.1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		12	22		12	22	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with the clear and load inputs grounded, and all other inputs at 4.5 V.

switching characteristics (see Note 2)

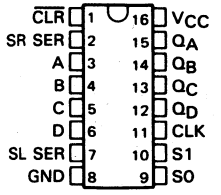
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS193		SN74ALS193		
			MIN	MAX	MIN	MAX	
f_{max}			25		30		MHz
t_{PLH}	UP	CO	3	20	4	16	ns
t_{PHL}			3	21	5	18	
t_{PLH}	Down	BO	4	20	4	16	ns
t_{PHL}			5	22	5	18	
t_{PLH}	Up or DOWN	Any Q	4	27	4	19	ns
t_{PHL}			4	23	4	17	
t_{PLH}	$\overline{LOAD}$	Any Q	8	38	8	30	ns
t_{PHL}			8	37	8	28	
t_{PHL}	CLR	Any Q	5	20	5	17	ns

Note 2: Load circuit and voltage waveforms are shown in Section 1.

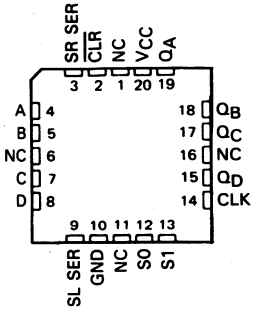
D2661, DECEMBER 1983 – REVISED MAY 1986

- **Parallel-to-Serial, Serial-to-Parallel Conversions**
- **Left or Right Shifts**
- **Parallel Synchronous Loading**
- **Direct Overriding Clear**
- **Temporary Data Latching Capability**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS194 . . . J PACKAGE
SN74AS194 . . . D OR N PACKAGE
(TOP VIEW)



SN54AS194 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These bidirectional shift registers feature parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Inhibit clock (temporary data latch/do nothing)
Shift-right (in the direction Q_A toward Q_D)
Shift-left (in the direction Q_D toward Q_A)
Parallel (broadside) load

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift-right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial inputs. Clocking of the flip-flop is inhibited when both mode control inputs are low.

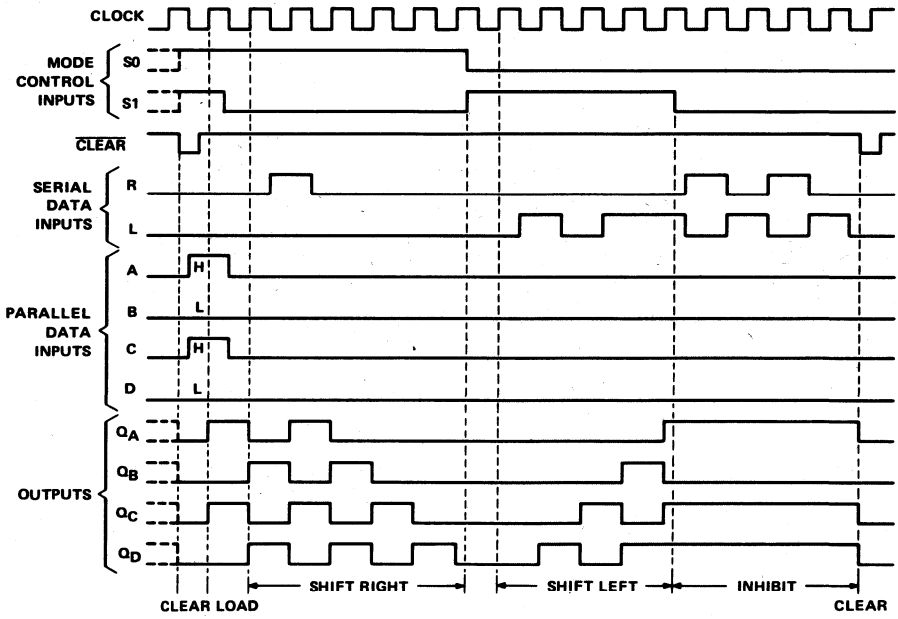
The SN54AS194 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS194 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS										OUTPUTS			
$\overline{\text{CLEAR}}$	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

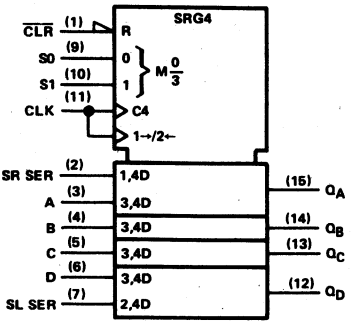
H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

typical clear, load, right-shift, inhibit, and clear sequences

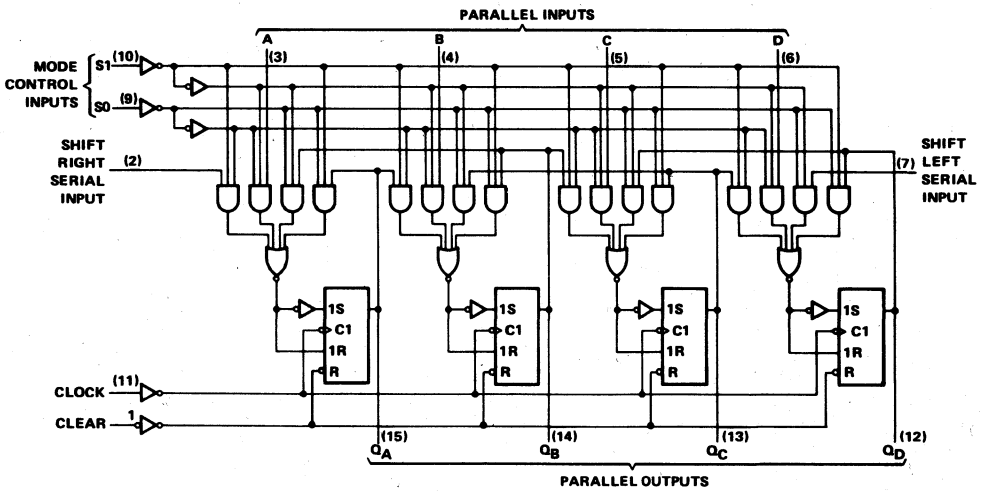


TEXAS INSTRUMENTS

logic symbol†



logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS194 . . . . . −55°C to 125°C
SN74AS194 . . . . . 0°C to 150°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS194			SN74AS194			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		75	0		80	MHz
t_w	Pulse duration	$\overline{CLR}$	4			4			ns
		CLK high	4			2			
		CLK low	6			6			
t_{su}	Set-up time before CLK↑	Select	9			8			ns
		Data	3.5			3			
t_{wr}	Recovery time	$\overline{CLR}$	6			6			ns
t_h	Hold time, data after CLK↑		0.5			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS194			SN74AS194			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	Data, CLK, $\overline{CLR}$	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	Mode, SL, SR					0.2			0.2	
I_{IH}	Data, CLK, $\overline{CLR}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	Mode, SL,SR					40			40	
I_{IL}	Data, CLK, $\overline{CLR}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	Mode, SL, SR					−1			−1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	Outputs high		30	49		30	43	mA
			Outputs low		38	60		38	53	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS194		SN74AS194		
			MIN	MAX	MIN	MAX	
f_{max}			75		80		MHz
t_{PLH}	CLK	Any Q	2.5	8	3	7	ns
t_{PHL}			2.5	8	3	7	
t_{PHL}	$\overline{CLR}$	Any Q	3.5	13	4	12	ns

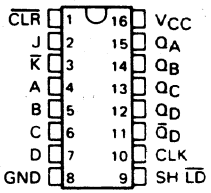
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN74AS195
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

D2661, DECEMBER 1983 – REVISED AUGUST 1987

- **Parallel-to-Serial, Serial-to-Parallel Conversions**
- **Parallel Synchronous Loading**
- **J and $\overline{K}$ Inputs to First Stage**
- **Right-Shift Only with Complementary Outputs on Last Stage**
- **Direct Overriding Clear**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74AS195 . . . D OR N PACKAGE
(TOP VIEW)



description

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation:

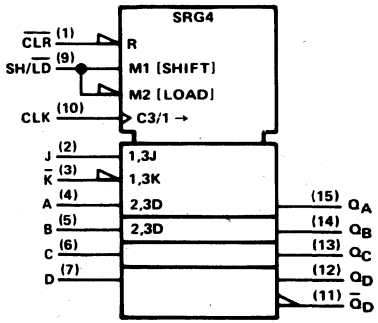
Parallel (broadside) load
Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift load control input low. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the function table.

The SN74AS195 is characterized for operation from 0°C to 70°C.

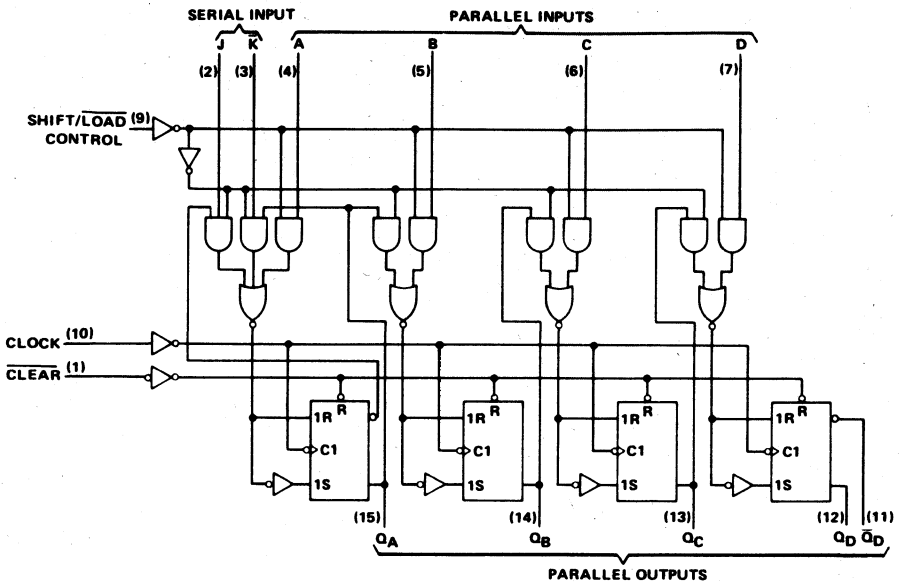
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D and N packages.

TEXAS INSTRUMENTS

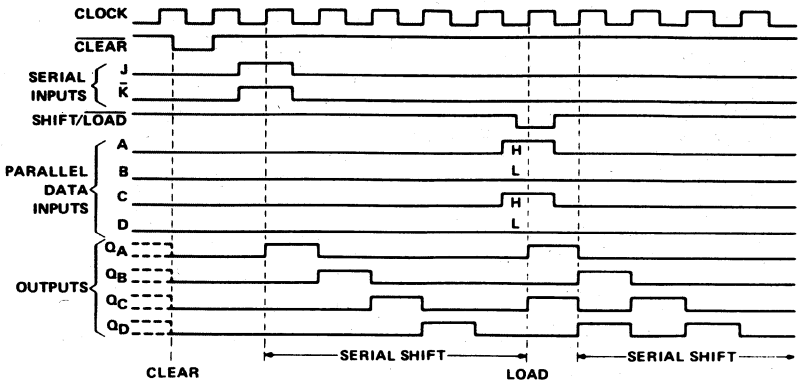
logic diagram (positive logic)



FUNCTION TABLE

INPUTS									OUTPUTS				
CLEAR	SHIFT/LOAD	CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

typical clear, shift, and load sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN74AS195 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN74AS195			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				20	mA
f_{clock}	Clock frequency		0		70	MHz
t_w	Pulse duration	CLK high	4			ns
		$\overline{CLR}$ low	4			
t_{su}	Setup time	Data before CLK↑	3.5			ns
		SH/$\overline{LD}$ before CLK↑	8			
		$\overline{CLR}$ high before CLK↑	6			
t_h	Hold time	Data after CLK↑	0.5			ns
		SH/$\overline{LD}$ after CLK↑	0			
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74AS195			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5	V
I_I	SH/$\overline{LD}$	V_{CC} = 5.5 V,	V_I = 7 V			0.2	mA
	All others					0.1	
I_{IH}	SH/$\overline{LD}$	V_{CC} = 5.5 V,	V_I = 2.7 V			40	μA
	All others					20	
I_{IL}	SH/$\overline{LD}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−1	mA
	All others					−0.5	
I_O*		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CCH}		V_{CC} = 5.5 V,			32	51	mA
I_{CCL}		V_{CC} = 5.5 V			36	57	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
* The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

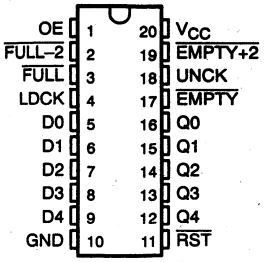
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX		UNIT
			SN74AS195		
			MIN	MAX	
f_{max}			70		MHz
t_{PLH}	CLK	Any Q	3	8.5	ns
t_{PHL}			2.5	10.5	
t_{PLH}	$\overline{CLR}$	$\overline{Q}_D$	4	8	ns
t_{PHL}		Q_A thru Q_D	5	11.5	

Note 1: Load circuit and voltage waveforms are shown in Section 1.

D3486, MARCH 1990

- **Independent Asychronous Inputs and Outputs**
- **16 Words by 5 Bits Each**
- **Data Rates From 0 to 40 MHz**
- **Fall-Through Time . . . 14 ns Typ**
- **3-State Outputs**

DW OR N PACKAGE
(TOP VIEW)



description

These 80-bit memories use Advanced Low-Power Schottky technology and feature high speed and fast fall-through times. They are organized as 16 words by 5 bits each.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

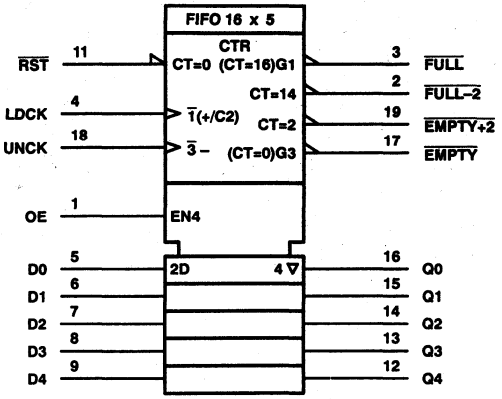
Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals will have no effect. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$, $\overline{\text{FULL–2}}$, and $\overline{\text{FULL+2}}$ output flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when it is not full. The $\overline{\text{FULL–2}}$ output is low when the memory contains 14 data words. The $\overline{\text{EMPTY}}$ output is low when the memory is empty and high when it is not empty. The $\overline{\text{EMPTY+2}}$ output is low when two words remain in memory.

A low level on the reset input ($\overline{\text{RST}}$) resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and sets $\overline{\text{FULL}}$, $\overline{\text{FULL–2}}$, and $\overline{\text{EMPTY+2}}$ high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK, after either a $\overline{\text{RST}}$ pulse or from an empty condition, causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable input (OE) is low. OE does not affect the output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

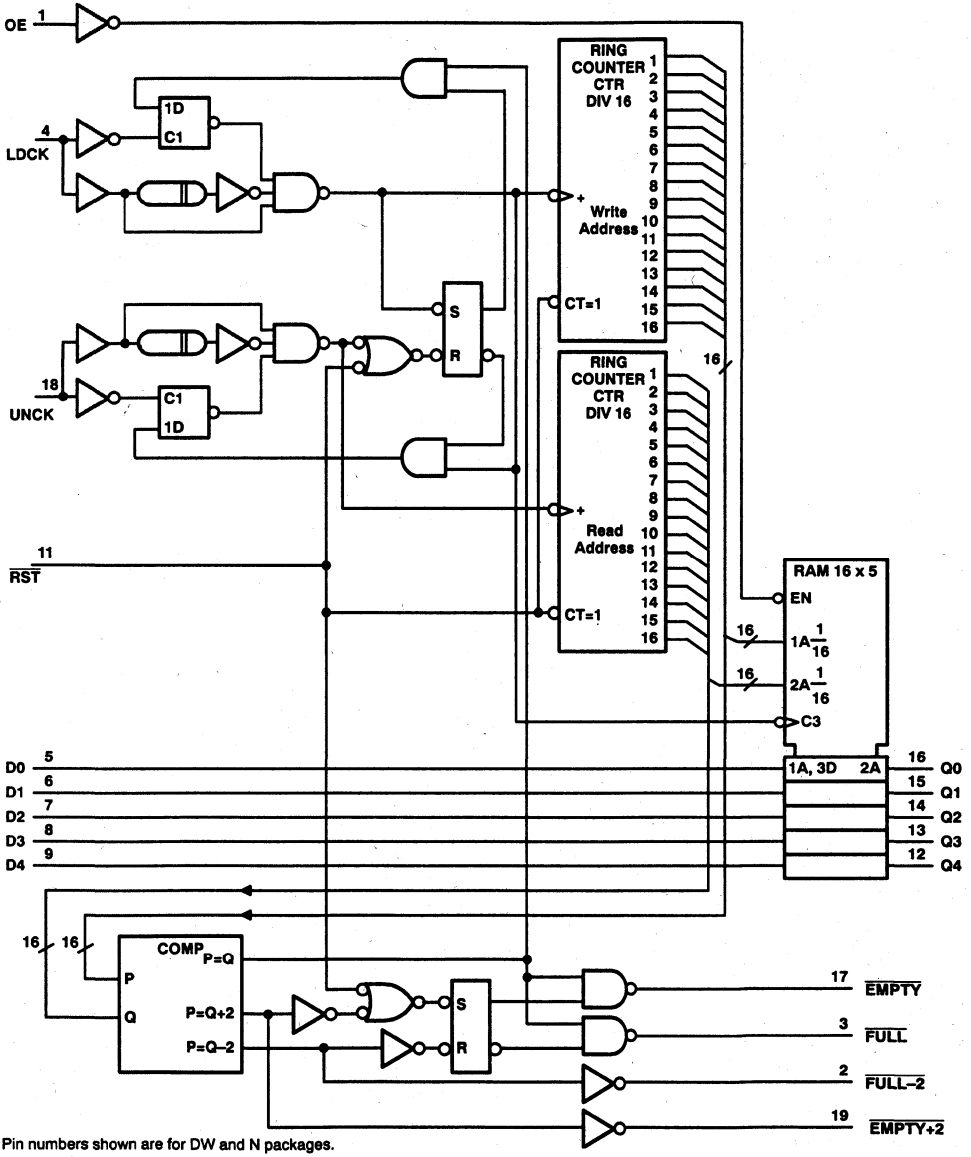
The SN74ALS229B is characterized for operation from 0°C to 70°C.

logic symbol†



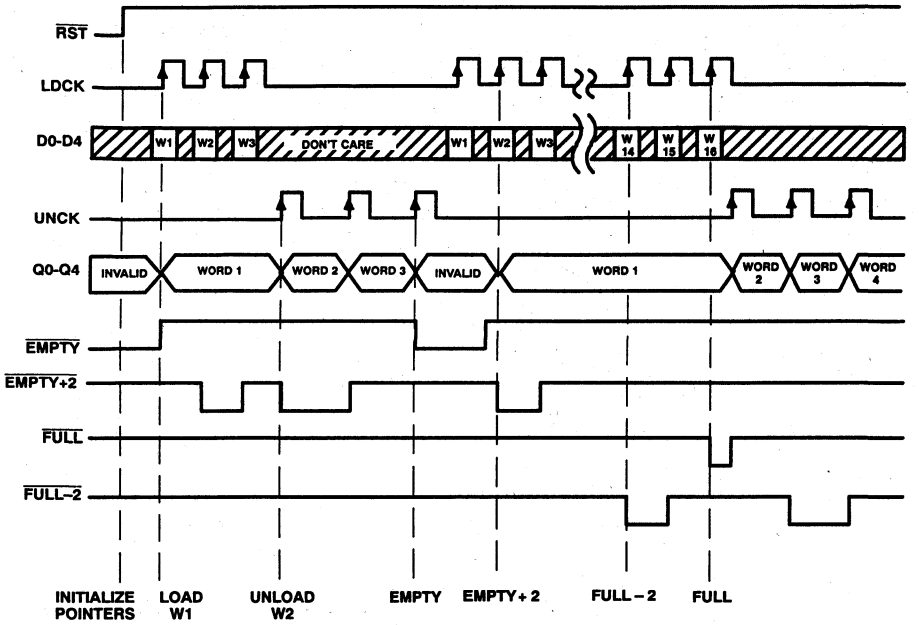
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.
Pin numbers shown are for DW and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW and N packages.

timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... 7 V
Input voltage, V_I ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltge		2			V
V_{IL}	Low-level input voltge				0.8	V
I_{OH}	High-level output curent	Q outputs			−1.6	mA
		Status flags			−0.4	
I_{OL}	Low-level output curent	Q outputs			24	mA
		Status flags			8	
fclock	Clock frequency	LDCK	0		40	MHz
		UNCK	0		40	
t_w	Pulse duration	$\overline{RST}$ low	18			ns
		LDCK low	15			
		LDCK high	10			
		UNCK low	15			
		UNCK high	10			
t_{su}	Setup time	Data before LDCK↑	8			ns
		$\overline{RST}$ (inactive) before LDCK↑	5			
		LDCK (inactive) before $\overline{RST}$↑	5			
t_h	Hold time	Data after LDCK↑	5			ns
T_A	Operating free-air temperature		0		70	°C

NOTE 1: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates the V_{IL}, V_{IH}, or minimum pulse duration limits can cause a false clock or improper operation of the internal read and write pointers.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = −2.6 mA	2.4	3.2		V
	Status flags	V_{CC} = 4.5 V to 5.5 V,	I_{OL} = −0.4 mA	V_{CC}−2			
V_{OL}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
	Status flags	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	µA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			85	140	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 2)

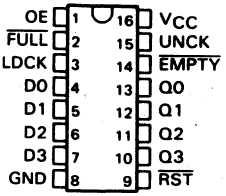
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	MAX	
	LDCK		40		
	UNCK		40		
t_{pd}	LDCK↑	Any Q	6	30	ns
t_{pd}	UNCK↑	Any Q	6	30	ns
t_{PLH}	LDCK↑	$\overline{EMPTY}$	5	25	ns
t_{PHL}	UNCK↑	$\overline{EMPTY}$	6	27	ns
t_{PHL}	$\overline{RST}$↓	$\overline{EMPTY}$	5	26	ns
t_{pd}	LDCK↑	$\overline{EMPTY+2}$	7	33	ns
t_{pd}	UNCK↑	$\overline{EMPTY+2}$	9	35	ns
t_{PLH}	$\overline{RST}$↓	$\overline{EMPTY+2}$	9	33	ns
t_{pd}	LDCK↑	$\overline{FULL-2}$	7	33	ns
t_{pd}	UNCK↑	$\overline{FULL-2}$	9	35	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL-2}$	9	33	ns
t_{PHL}	LDCK↑	$\overline{FULL}$	6	27	ns
t_{PLH}	UNCK↑	$\overline{FULL}$	5	25	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL}$	8	31	ns
t_{en}	OE↑	Q	2	15	ns
t_{dis}	OE↓	Q	1	15	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

D3247, FEBRUARY 1989

- **Independent Asynchronous Inputs and Outputs**
- **16 Words by 4 Bits Each**
- **Data Rates From 0 to 40 MHz**
- **Fall-Through Time . . . 14 ns Typ**
- **3-State Outputs**

DW OR N PACKAGE
(TOP VIEW)



description

This 64-bit memory uses Advanced Low-Power Schottky technology and features high speed and fast fall-through times. It is organized as 16 words by 4 bits each.

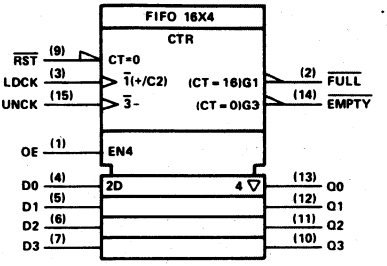
A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ output flags. The $\overline{\text{FULL}}$ output will be low when the memory is full, and high when the memory is not full. The $\overline{\text{EMPTY}}$ output will be low when the memory is empty, and high when it is not empty.

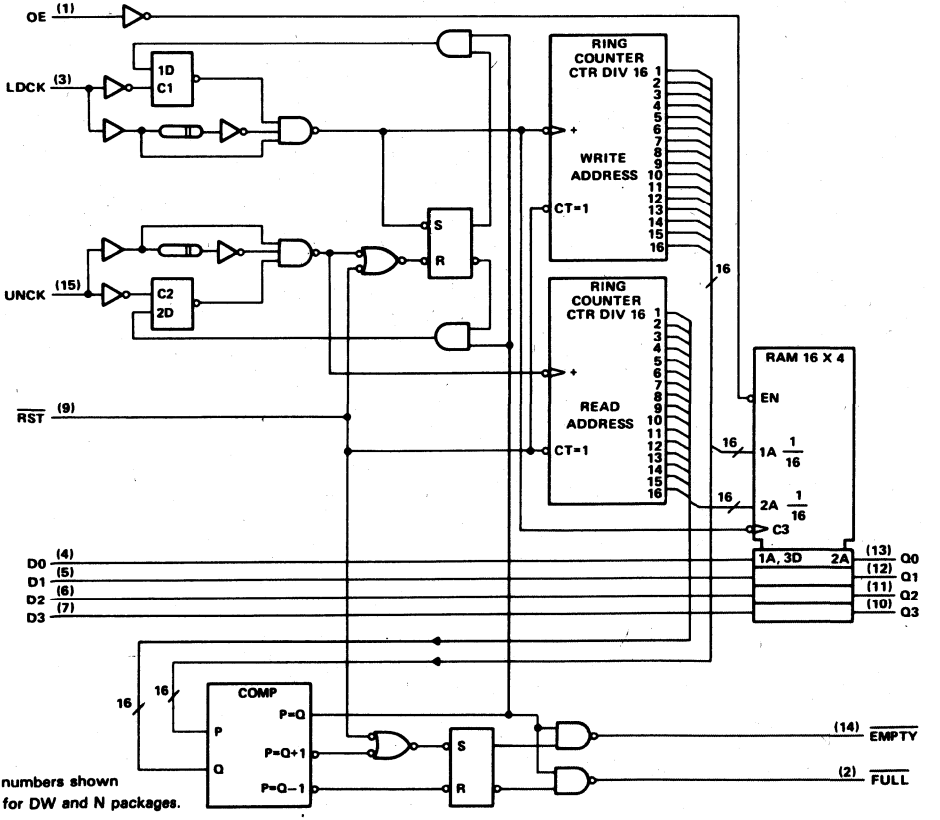
A low level on the reset input ($\overline{\text{RST}}$) resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and sets $\overline{\text{FULL}}$ high. The outputs are not reset to any specific logic levels. The first low-to-high transition on LDCK, either after a $\overline{\text{RST}}$ pulse or from an empty condition, will cause $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable input (OE) is low. OE does not affect either the $\overline{\text{FULL}}$ or $\overline{\text{EMPTY}}$ output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

logic symbol†



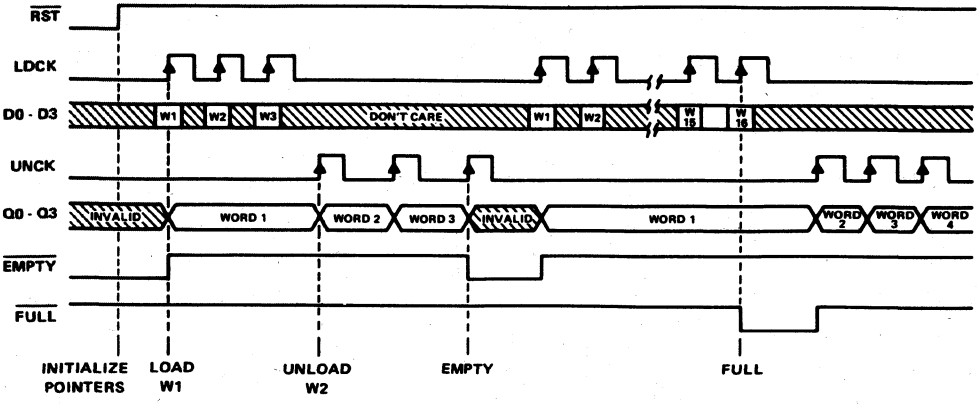
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

logic diagram (positive logic)



Pin numbers shown are for DW and N packages.

timing diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			−2.6	mA
		$\overline{FULL}$, $\overline{EMPTY}$			−0.4	
I_{OL}	Low-level output current	Q outputs			24	mA
		$\overline{FULL}$, $\overline{EMPTY}$			8	
f_{clock}†	Clock frequency	LDCK	0		40	MHz
		UNCK	0		40	
t_w	Pulse duration	$\overline{RST}$ low	18			ns
		LDCK low	15			
		LDCK high	10			
		UNCK low	15			
		UNCK high	10			
t_{su}	Setup time	Data before LDCK↑	8			ns
		LDCK inactive before $\overline{RST}$↑	5			
t_h	Hold time	Data after LDCK↑	5			ns
		LDCK inactive after $\overline{RST}$↑	5			
T_A	Operating free-air temperature		0		70	°C

†The maximum possible clock frequency is 40 MHz. The maximum clock frequency when using a 50% duty cycle is 33.3 MHz.

NOTE 1: To ensure proper operation, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates limits for maximum V_{IL}, minimum V_{IH}, or minimum pulse duration can cause a false clock or improper operation of the internal read and write pointers.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	$\overline{FULL}$, EMPTY	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
	$\overline{FULL}$, $\overline{EMPTY}$	V_{CC} = 4.5 V,	I_{OH} = 4 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			80	125	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 2)

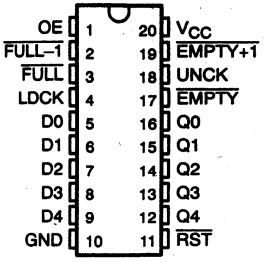
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}	LDCK			50		40		MHz
	UNCK			50		40		
t_{pd}	LDCK↑	Any Q		14	23	6	30	ns
t_{pd}	UNCK↑	Any Q		15	23	6	30	ns
t_{PLH}	LDCK↑	$\overline{EMPTY}$		13	20	5	25	ns
t_{PHL}	UNCK↑	$\overline{EMPTY}$		15	22	6	27	ns
t_{PHL}	$\overline{RST}$↓	$\overline{EMPTY}$		15	21	5	26	ns
t_{PHL}	LDCK↑	$\overline{FULL}$		15	22	6	27	ns
t_{PLH}	UNCK↑	$\overline{FULL}$		13	20	5	25	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL}$		16	23	7	28	ns
t_{en}	OE↑	Q		5	12	1	14	ns
t_{dis}	OE↓	Q		5	12	1	16	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

D3487, MARCH 1990

- **Independent Asychronous Inputs and Outputs**
- **16 Words by 5 Bits Each**
- **Data Rates From 0 to 40 MHz**
- **Fall-Through Time . . . 14 ns Typ**
- **3-State Outputs**

DW OR N PACKAGE
(TOP VIEW)



description

These 80-bit memories use Advanced Low-Power Schottky technology and feature high speed and fast fall-through times. They are organized as 16 words by 5 bits each.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

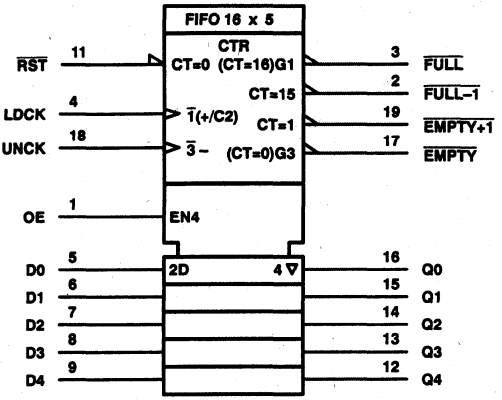
Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals will have no effect. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$, $\overline{\text{FULL–1}}$, and $\overline{\text{FULL+1}}$ output flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when it is not full. The $\overline{\text{FULL–1}}$ output is low when the memory contains 15 data words. The $\overline{\text{EMPTY}}$ output is low when the memory is empty and high when it is not empty. The $\overline{\text{EMPTY+1}}$ output is low when two words remain in memory.

A low level on the reset input ($\overline{\text{RST}}$) resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and sets $\overline{\text{FULL}}$, $\overline{\text{FULL–1}}$, and $\overline{\text{EMPTY+1}}$ high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK, after either a $\overline{\text{RST}}$ pulse or from an empty condition, causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable input (OE) is low. OE does not affect the output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

The SN74ALS233B is characterized for operation from 0°C to 70°C.

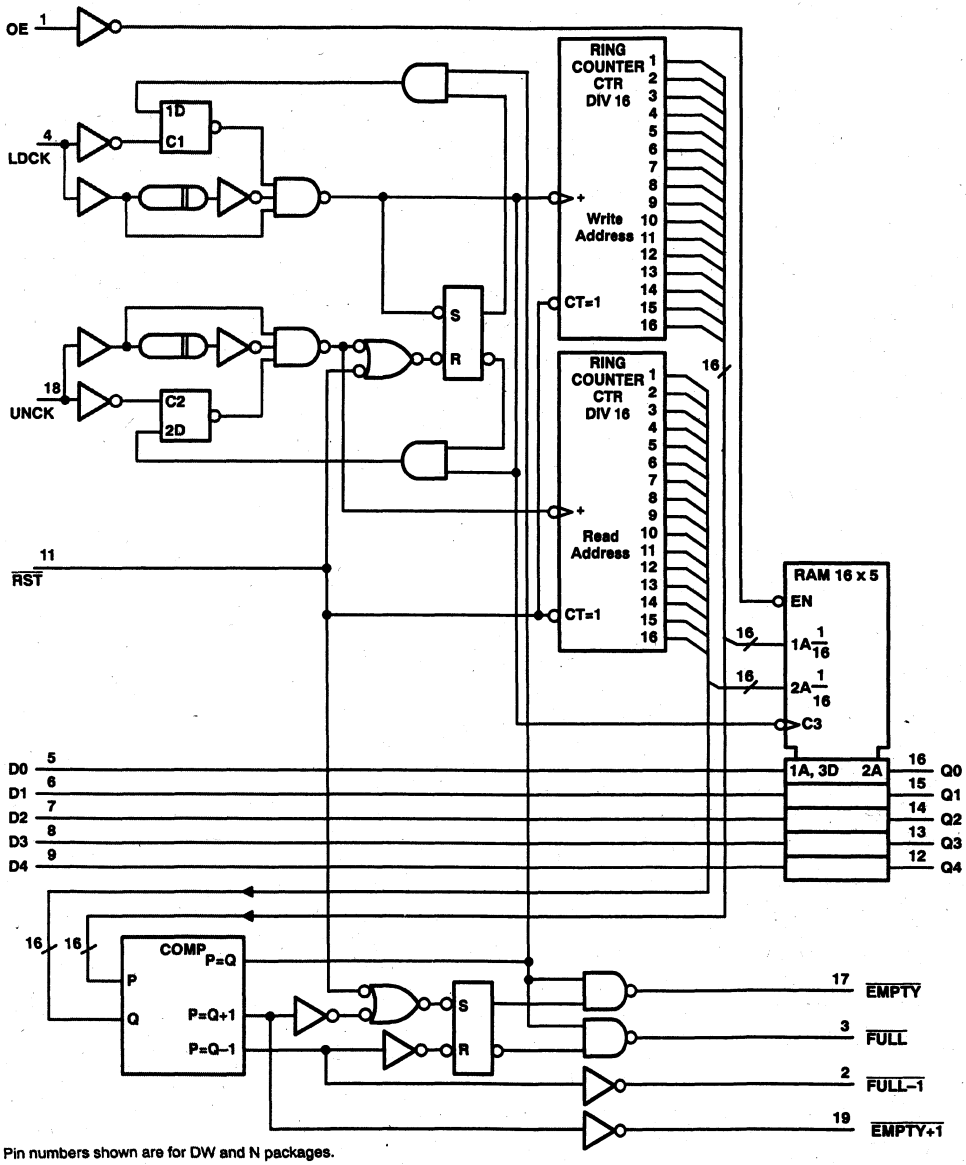
logic symbol†



† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

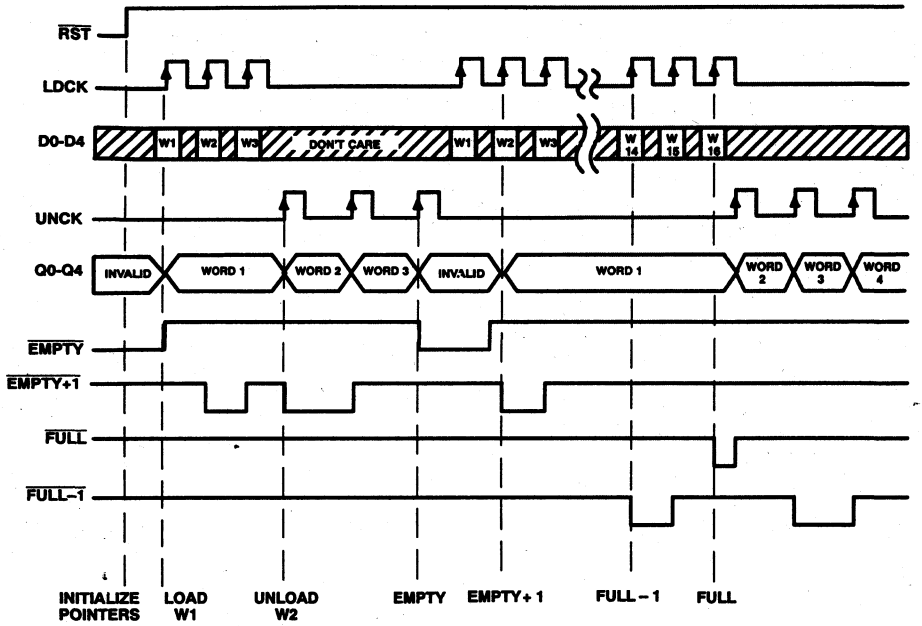
Pin numbers shown are for DW and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW and N packages.

timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	– 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltge		2			V
V_{IL}	Low-level input voltge				0.8	V
I_{OH}	High-level output curent	Q outputs			−1.6	mA
		Status flags			−0.4	
I_{OL}	Low-level output curent	Q outputs			24	mA
		Status flags			8	
fclock	Clock frequency	LDCK	0		40	MHz
		UNCK	0		40	
t_w	Pulse duration	$\overline{RST}$ low	18			ns
		LDCK low	15			
		LDCK high	10			
		UNCK low	15			
		UNCK high	10			
t_{su}	Setup time	Data before LDCK↑	8			ns
		$\overline{RST}$ (inactive) before LDCK↑	5			
		LDCK (inactive) before $\overline{RST}$↑	5			
t_h	Hold time	Data after LDCK↑	5			ns
T_A	Operating free-air temperature		0		70	°C

NOTE 1: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates the V_{IL}, V_{IH}, or minimum pulse duration limits can cause a false clock or improper operation of the internal read and write pointers.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = −2.6 mA	2.4	3.2		V
	Status flags	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			
V_{OL}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
	Status flags	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	µA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			88	133	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 2)

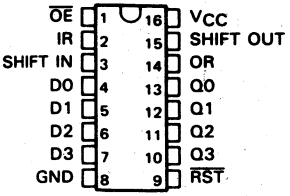
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	MAX	
	LDCK		40		
	UNCK		40		
t_{pd}	LDCK↑	Any Q	6	32	ns
t_{pd}	UNCK↑	Any Q	6	30	ns
t_{PLH}	LDCK↑	$\overline{EMPTY}$	5	25	ns
t_{PHL}	UNCK↑	$\overline{EMPTY}$	6	27	ns
t_{PHL}	$\overline{RST}$↓	$\overline{EMPTY}$	5	25	ns
t_{pd}	LDCK↑	$\overline{EMPTY+1}$	7	34	ns
t_{pd}	UNCK↑	$\overline{EMPTY+1}$	7	34	ns
t_{PLH}	$\overline{RST}$↓	$\overline{EMPTY+1}$	8	31	ns
t_{pd}	LDCK↑	$\overline{FULL-1}$	9	33	ns
t_{pd}	UNCK↑	$\overline{FULL-1}$	8	32	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL-1}$	11	32	ns
t_{PHL}	LDCK↑	$\overline{FULL}$	6	27	ns
t_{PLH}	UNCK↑	$\overline{FULL}$	5	25	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL}$	9	30	ns
t_{en}	OE↑	Q	2	15	ns
t_{dis}	OE↓	Q	1	15	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

D2958, OCTOBER 1986 – REVISED APRIL 1988

- **Asynchronous Operation**
- **Organized as 64 Words of 4 Bits**
- **Data Rates from 0 to 30 MHz**
- **3-State Outputs**
- **Similar to MMI67401B with Higher Speed and 3-State Outputs**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS234 . . . N PACKAGE
(TOP VIEW)



description

The SN74ALS234 is a 256-bit memory utilizing Advanced Low-Power Schottky IMPACT™ Technology. It features high speed with fast fall-through times and is organized as 64 words by 4 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The 'ALS234 is designed to process data at rates from 0 to 30 megahertz in a bit-parallel format, word by word.

Data is written into memory on the rising edge of the Shift In input. When Shift In goes low, the first data word ripples through to the output (see Figure 1). As the FIFO fills up, the data words stack up in the order they were written. When the FIFO is full, additional Shift In pulses have no effect. Data is shifted out of memory on the falling edge of the Shift Out input (see Figure 2). When the FIFO is empty, additional Shift Out pulses have no effect. The last data word remains at the outputs until a new word falls through or $\overline{RST}$ goes low.

Status of the 'ALS234 FIFO memory is monitored by the Output Ready (OR) and Input Ready (IR) flags. When the OR flag is high, valid data is available at the outputs. The OR flag is low when Shift Out is high and will stay low when the FIFO is empty. The IR status flag is high when the inputs are ready to receive more data. The IR flag is low when Shift In is high and stays low when the FIFO is full.

When the FIFO is empty, input data is shifted to the output automatically when Shift In goes low. If Shift Out is held high during this time, the OR flag pulses high indicating valid data at the outputs (see Figure 3).

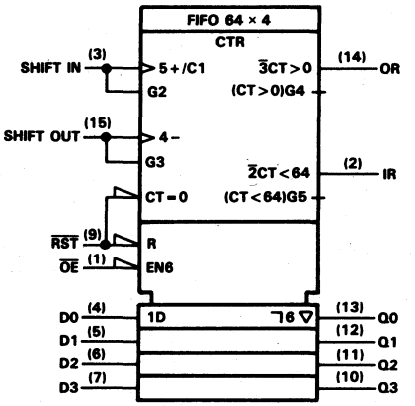
When the FIFO is full, data can be shifted in automatically by holding Shift In high and taking Shift Out low. A propagation delay after Shift Out goes low, IR will go high. If Shift In is still high when IR goes high, data at the inputs are automatically shifted in. Since IR is normally low when the FIFO is full and Shift In is high, only a high-level pulse is seen on the IR output (see Figure 4).

description (continued)

The FIFO must be reset after power up with a low-level pulse on the Master Reset input ($\overline{RST}$). This sets Input Ready (IR) high and Output Ready (OR) low signifying that the FIFO is empty. Resetting the FIFO sets the outputs to a low logic level (see Figure 1). If Shift In is high when $\overline{RST}$ goes high, the input data is shifted in and IR goes low and remains low until Shift In goes low. If Shift In goes low before $\overline{RST}$ goes high, the input data will not be shifted in and IR goes high. Data outputs are noninverting with respect to the data inputs and are at high impedance when Output Enable ($\overline{OE}$) is high. $\overline{OE}$ does not affect the IR and OR outputs.

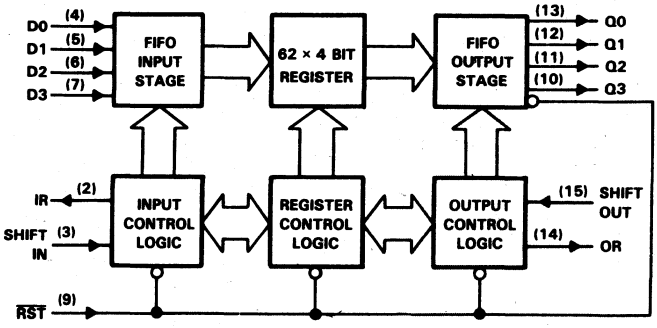
The SN74ALS234 is characterized for operation from 0°C to 70°C.

logic symbol†



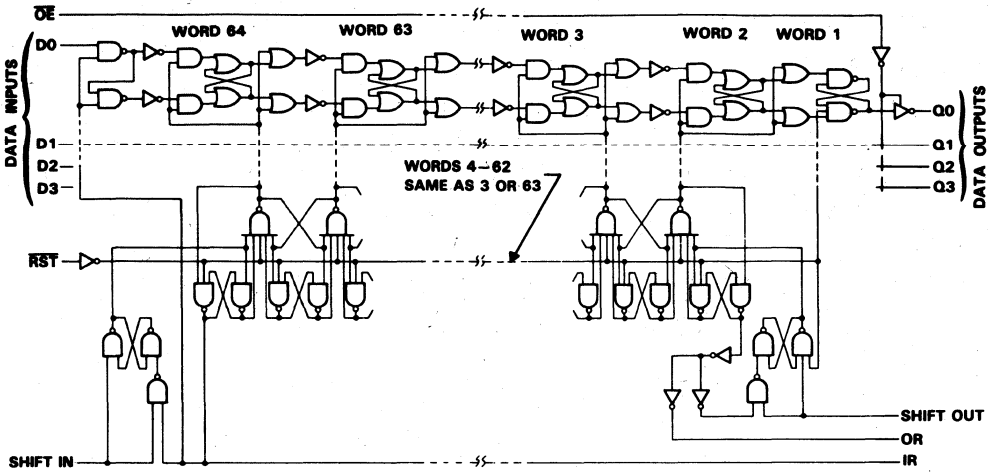
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram

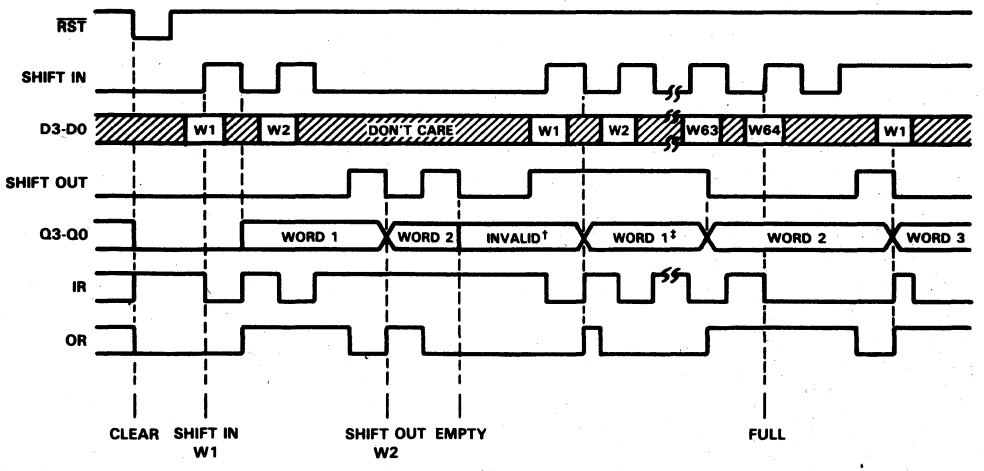


Pin numbers shown are for N packages.

logic diagram (positive logic)

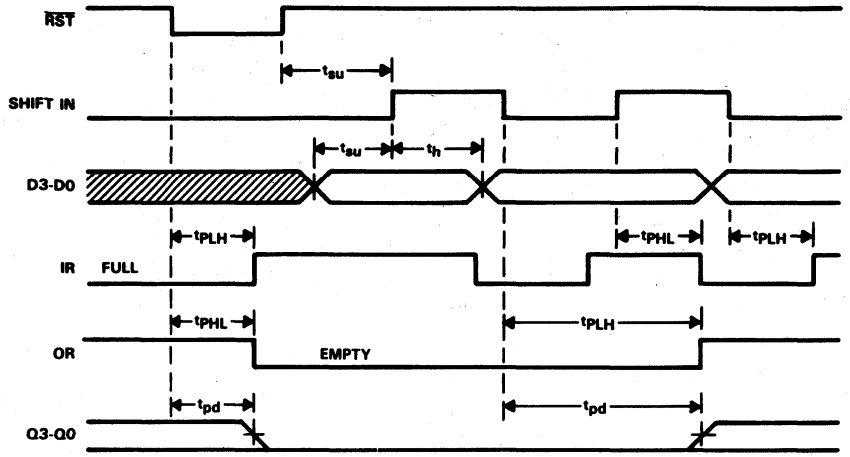


timing diagram



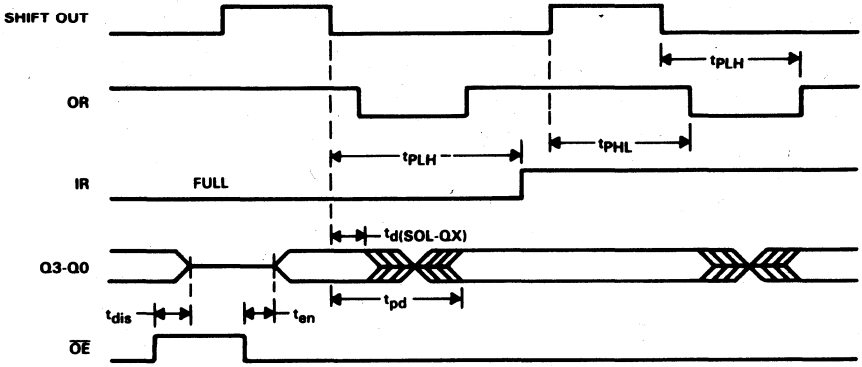
† The last data word shifted out of the FIFO remains at the output until a new word falls through or a $\overline{RST}$ pulse clears the FIFO.

‡ While the output data is considered valid only when the OR flag is high, the stored data remains at the output. Any additional words written into the FIFO will stack up behind the first word and will not appear at the output until Shift Out is taken low.



NOTE: SHIFT OUT is low

FIGURE 1. MASTER RESET AND DATA IN WAVEFORMS



NOTE: SHIFT IN is low

FIGURE 2. DATA OUT WAVEFORMS

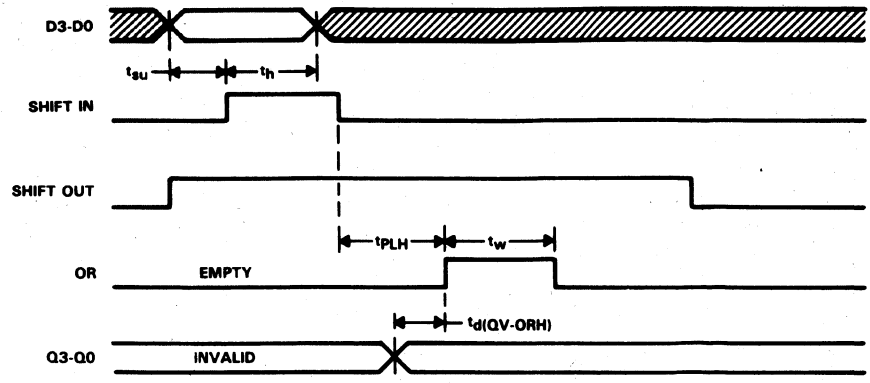


FIGURE 3. DATA FALL THROUGH WAVEFORMS

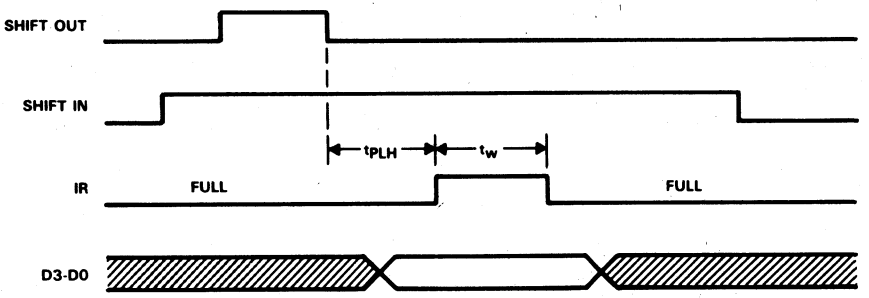


FIGURE 4. AUTOMATIC DATA IN WAVEFORMS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN74ALS234 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN74ALS234			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			−2.6	mA
		IR and OR			−0.4	
I_{OL}	Low-level output current	Q outputs			24	mA
		IR and OR			8	
f_{clock}	Clock frequency	SHIFT IN or SHIFT OUT	0		30	MHz
t_w	Pulse duration	SHIFT IN or SHIFT OUT high or low	15			ns
		$\overline{RST}$ low	15			
t_{su}	Setup time before SHIFT IN↑	Data	0			ns
		$\overline{RST}$ high (inactive)	15			
t_h	Hold time, data after SHIFT IN↑		17			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS234			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	Q	V_{CC} = 4.5 V,	I_{OH} = −1 mA				V
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
	IR, OR	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.7	3.4		
V_{OL}	Q	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
	IR, OR	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	I_{CCL}		100	145	mA
			I_{CCH}		97	142	
			I_{CCZ}		103	148	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			'ALS234			SN74ALS234		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	SHIFT IN			35		30		MHz
	SHIFT OUT			35		30		
t_w†	IR high			15		8		ns
t_w‡	OR high			19		8		ns
$t_{d(QV-ORH)}$	Q valid before OR ↑			6	9	-5	12	ns
$t_{d(SOL-QX)}$	Q valid after SHIFT OUT ↓			13		4		ns
tpd	SHIFT IN ↓	Q		600	800	350	1000	ns
t_{PHL}	SHIFT IN ↑	IR		20	26	8	30	ns
t_{PLH}	SHIFT IN ↓	IR		16	21	6	25	ns
t_{PLH}§	SHIFT IN ↓	OR		600	800	350	1000	ns
tpd	SHIFT OUT ↓	Q		13	17	4	22	ns
t_{PHL}	SHIFT OUT ↑	OR		23	27	7	33	ns
t_{PLH}	SHIFT OUT ↓	OR		20	24	6	30	ns
t_{PLH}§	SHIFT OUT ↓	IR		600	800	350	1000	ns
t_{PHL}	$\overline{RST}$ ↓	OR		22	26	10	34	ns
t_{PLH}	$\overline{RST}$ ↓	IR		17	21	6	27	ns
t_{PHL}	$\overline{RST}$ ↓	Q		14	17	5	19	ns
t_{dis}	$\overline{OE}$ ↑	Q		7	13	2	15	ns
t_{en}	$\overline{OE}$ ↓	Q		6	12	2	13	ns

† The IR output pulse occurs when the FIFO is full, Shift In is high, and Shift Out is pulsed (see Figure 4).
‡ The OR output pulse occurs when the FIFO is empty, Shift Out is high, and Shift In is pulsed (see Figure 3).
§ Data throughput or "fall through" times.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION INFORMATION

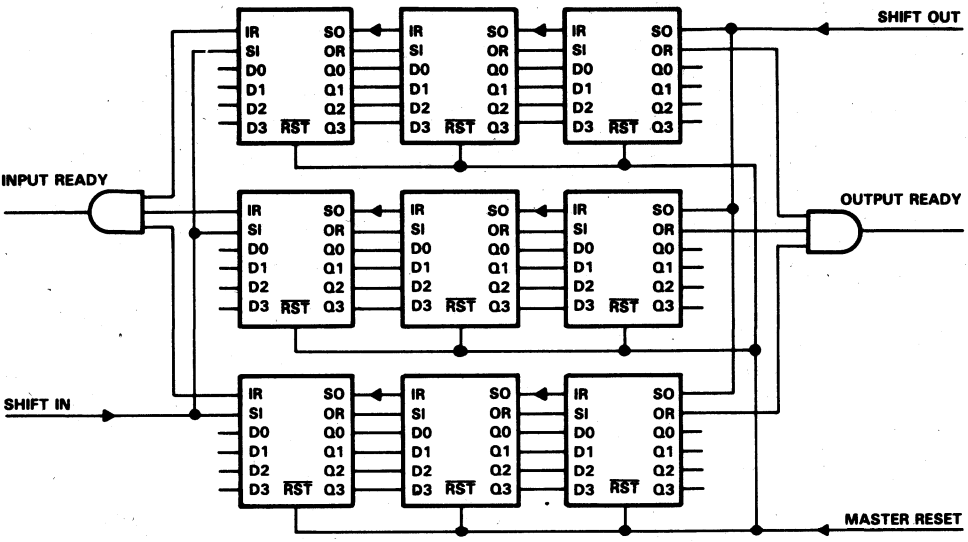


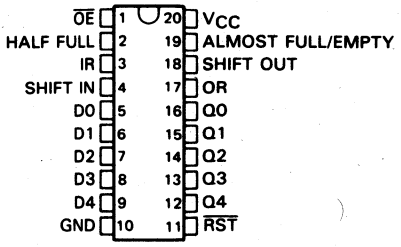
FIGURE 5. 192-WORD BY 12-BIT EXPANSION

SN74ALS235
64 x 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORY

D2958, OCTOBER 1986

- **Asynchronous Operation**
- **Organized as 64 Words of 5 Bits**
- **Data Rates from 0 to 25 MHz**
- **3-State Outputs**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS235 . . . DW OR N PACKAGE
(TOP VIEW)



description

The SN74ALS235 is a 320-bit memory utilizing Advanced Low-Power Schottky IMPACT™ Technology. It features high speed with fast fall-through times and is organized as 64 words by 5 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The 'ALS235 is designed to process data at rates from 0 to 25 megahertz in a bit-parallel format, word by word.

Data is written into memory on the rising edge of the Shift In input. When Shift In goes low, the first data word ripples through to the output (see Figure 1). As the FIFO fills up, the data words stack up in the order they were written. When the FIFO is full, additional Shift In pulses have no effect. Data is shifted out of memory on the falling edge of the Shift Out input (see Figure 2). When the FIFO is emply, additional Shift Out pulses have no effect. The last data word remains at the outputs until a new word falls through or $\overline{RST}$ goes low.

Status of the 'ALS235 FIFO memory is monitored by the Output Ready (OR), Input Ready (IR), Almost Full/Empty, and Half Full flags. When the OR flag is high, valid data is available at the outputs. The OR flag is low when Shift Out is high and will stay low when the FIFO is empty. The IR status flag is high when the inputs are ready to receive more data. The IR flag is low when Shift In is high and stays low when the FIFO is full. The Almost Full/Empty flag is high when the FIFO contains eight or less words (see Figure 5), or fifty-six or more words (see Figure 6). The Almost Full/Empty flag is low when the FIFO contains between nine and fifty-five words. The Half Full flag is high when the FIFO contains thirty-two or more words, and is low when the FIFO contains thirty-one words or less (see Figure 7).

When the FIFO is empty, input data is shifted to the output automatically when Shift In goes low. If Shift Out is held high during this time, the OR flag pulses high indicating valid data at the outputs (see Figure 3).

When the FIFO is full, data can be shifted in automatically by holding Shift In high and taking Shift Out low. A propagation delay after Shift Out goes low, IR will go high. If Shift In is still high when IR goes high, data at the inputs are automatically shifted in. Since IR is normally low, when the FIFO is full and Shift In is high, only a high-level pulse is seen on the IR output.

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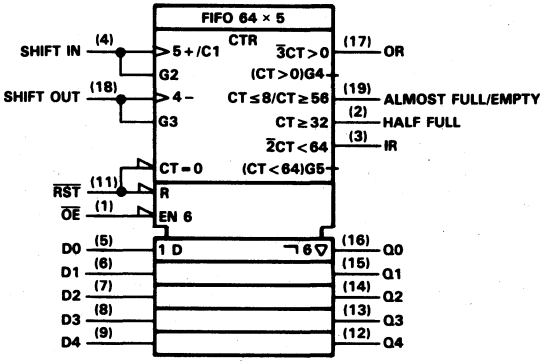
TEXAS INSTRUMENTS

description (continued)

The FIFO must be reset after power up with a low-level pulse on the Master Reset input ($\overline{RST}$). This sets Input Ready (IR) high and Output Ready (OR) low signifying that the FIFO is empty. Resetting the FIFO sets the outputs to a low logic level (see Figure 1). If Shift In is high when $\overline{RST}$ goes high, the input data is shifted in and IR goes low and remains low until Shift In goes low. If Shift In goes low before $\overline{RST}$ goes high, the input data will not be shifted in and IR goes high. Data outputs are noninverting with respect to the data inputs and are at high impedance when Output Enable ($\overline{OE}$) is high. $\overline{OE}$ does not affect the status flag outputs (see Figure 2).

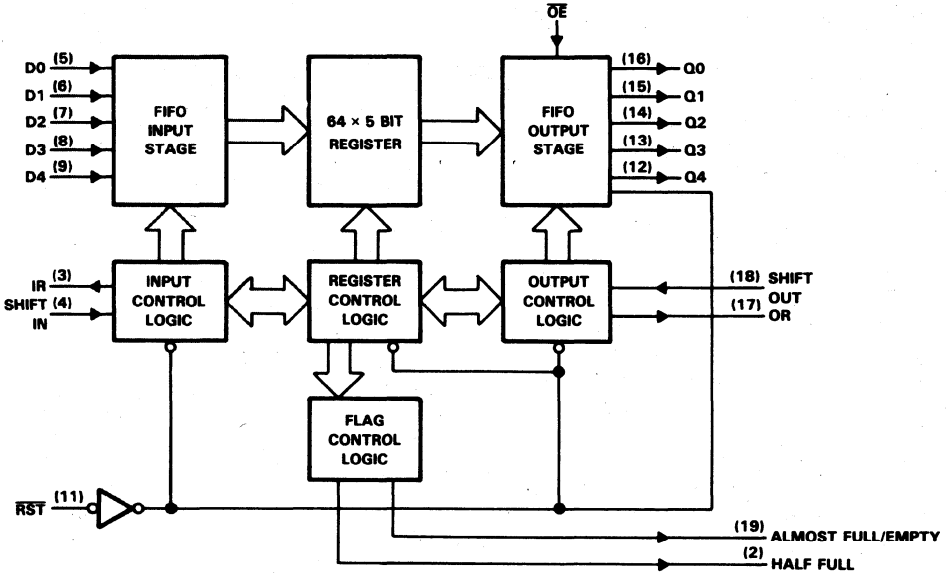
The SN74ALS235 is characterized for operation from 0°C to 70°C.

logic symbol†

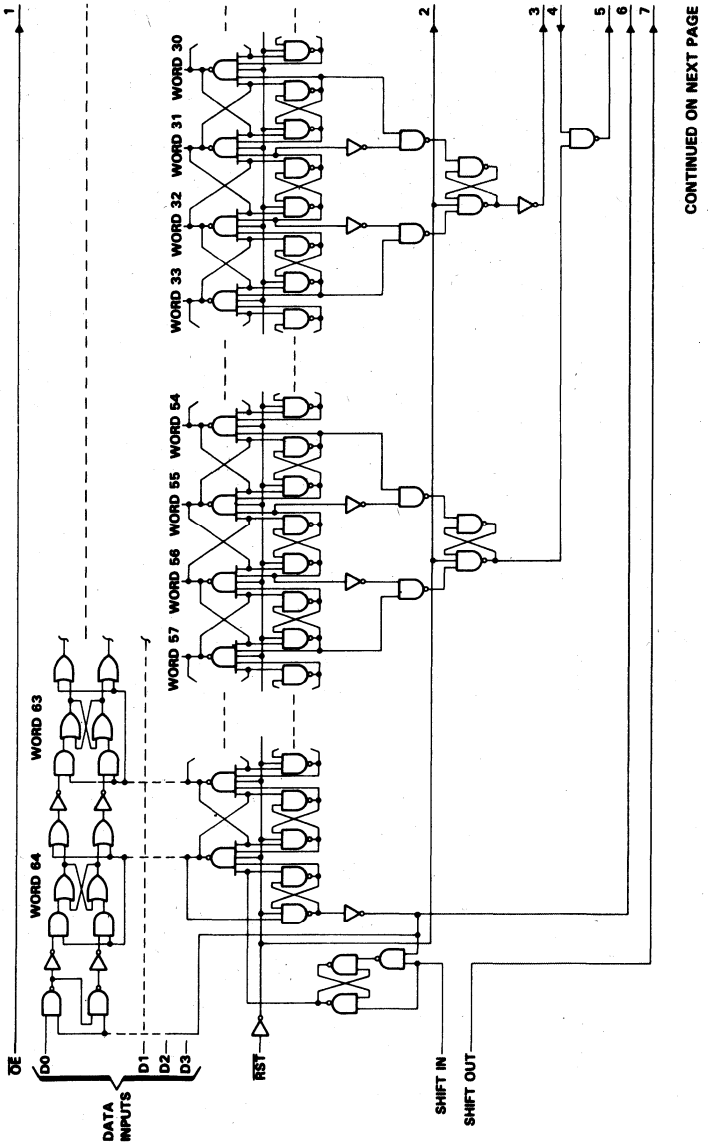


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

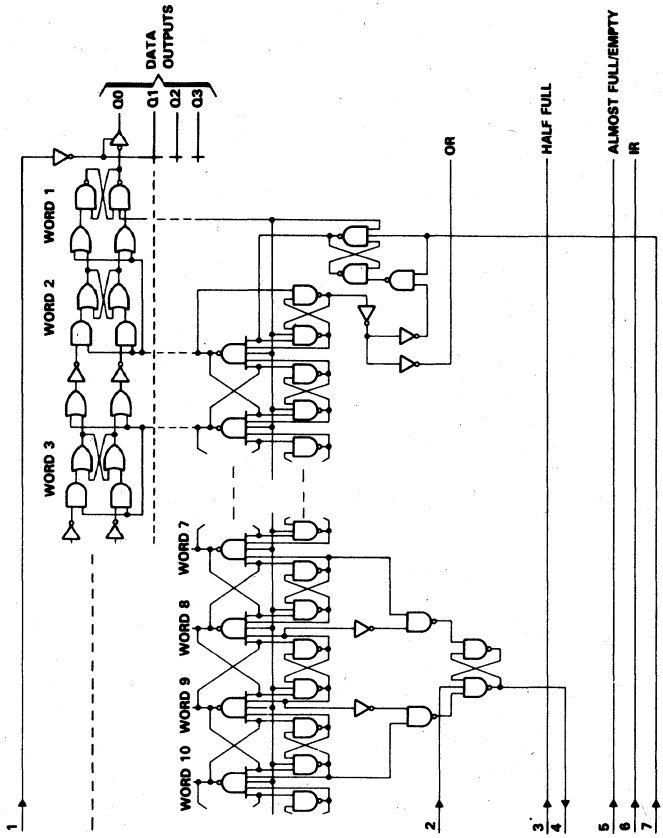
functional block diagram



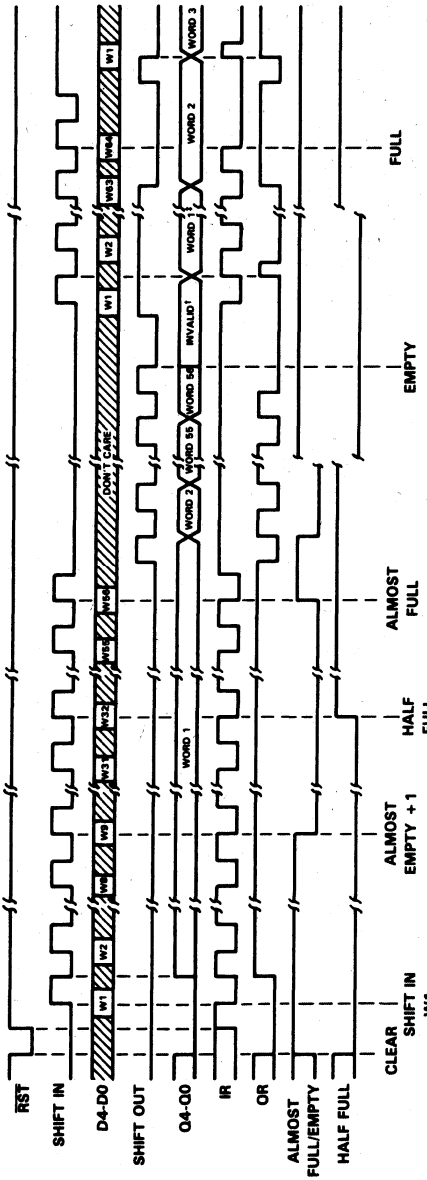
logic diagram (positive logic)



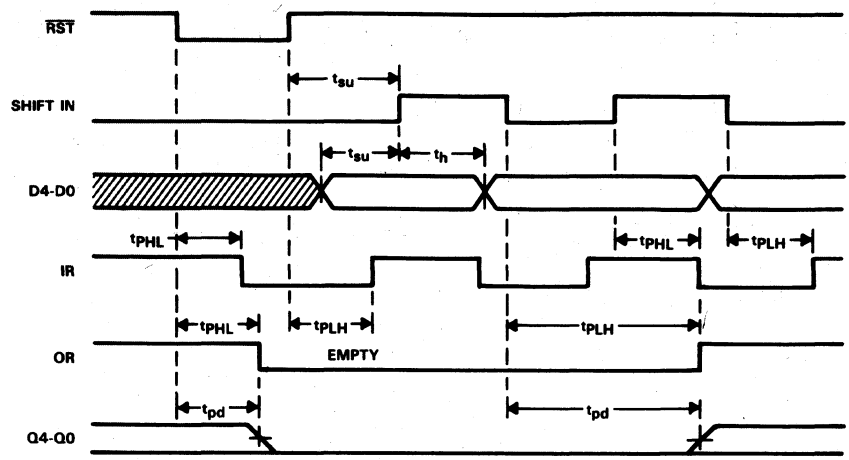
logic diagram (positive logic) (continued)



timing diagram

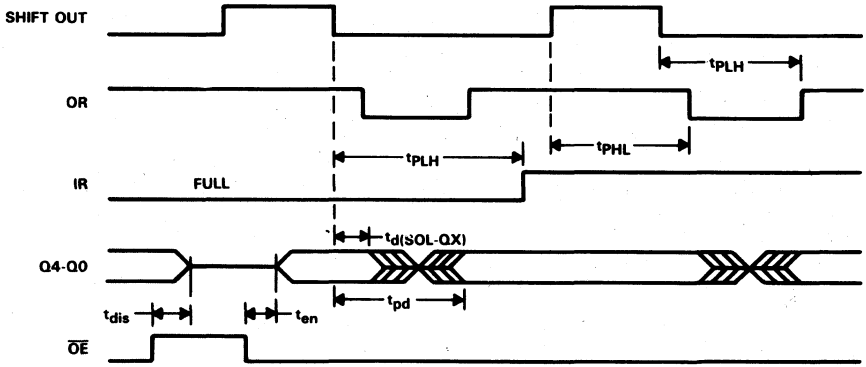


† The last data word shifted out of the FIFO remains at the output until a new word falls through or a $\overline{RST}$ pulse clears the FIFO.
‡ While the output data is considered valid only when the OR flag is high, the stored data remains at the output. Any additional words written into the FIFO will stack up behind the first word and will not appear at the output until Shift Out is taken low.



NOTE: SHIFT OUT is low

FIGURE 1. MASTER RESET AND DATA IN WAVEFORMS



NOTE: SHIFT IN is low

FIGURE 2. DATA OUT WAVEFORMS

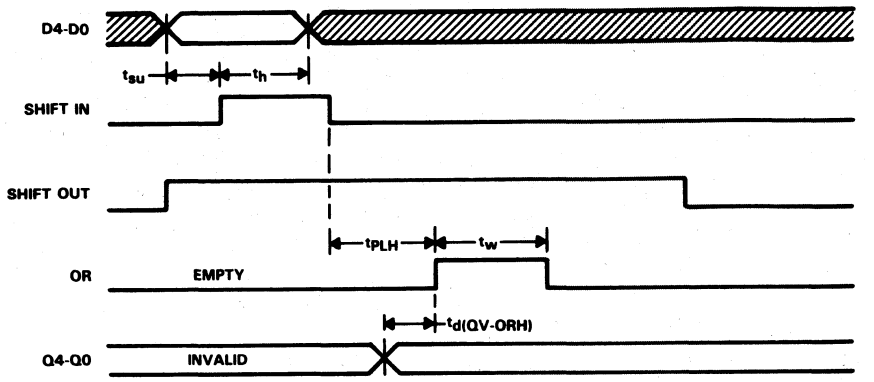


FIGURE 3. DATA FALL THROUGH WAVEFORMS

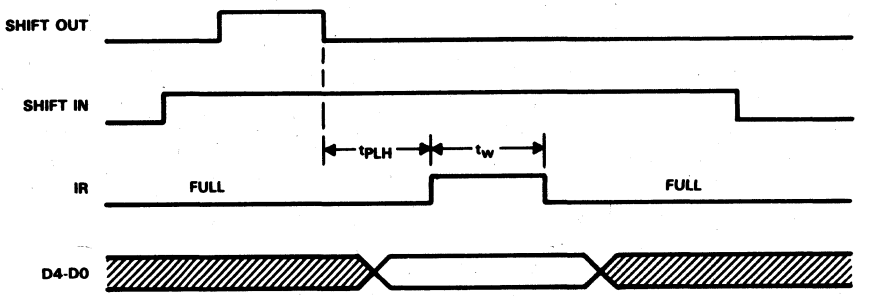


FIGURE 4. AUTOMATIC DATA IN WAVEFORMS

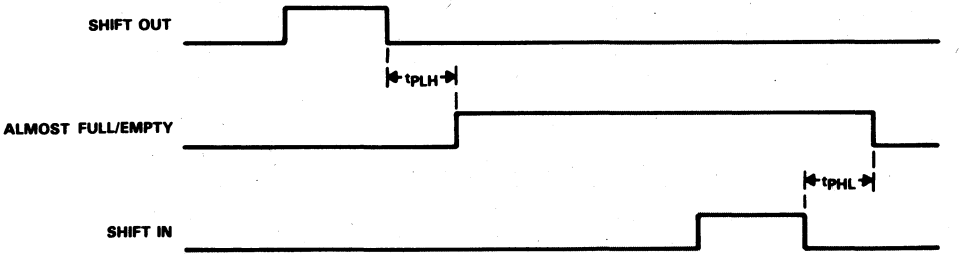


FIGURE 5. ALMOST EMPTY WAVEFORMS

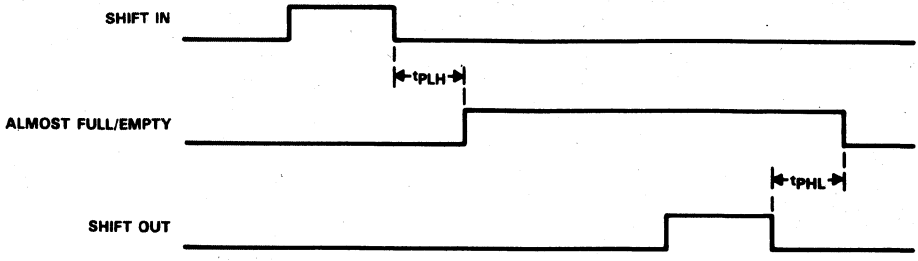


FIGURE 6. ALMOST FULL WAVEFORMS

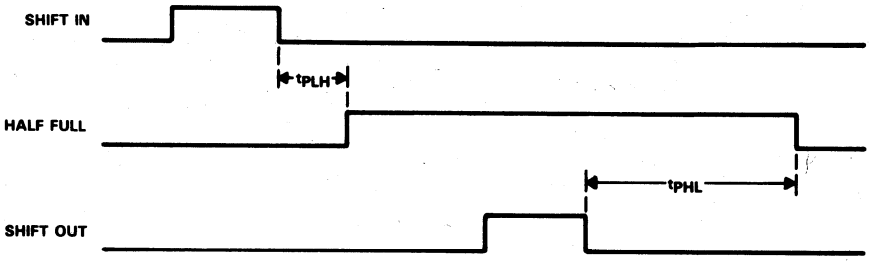


FIGURE 7. HALF FULL WAVEFORMS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN74ALS235 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN74ALS235			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			−2.6	mA
		Flags			−0.4	
I_{OL}	Low-level output current	Q outputs			24	mA
		Flags			8	
f_{clock}	Clock frequency	SHIFT IN or SHIFT OUT	0		25	MHz
t_w	Pulse duration	SHIFT IN or SHIFT OUT high or low	15			ns
		$\overline{RST}$ low	15			
t_{su}	Setup time before SHIFT IN↑	Data	0			ns
		$\overline{RST}$ high (inactive)	15			
t_h	Hold time, data after SHIFT IN↑		17			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS235			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	Q	V_{CC} = 4.5 V,	I_{OH} = −1 mA				V
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
	Flags	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.7	3.4		
V_{OL}	Q	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
	Flags	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	I_{CCL}		112	165	mA
			I_{CCH}		105	160	
			I_{CCZ}		115	170	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, $R1$ = 500 Ω, $R2$ = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, $R1$ = 500 Ω, $R2$ = 500 Ω, T_A = MIN to MAX		UNIT
			'ALS235			SN74ALS235		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	SHIFT IN			30		25		MHz
	SHIFT OUT			30		25		
t_w†	IR high			15		8		ns
t_w‡	OR high			19		8		ns
$t_{d(QV-ORH)}$	Q valid before OR ↑			6	9	−5	12	ns
$t_{d(SOL-QX)}$	Q valid after SHIFT OUT ↓			13		4		ns
t_{pd}	SHIFT IN ↓	Q		600	800	350	1000	ns
t_{PHL}	SHIFT IN ↑	IR		20	26	8	30	ns
t_{PLH}	SHIFT IN ↓	IR		16	21	6	25	ns
t_{PLH}§	SHIFT IN ↓	OR		600	800	350	1000	ns
t_{PHL}	SHIFT IN ↓	ALMOST F/E		550	700	290	880	ns
t_{PLH}	SHIFT IN ↓	ALMOST F/E		85	115	40	150	ns
t_{PLH}	SHIFT IN ↓	HALF FULL		340	410	180	510	ns
t_{pd}	SHIFT OUT ↓	Q		13	17	4	22	ns
t_{PHL}	SHIFT OUT ↑	OR		23	27	7	33	ns
t_{PLH}	SHIFT OUT ↓	OR		20	24	6	30	ns
t_{PLH}§	SHIFT OUT ↓	IR		600	800	350	1000	ns
t_{PHL}	SHIFT OUT ↓	ALMOST F/E		550	700	290	880	ns
t_{PLH}	SHIFT OUT ↓	ALMOST F/E		85	115	35	150	ns
t_{PHL}	SHIFT OUT ↓	HALF FULL		340	410	170	510	ns
t_{PHL}	$\overline{RST}$ ↓	OR		22	26	10	34	ns
t_{PLH}	$\overline{RST}$ ↑	IR		12	18	5	22	ns
t_{PHL}	$\overline{RST}$ ↓	IR		12	18	5	22	ns
t_{PHL}	$\overline{RST}$ ↓	Q		14	17	5	19	ns
t_{dis}	$\overline{OE}$ ↑	Q		7	13	2	15	ns
t_{en}	$\overline{OE}$ ↓	Q		6	12	2	13	ns

† The IR output pulse occurs when the FIFO is full, Shift In is high, and Shift Out is pulsed (see Figure 4).
‡ The OR output pulse occurs when the FIFO is empty, Shift Out is high, and Shift In is pulsed (see Figure 3).
§ Data throughput or "fall through" times.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION INFORMATION

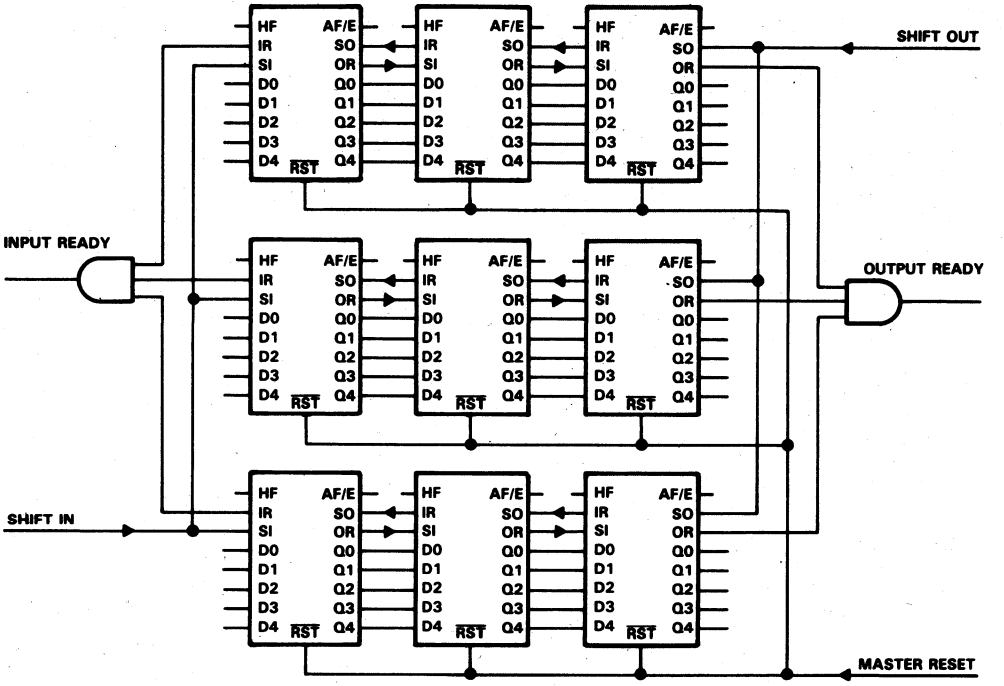


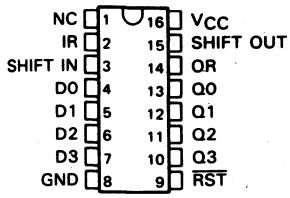
FIGURE 8. 192-WORD BY 15-BIT EXPANSION

D2958, OCTOBER 1986 – REVISED APRIL 1988

- **Asynchronous Operation**
- **Organized as 64 Words of 4 Bits**
- **Data Rates from 0 to 30 MHz**
- **Pin-Compatible with MMI67401B with Higher Speed**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS236 . . . N PACKAGE

(TOP VIEW)



description

The SN74ALS236 is a 256-bit memory utilizing Advanced Low-Power Schottky IMPACT™ Technology. It features high speed with fast fall-through times and is organized as 64 words by 4 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The 'ALS236 is designed to process data at rates from 0 to 30 megahertz in a bit-parallel format, word by word.

Data is written into memory on the rising edge of the Shift In input. When Shift In goes low, the first data word ripples through to the output (see Figure 1). As the FIFO fills up, the data words stack up in the order they were written. When the FIFO is full, additional Shift In pulses have no effect. Data is shifted out of memory on the falling edge of the Shift Out input (see Figure 2). When the FIFO is empty, additional Shift Out pulses have no effect. The last data word remains at the outputs until a new word falls through or $\overline{RST}$ goes low

Status of the 'ALS236 FIFO memory is monitored by the Output Ready (OR) and Input Ready (IR) flags. When the OR flag is high, valid data is available at the outputs. The OR flag is low when Shift Out is high and will stay low when the FIFO is empty. The IR status flag is high when the inputs are ready to receive more data. The IR flag is low when Shift In is high and stays low when the FIFO is full.

When the FIFO is empty, input data is shifted to the output automatically when Shift In goes low. If Shift Out is held high during this time, the OR flag pulses high indicating valid data at the outputs (see Figure 3).

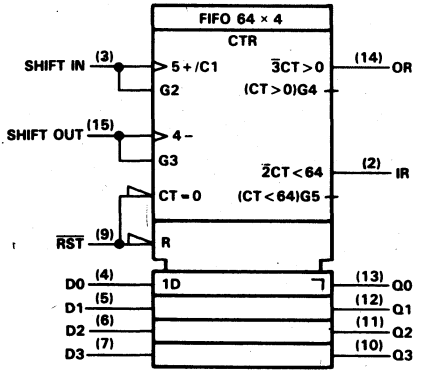
When the FIFO is full, data can be shifted in automatically by holding Shift In high and taking Shift Out low. A propagation delay after Shift Out goes low, IR will go high. If Shift In is still high when IR goes high, data at the inputs are automatically shifted in. Since IR is normally low when the FIFO is full and Shift In is high, only a high-level pulse is seen on the IR output (see Figure 4).

description (continued)

The FIFO must be reset after power up with a low-level pulse on the Master Reset input ($\overline{RST}$). This sets Input Ready (IR) high and Output Ready (OR) low signifying that the FIFO is empty. Resetting the FIFO sets the outputs to a low logic level (see Figure 1). If Shift In is high when $\overline{RST}$ goes high, the input data is shifted in and IR goes low and remains low until Shift In goes low. If Shift In goes low before $\overline{RST}$ goes high, the input data will not be shifted in and IR goes high. Data outputs are noninverting with respect to the data inputs.

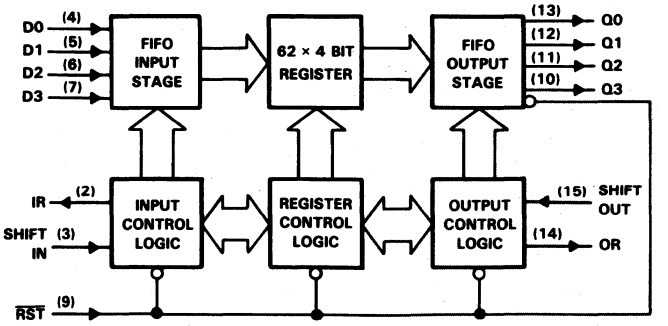
The SN74ALS236 is characterized for operation from 0°C to 70°C.

logic symbol†



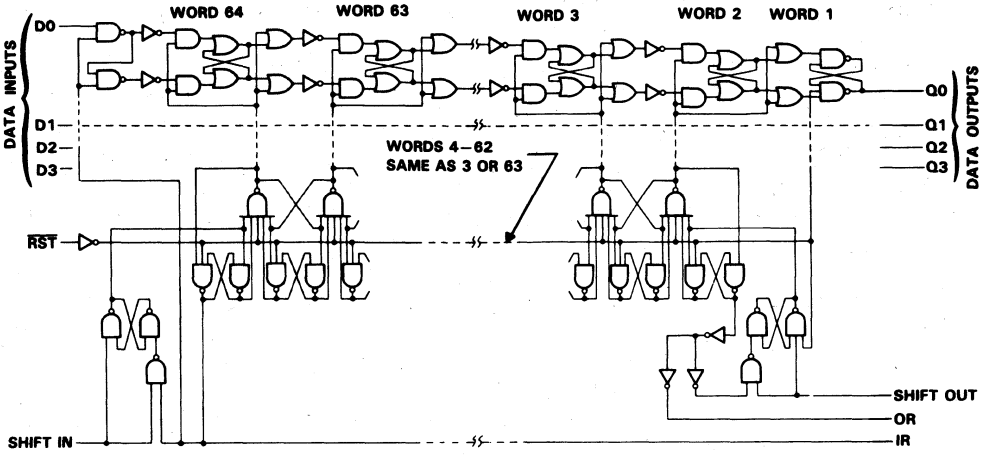
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram

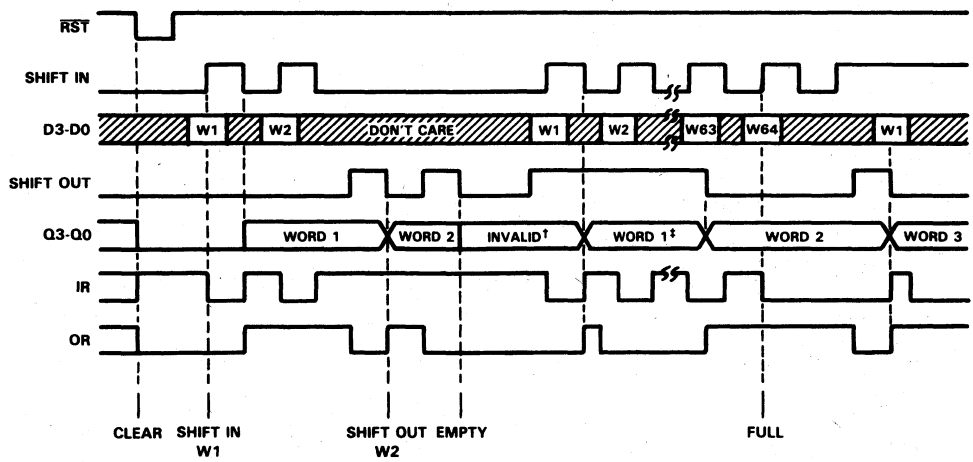


Pin numbers shown are for N packages.

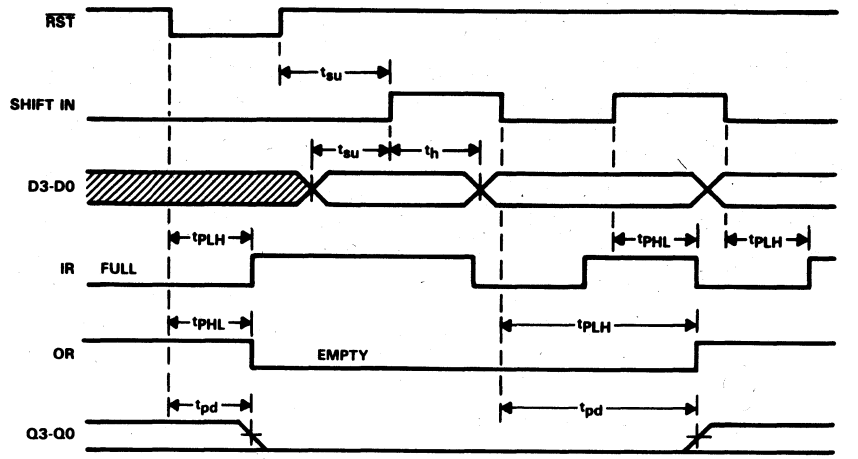
logic diagram (positive logic)



timing diagram

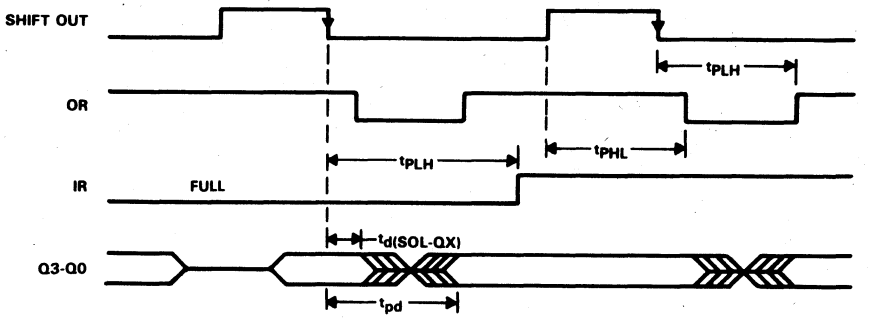


† The last data word shifted out of the FIFO remains at the output until a new word falls through or a $\overline{\text{RST}}$ pulse clears the FIFO.
‡ While the output data is considered valid only when the OR flag is high, the stored data remains at the output. Any additional words written into the FIFO will stack up behind the first word and will not appear at the output until SHIFT OUT is taken low.



NOTE: SHIFT OUT is low

FIGURE 1. MASTER RESET AND DATA IN WAVEFORMS



NOTE: SHIFT IN is low

FIGURE 2. DATA OUT WAVEFORMS

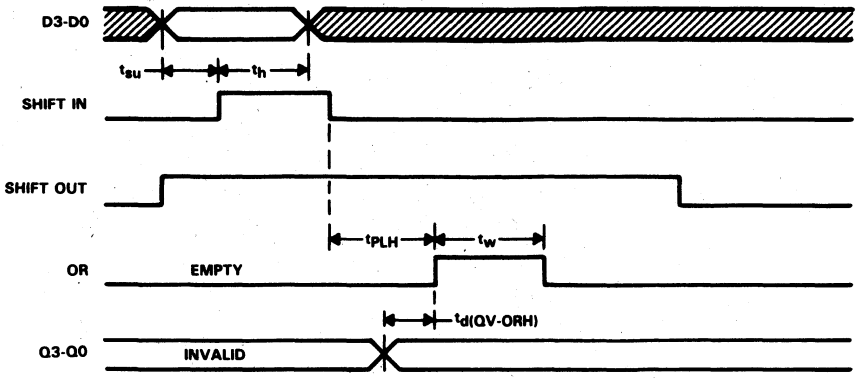


FIGURE 3. DATA FALL THROUGH WAVEFORMS

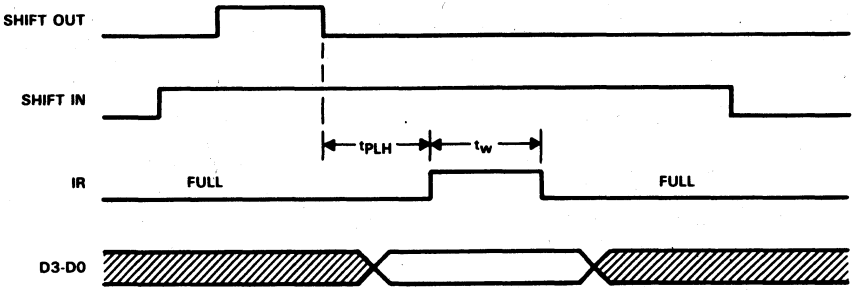


FIGURE 4. AUTOMATIC DATA IN WAVEFORMS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN74ALS236 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN74ALS236			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			−2.6	mA
		IR and OR			−0.4	
I_{OL}	Low-level output current	Q outputs			24	mA
		IR and OR			8	
f_{clock}	Clock frequency	SHIFT IN or SHIFT OUT	0		30	MHz
t_w	Pulse duration	SHIFT IN or SHIFT OUT high or low	15			ns
		$\overline{RST}$ low	15			
t_{su}	Setup time before SHIFT IN↑	Data	0			ns
		$\overline{RST}$ high (inactive)	15			
t_h	Hold time, data after SHIFT IN↑		17			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS236			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	Q	V_{CC} = 4.5 V,	I_{OH} = −1 mA				V
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
	IR, OR	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.7	3.4		
V_{OL}	Q	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
	IR, OR	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	I_{CCL}		100	145	mA
			I_{CCH}		97	142	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			'ALS236			SN74ALS236		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	SHIFT IN			35		30		MHz
	SHIFT OUT			35		30		
t_w†	IR high			15		8		ns
t_w‡	OR high			19		8		ns
$t_{d(QV-ORH)}$	Q valid before OR ↑			6	9	−5	12	ns
$t_{d(SOL-QX)}$	Q valid after SHIFT OUT ↓			13		4		ns
t_{pd}	SHIFT IN ↓	Q		600	800	350	1000	ns
t_{PHL}	SHIFT IN ↑	IR		20	26	8	30	ns
t_{PLH}	SHIFT IN ↓	IR		16	21	6	25	ns
t_{PLH}§	SHIFT IN ↓	OR		600	800	350	1000	ns
t_{pd}	SHIFT OUT ↓	Q		13	17	4	22	ns
t_{PHL}	SHIFT OUT ↑	OR		23	27	7	33	ns
t_{PLH}	SHIFT OUT ↓	OR		20	24	6	30	ns
t_{PLH}§	SHIFT OUT ↓	IR		600	800	350	1000	ns
t_{PHL}	$\overline{RST}$ ↓	OR		22	26	10	34	ns
t_{PLH}	$\overline{RST}$ ↓	IR		17	21	6	27	ns
t_{PHL}	$\overline{RST}$ ↓	Q		14	17	5	19	ns

† The IR output pulse occurs when the FIFO is full, Shift In is high, and Shift Out is pulsed (see Figure 4).
‡ The OR output pulse occurs when the FIFO is empty, Shift Out is high, and Shift In is pulsed (see Figure 3).
§ Data Throughput or "fall through" times.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION INFORMATION

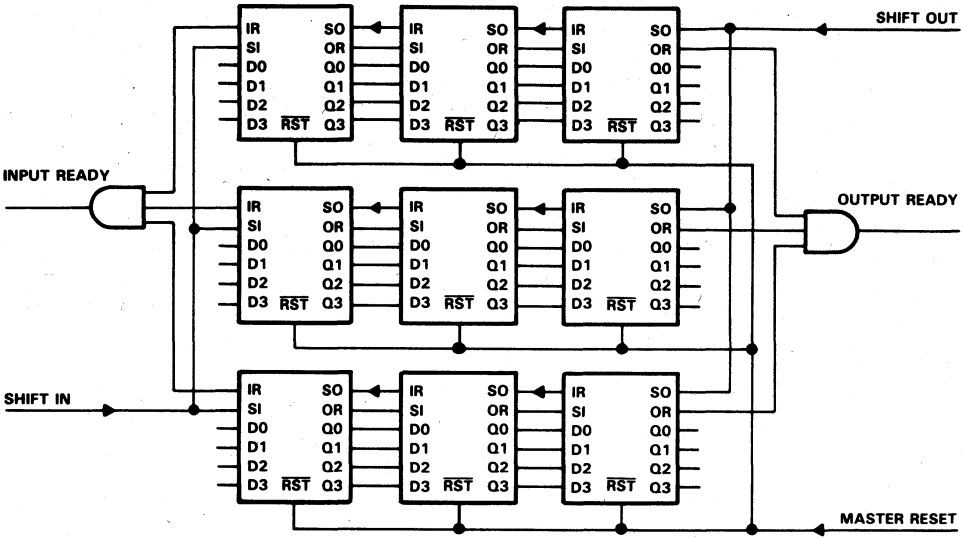


FIGURE 5. 192-WORD BY 12-BIT EXPANSION

OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982 – REVISED MAY 1986

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce DC Loading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

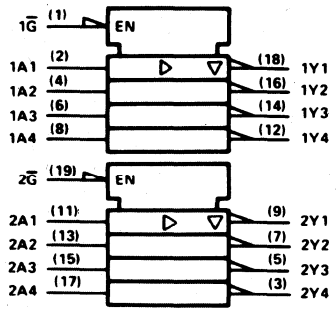
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the ALS/AS241 the designer has a choise of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out and improved fan-in.

The -1 versions of the SN74ALS' parts are identical to their standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

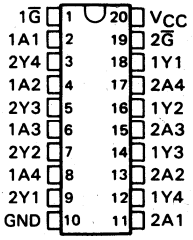
The SN54' family is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74' family is characterized for operation from 0 °C to 70 °C.

logic symbol†

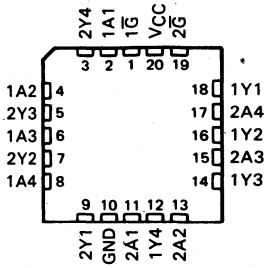


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for DW, J, and N packages.

SN54ALS', SN54AS' ... J PACKAGE
SN74ALS', SN74AS' ... DW OR N PACKAGE
(TOP VIEW)

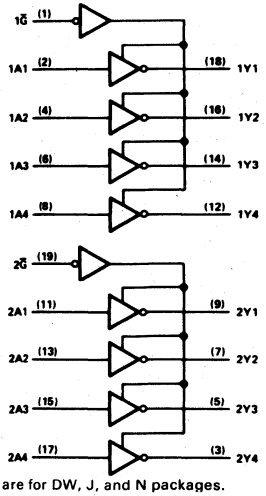


SN54ALS' SN54AS' ... FK PACKAGE
(TOP VIEW)



* $2\overline{G}$ for 'ALS240A, 'AS240

logic diagram (positive logic)



Pin numbers are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS240A . . . . . −55 °C to 125 °C
SN74ALS240A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS240A			SN74ALS240A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

† The 48 mA limit applies only to the −1 versions and only if the V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS240A			SN74ALS240A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
	V_{CC} = 4.75 V,	I_{OL} = 48 mA (-1 versions)							
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O*	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		4	11		4	11	mA
		Outputs low		13	23		13	23	
		Outputs disabled		14	25		14	25	

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
* The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25 °C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS240A	SN54ALS240A		SN74ALS240A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	6	2	22	2	9	ns
t_{PHL}			5	2	11	2	9	
t_{PZH}	$\overline{G}$	Y	9	4	34	5	13	ns
t_{PZL}			10	5	26	5	18	
t_{PHZ}	$\overline{G}$	Y	6	1	15	2	10	ns
t_{PLZ}			7	3	24	3	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS240 . . . . . −55 °C to 125 °C
SN74AS240 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS240			SN74AS240			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS240			SN74AS240			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.27	0.55				V
	V_{CC} = 4.75 V,	I_{OL} = 64 mA					0.31	0.55	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O*	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		11	17		11	17	mA
		Outputs low		51	75		51	75	
		Outputs disabled		24	38		24	38	

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
* The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS240		SN74AS240		
			MIN	MAX	MIN	MAX	
tPLH	A	Y	2	7	2	6.5	ns
tPHL			2	6	2	5.7	
tPZH	$1\overline{G}$	Y	2	7	2	6.4	ns
tPZL			2	9.5	2	9	
tPHZ	$\overline{G}$	Y	2	5.5	2	5	ns
tPLZ			2	12.5	2	9.5	

NOTE 1: Load Circuit and voltage waveforms are shown in Section 1.

SN74ALS241B, SN74AS241, SN54ALS241B, SN54AS241
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982 – REVISED AUGUST 1988

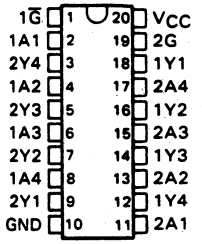
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce DC Loading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

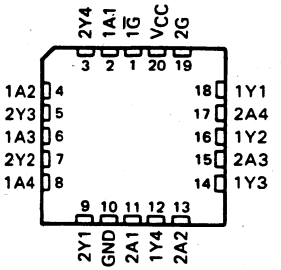
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ALS240 and 'AS240, the designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out and improved fan-in.

The SN54' family is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74' family is characterized for operation from 0 °C to 70 °C.

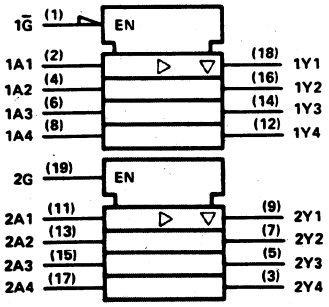
SN54ALS241B, SN54AS241 ... J PACKAGE
SN74ALS241B, SN74AS241 ... D OR N PACKAGE
(TOP VIEW)



SN54ALS241B, SN54AS241 ... FK PACKAGE
(TOP VIEW)

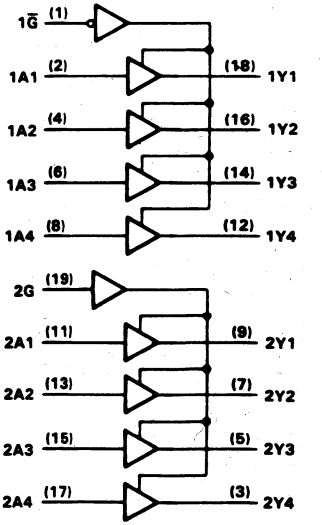


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS241B . . . . . −55 °C to 125 °C
SN74ALS241B . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS241B			SN74ALS241B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24†	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

† The SN74ALS241A-1 can sink 48 mA if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS241B			SN74ALS241B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O*	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		9	17		9	15	mA
		Outputs low		15	28		15	26	
		Outputs disabled		17	32		17	30	

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
* The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_1 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS241B		SN74ALS241B		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	31	3	11	ns
t_{PHL}			1	14	3	10	
t_{PZH}	$1\overline{G}$	Y	5	33	5	21	ns
t_{PZL}			7	27	5	21	
t_{PHZ}	$1\overline{G}$	Y	2	13	2	10	ns
t_{PLZ}			2	32	2	15	
t_{PZH}	2G	Y	7	38	5	21	ns
t_{PZL}			7	30	5	21	
t_{PHZ}	2G	Y	2	17	2	10	ns
t_{PLZ}			3	35	3	15	

switching characteristics SN74ALS241A-1

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, T_A = MIN to MAX†		UNIT
			MIN	MAX	
t_{PLH}	A	Y	3	11	ns
t_{PHL}			3	10	
t_{PZH}	$1\overline{G}$	Y	7	21	ns
t_{PZL}			7	21	
t_{PHZ}	$1\overline{G}$	Y	2	10	ns
t_{PLZ}			3	15	
t_{PZH}	2G	Y	7	21	ns
t_{PZL}			7	21	
t_{PHZ}	2G	Y	2	10	ns
t_{PLZ}			3	15	

† For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions for the applicable type.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS241 . . . . . −55 °C to 125 °C
SN74AS241 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS241			SN74AS241			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

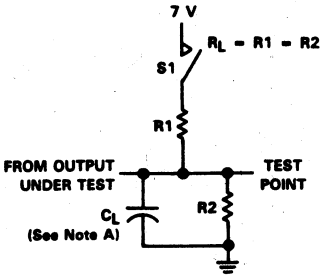
PARAMETER	TEST CONDITIONS		SN54AS241			SN74AS241			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.27	0.55				V
	V_{CC} = 4.75 V,	I_{OL} = 64 mA					0.31	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
I_O*	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		22	35		22	35	mA
		Outputs low		61	90		61	90	
		Outputs disabled		35	56		35	56	

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
* The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

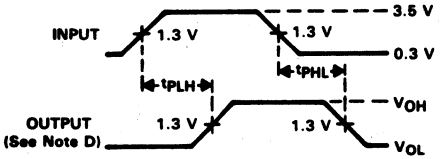
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS241		SN74AS241		
			MIN	MAX	MIN	MAX	
tPLH	A	Y	2	9	2	6.2	ns
tPHL			2	7	2	6.2	
tPZH	$1\overline{G}$	Y	2	10	2	9	ns
tPZL			2	8	2	7.5	
tPHZ	$1\overline{G}$	Y	2	6.5	2	6	ns
tPLZ			2	10.5	2	9	
tPZH	2G	Y	2	11	3	10.5	ns
tPZL			3	9.5	3	8.5	
tPHZ	2G	Y	3	7	3	7	ns
tPLZ			3	12	3	12	

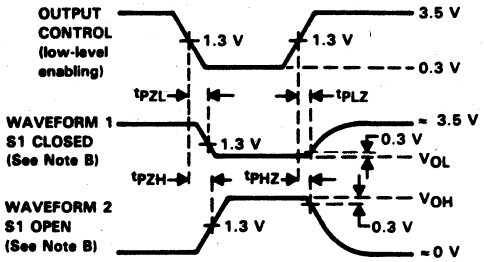
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR
THREE-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay items of 3-state outputs, switch S1 is open.
E. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1

D2661, DECEMBER 1982 – REVISED JULY 1987

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce DC Loading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

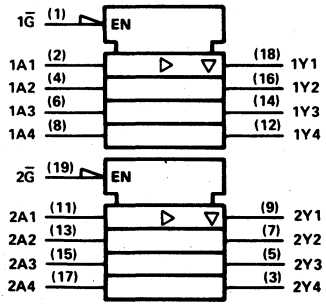
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ALS240A, 'ALS241B, 'AS240, and 'AS241, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{G}$ (active-low input control) inputs, and complementary G and $\overline{G}$ inputs.

The SN74ALS244A-1 is similar to the standard version except that the recommended maximum I_{OL} is increased to 48 milliamperes. There is no -1 version of the SN54ALS244B.

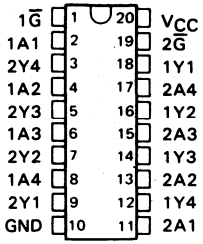
The SN54ALS244B and SN54AS244 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS244B and SN74AS244 are characterized for operation from 0°C to 70°C.

logic symbol†

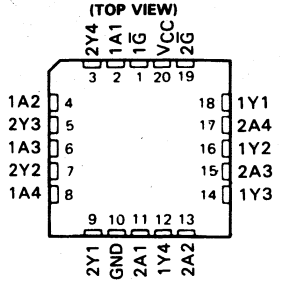


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for DW, J, and N packages.

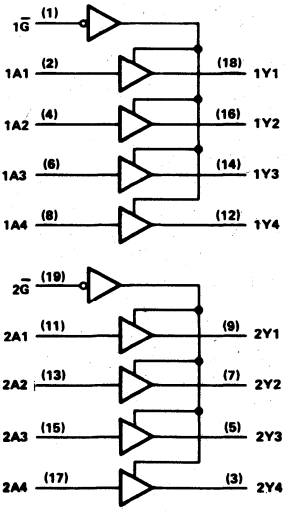
SN54ALS244B, SN54AS244 . . . J PACKAGE
SN74ALS244B, SN74AS244 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS244B, SN54AS244 . . . FK PACKAGE
(TOP VIEW)



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS244B . . . . . −55°C to 125°C
SN74ALS244B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS244B			SN74ALS244B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage						0.8	V
				0.8†				
				0.7‡				
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48§	
T_A	Operating free-air temperature	−55		125	0		70	°C

† Tested at −55°C to 70°C.
‡ Tested at 70°C to 125°C, per MIL-STD-883, method 5005, sub-group 1, 2, and 3. Static tests are performed at 25°C, 125°C, and −55°C.
§ The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS244A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS244B			SN74ALS244B			UNIT
			MIN	TYP¶	MAX	MIN	TYP¶	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 version)	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O#	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	Outputs high		9	15		9	15	mA
		Outputs low		15	24		15	24	
		Outputs disabled		17	27		17	27	

¶ All typical values are at V_{CC} = 5 V, T_A = 25°C.
# The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS244B		SN74ALS244B		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	16	3	10	ns
t_{PHL}			3	12	3	10	
t_{PZH}	$\overline{G}$	Y	1	26	3	20	ns
t_{PZL}			1	24	3	20	
t_{PHZ}	$\overline{G}$	Y	2	10	2	10	ns
t_{PLZ}			1	26	1	13	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

switching characteristics SN74ALS244A-1

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS244A		SN74ALS244A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	13	3	10	ns
t_{PHL}			3	13	3	10	
t_{PZH}	$\overline{G}$	Y	7	25	7	20	ns
t_{PZL}			7	25	7	20	
t_{PHZ}	$\overline{G}$	Y	2	12	2	10	ns
t_{PLZ}			3	18	3	13	

NOTE 1: For load circuit and voltage waveforms see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS244 . . . . . −55°C to 125°C
SN74AS244 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS244			SN74AS244			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS244			SN74AS244			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55				V
	V_{CC} = 4.5 V,	I_{OL} = 64 mA						0.55	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL} $\overline{G}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_{IL} A					−1			−1	
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		22	34		22	34	mA
		Outputs low		60	90		60	90	
		Outputs disabled		34	54		34	54	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

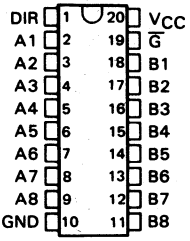
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS244		SN74AS244		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2	9	2	6.2	ns
t_{PHL}			2	7	2	6.2	
t_{PZH}	$\overline{G}$	Y	2	10	2	9	ns
t_{PZL}			2	8	2	7.5	
t_{PHZ}	$\overline{G}$	Y	2	6.5	2	6	ns
t_{PLZ}			2	10.5	2	9	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

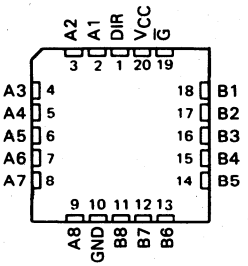
D2661, DECEMBER 1982 – REVISED MAY 1986

- **3-State Outputs Drive Bus Lines Directly**
- **P-N-P Inputs Reduce DC Loading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS245A, SN54AS245 . . . J PACKAGE
SN74ALS245A, SN74AS245 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS245A, SN54AS245 . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

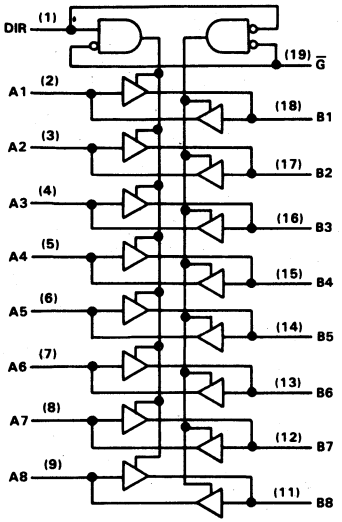
The –1 version of the SN74ALS245A is identical to the standard version except that the recommended maximum I_{OL} is increased to 48 milliamperes. There is no –1 version of the SN54ALS245A.

The SN54ALS245A and SN54AS245 are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS245A and SN74AS245 are characterized for operation from 0°C to 70°C.

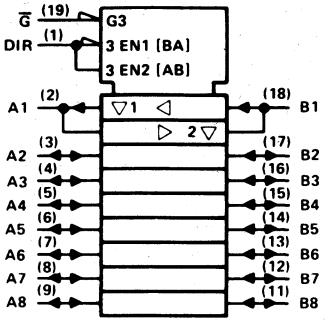
FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS245A . . . . . −55°C to 125°C
SN74ALS245A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS245A			SN74ALS245A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48‡	
T_A	Operating free-air temperature	−55		125	0		70	°C

‡The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS245A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS245A			SN74ALS245A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports‡					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		30	48		30	45	mA
			Outputs low		36	60		36	55	
			Outputs disabled		38	63		38	58	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS245A		SN74ALS245A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	19	3	10	ns
t_{PHL}			1	14	3	10	
t_{PZH}	$\overline{G}$	A or B	2	30	5	20	ns
t_{PZL}			2	29	5	20	
t_{PHZ}	$\overline{G}$	A or B	2	14	2	10	ns
t_{PLZ}			2	30	4	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS245 . . . . . −55°C to 125°C
SN74AS245 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS245			SN74AS245			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS245			SN74AS245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.3	0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.35	0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.4 V			50			20	μA
	A or B ports‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.75			−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		62	97		62	97	mA
			Outputs low		95	143		95	143	
			Outputs disabled		79	123		79	123	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports (Q_A through Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

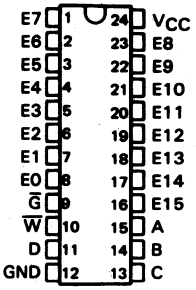
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS245		SN74AS245		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	9.5	2	7.5	ns
t_{PHL}			2	9	2	7	
t_{PZH}	$\overline{G}$	A or B	2	11	2	9	ns
t_{PZL}			2	10.5	2	8.5	
t_{PHZ}	$\overline{G}$	A or B	2	7.5	2	5.5	ns
t_{PLZ}			2	12	2	9.5	

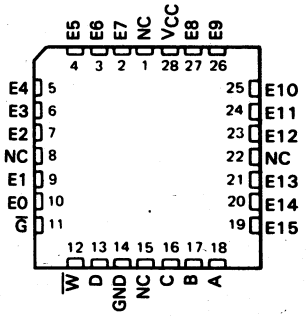
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **4-Line to 1-Line Multiplexer that Can Select 1 and 16 Data Inputs**
- **Applications:**
  Boolean Function Generator
  Parallel-to-Serial Converter
  Data Source Selector
- **Buffered 3-State Bus Driver Inputs Permit Multiplexing from N Lines to One Line**
- **Package Options Include Plastic "Small Outline" Packages, Plastic Chip Carriers, and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS250A . . . JT PACKAGE
SN74AS250A . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS250A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

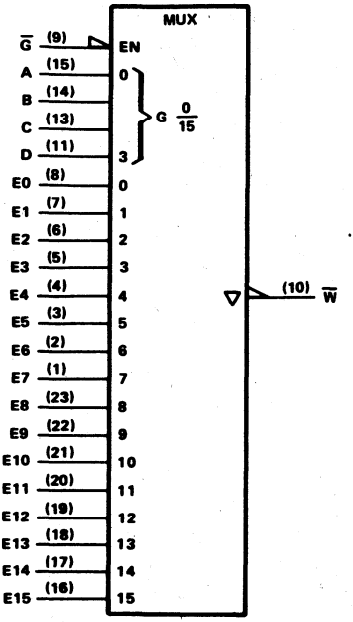
The 'AS250A provides full binary decoding to select one of sixteen data sources with an inverting $\overline{W}$ output. The selected sources are buffered with symmetrical propagation delay times. This reduces the possibility of transients occurring at the output.

A buffered enable output ($\overline{G}$) may be used for n-line-to-one-line cascading. Taking the $\overline{G}$ high will place the output in a high-impedance state. In the high-impedance state, the output neither loads nor drives the bus lines significantly.

The enable ($\overline{G}$) does not affect the internal operations of the data selector/multiplexer. New data can be set up while the outputs are disabled.

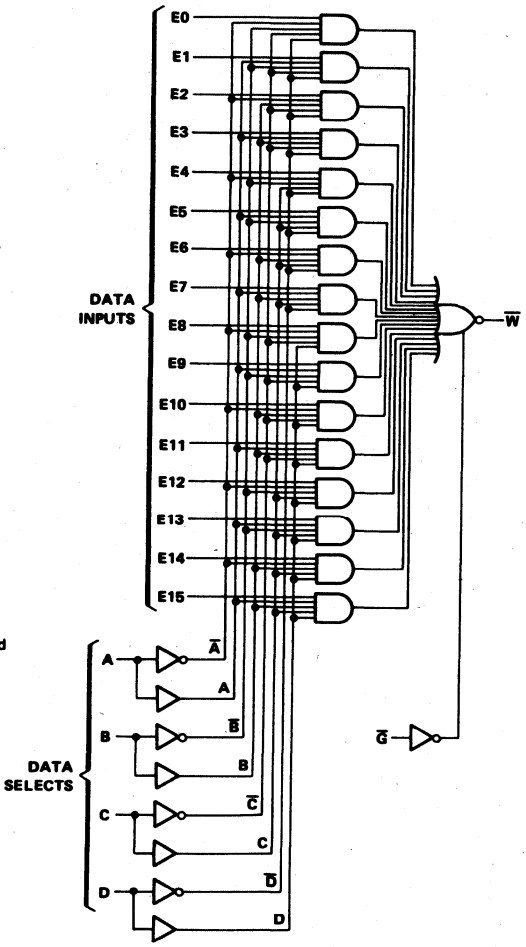
The SN54AS250A is characterized for operation from −55°C to 125°C. The SN74AS250A is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



TEXAS INSTRUMENTS

FUNCTION TABLE

INPUT						OUTPUT
$\overline{G}$	A	B	C	D	EI	$\overline{W}$
L	L	L	L	L	E0	$\overline{E0}$
L	H	L	L	L	E1	$\overline{E1}$
L	L	H	L	L	E2	$\overline{E2}$
L	H	H	L	L	E3	$\overline{E3}$
L	L	L	H	L	E4	$\overline{E4}$
L	H	L	H	L	E5	$\overline{E5}$
L	L	H	H	L	E6	$\overline{E6}$
L	H	H	H	L	E7	$\overline{E7}$
L	L	L	L	H	E8	$\overline{E8}$
L	H	L	L	H	E9	$\overline{E9}$
L	L	H	L	H	E10	$\overline{E10}$
L	H	H	L	H	E11	$\overline{E11}$
L	L	L	H	H	E12	$\overline{E12}$
L	H	L	H	H	E13	$\overline{E13}$
L	L	H	H	H	E14	$\overline{E14}$
L	H	H	H	H	E15	$\overline{E15}$
H	X	X	X	X	X	Z

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS250A . . . . . −55°C to 125°C
SN74AS250A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		54AS250A			74AS250A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−15			−15	mA
I_{OL}	Low-level output current			48			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		54AS250A			74AS250A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.3		2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5		0.35	0.5	V
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		26	42		26	42	mA
		Outputs low		31	50		31	50	
		Outputs disabled		30	48		30	48	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

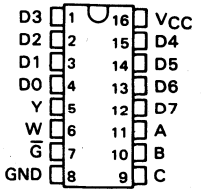
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN TO MAX§				UNIT
			54AS250A		74AS250A		
			MIN	MAX	MIN	MAX	
t_{PLH}	DATA	$\overline{W}$	2	9.5	2	7.5	ns
t_{PHL}			2	8.5	2	7	
t_{PLH}	SELECT	$\overline{W}$	4	15.5	4	13	ns
t_{PHL}			4	12	4	10.5	
t_{PZH}	$\overline{G}$	$\overline{W}$	2	7.5	2	7	ns
t_{PZL}			2	10	2	9	
t_{PHZ}	$\overline{G}$	$\overline{W}$	1.5	6.5	1.5	6	ns
t_{PLZ}			2	8.5	2	6.5	

§For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982 – REVISED MAY 1986

- **Three-State Version of 'ALS151**
- **Three-State Outputs Interface Directly with System Bus**
- **Performs Parallel-to-Serial Conversion**
- **Complementary Outputs Provide True and Inverted Data**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS251 . . . J PACKAGE
SN74ALS251 . . . D OR N PACKAGE
(TOP VIEW)



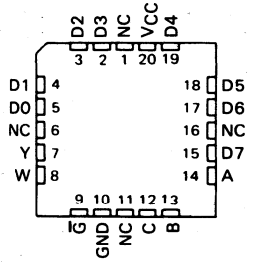
description

These data selectors/multiplexers contain full binary decoding to select one-of-eight data sources and feature strobe-controlled complementary three-state outputs.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the signal enabled output will drive the bus line to a high or low logic level. Both outputs are controlled by the strobe ($\overline{G}$). The outputs are disabled when $\overline{G}$ is high.

The SN54ALS251 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS251 is characterized for operation from 0°C to 70°C.

SN54ALS251 . . . FK PACKAGE
(TOP VIEW)



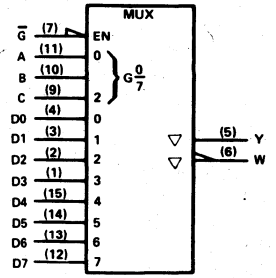
NC – No internal connection.

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	$\overline{G}$		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

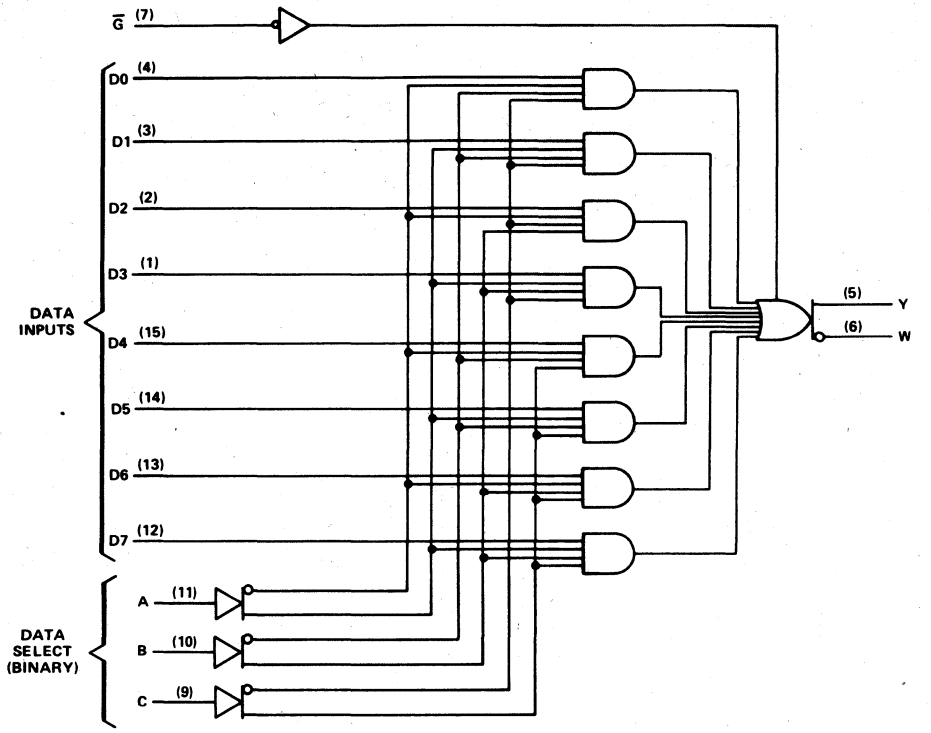
D0, D1 . . . D7 = the level of the respective D input

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS251 . . . . . −55°C to 125°C
SN74ALS251 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS251			SN74ALS251			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS251			SN74ALS251			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	$V_{CC}-2$			$V_{CC}-2$			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	Enabled	V_{CC} = 5.5 V,	Inputs at Gnd.		7	10		7	10	mA
	Disabled	V_{CC} = 5.5 V,	Inputs at 4.5 V		9.4	14		9.4	14	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS251		SN74ALS251		
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B or C	Y	1	21	5	18	ns
t_{PHL}			8	34	8	24	
t_{PLH}	A, B or C	W	8	38	8	24	ns
t_{PHL}			7	26	7	23	
t_{PLH}	Any D	Y	2	15	2	10	ns
t_{PHL}			3	23	3	15	
t_{PLH}	Any D	W	3	25	3	15	ns
t_{PHL}			3	20	3	15	
t_{PZH}	$\overline{G}$	Y	3	21	3	15	ns
t_{PZL}			3	19	3	15	
t_{PZH}	$\overline{G}$	W	3	21	3	15	ns
t_{PZL}			3	19	3	15	
t_{PHZ}	$\overline{G}$	Y	2	12	2	10	ns
t_{PLZ}			1	18	1	10	
t_{PHZ}	$\overline{G}$	W	2	12	2	10	ns
t_{PLZ}			1	18	1	10	

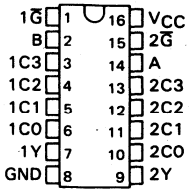
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN74ALS253, SN74AS253, SN54ALS253
DUAL 1-OF-4 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

D2661, APRIL 1982 – REVISED MAY 1986

- **Three-State Versions of 'ALS153 and 'AS153**
- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS253 . . . J PACKAGE
SN74ALS253, SN74AS253 . . . D OR N PACKAGE
(TOP VIEW)



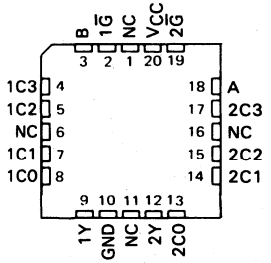
description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$). The output is disabled when its strobe is high.

The SN54ALS253 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS253 and SN74AS253 are characterized for operation from 0°C to 70°C.

SN54ALS253 . . . FK PACKAGE
(TOP VIEW)



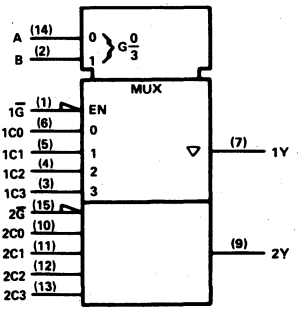
NC – No internal connection

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.

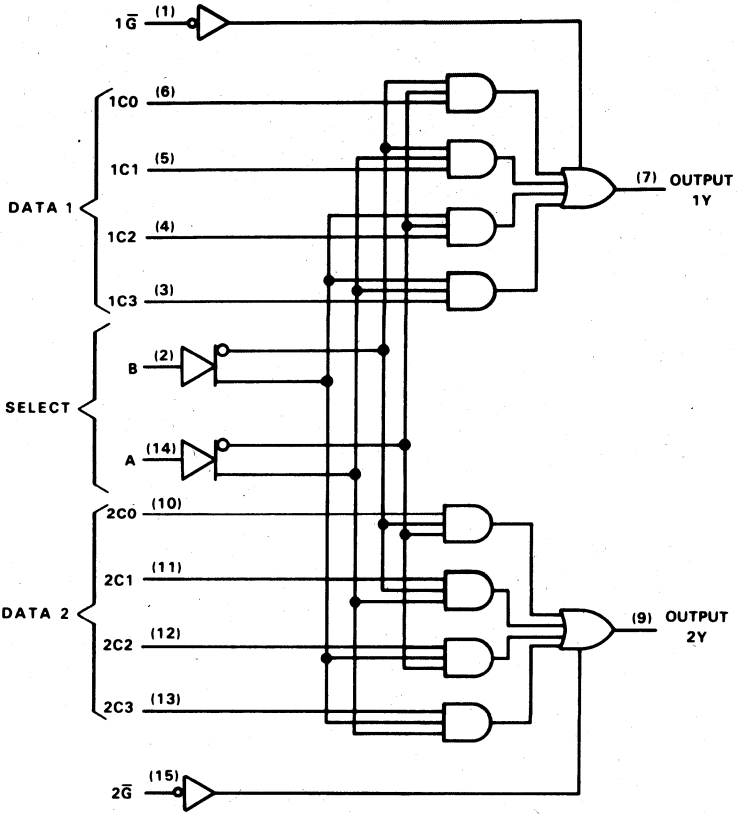
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

TEXAS INSTRUMENTS

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS253 . . . . . −55°C to 125°C
SN74ALS253, SN74AS253 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS253			SN74ALS253			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS253			SN74ALS253			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs enabled		6.5	12		6.5	12	mA
		Outputs disabled		7.5	14		7.5	14	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS253		SN74ALS253		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	5	30	5	21	ns
t_{PHL}			5	27	5	21	
t_{PLH}	Data (Any C)	Any Y	2	15	2	10	ns
t_{PHL}			3	18	3	14	
t_{PZH}	$\overline{G}$	Any Y	3	20	3	14	ns
t_{PZL}			2	19	4	16	
t_{PHZ}	$\overline{G}$	Any Y	2	12	2	10	ns
t_{PLZ}			2	18	2	14	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN74AS253			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74AS253			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA				
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50	µA
I_I	A, B	V_{CC} = 5.5 V,	V_I = 7 V			0.2	mA
	All others					0.1	
I_{IH}	A, B	V_{CC} = 5.5 V,	V_I = 2.7 V			40	µA
	All others					20	
I_{IL}	A, B	V_{CC} = 5.5 V,	V_I = 0.4 V			−1	mA
	All others					−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		18	29	mA
			Outputs low		20	32	
			Outputs disabled		21	33	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			SN74AS253		
			MIN	MAX	
t_{PLH}	A or B	Y	4	13.5	ns
t_{PHL}			4	11.5	
t_{PLH}	Data (Any C)	Y	3	7.5	ns
t_{PHL}			3	8	
t_{PZH}	G	Any Y	4	12.5	ns
t_{PZL}			4	11.5	
t_{PHZ}	G	Any Y	2	6	ns
t_{PLZ}			2	7	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

D2661, APRIL 1982 – REVISED APRIL 1987

- **Three-State Outputs Interface Directly with System Bus**
- **Provides Bus Interface from Multiple Sources in High-Performance Systems**
- **Dependable Texas Instruments Quality and Reliability**

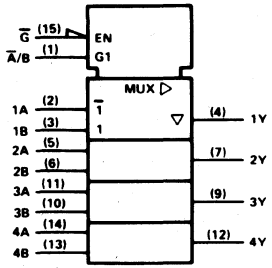
description

These devices are designed to multiplex signals from four-bit data sources to four-output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output control pin (G) is at a high-logic level.

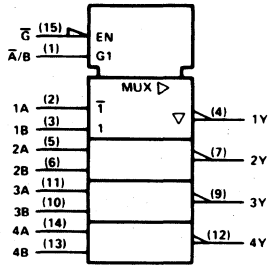
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

logic symbol†

'ALS257, 'AS257



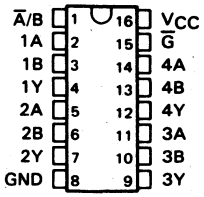
'ALS258, 'AS258



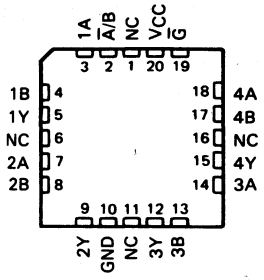
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

SN54ALS'...J PACKAGE
SN74ALS', SN74AS'...D OR N PACKAGE
(TOP VIEW)



SN54ALS'...FK PACKAGE
(TOP VIEW)



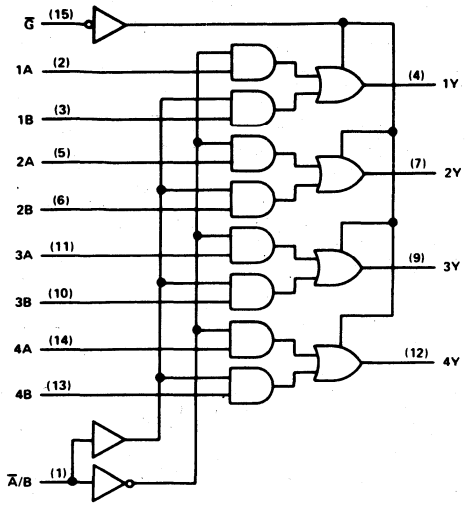
NC – No internal connection

FUNCTION TABLE

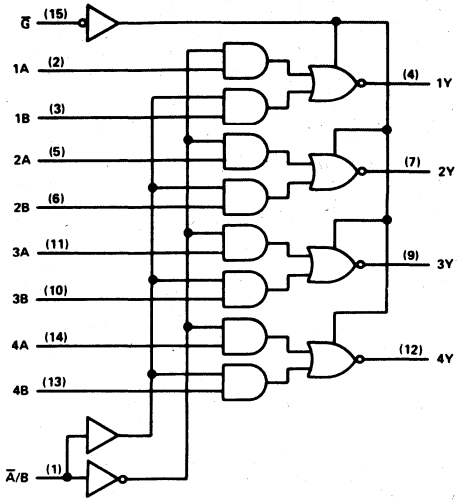
INPUTS				OUTPUT Y	
OUTPUT CONTROL $\overline{G}$	SELECT $\overline{A}/B$	DATA A	DATA B	'ALS257 'AS257	'ALS258 'AS258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

logic diagram (positive logic)

'ALS257, 'AS257



'ALS258, 'AS258



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS' . . . . . −55°C to 125°C
SN74ALS', SN74AS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS257 SN54ALS258			SN74ALS257 SN74ALS258			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS257 SN54ALS258			SN74ALS257 SN74ALS258			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS257	V_{CC} = 5.5 V	Outputs high		3	6		3	6	mA
			Outputs low		8	12		8	12	
			Outputs disabled		9	14		9	14	
	'ALS258	V_{CC} = 5.5 V	Outputs high		2.5	4		2.5	4	
			Outputs low		7	11		7	11	
			Outputs disabled		8	13		8	13	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS257 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS257		SN74ALS257		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	2	12	2	10	ns
t_{PHL}			2	14	2	12	
t_{PLH}	$\overline{A}$/B	Any Y	7	21	7	18	ns
t_{PHL}			6	25	6	22	
t_{PZH}	$\overline{G}$	Any Y	4	20	4	16	ns
t_{PZL}			5	22	5	18	
t_{PHZ}	$\overline{G}$	Any Y	2	12	2	10	ns
t_{PLZ}			4	35	3	15	

'ALS258 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS258		SN74ALS258		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	1	12	2	8	ns
t_{PHL}			2	9	2	7	
t_{PLH}	$\overline{A}$/B	Any Y	5	28	5	25	ns
t_{PHL}			8	25	8	20	
t_{PZH}	$\overline{G}$	Any Y	5	20	5	18	ns
t_{PZL}			5	21	5	18	
t_{PHZ}	$\overline{G}$	Any Y	2	12	2	10	ns
t_{PLZ}			5	37	4	18	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN74AS257 SN74AS258			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74AS257 SN74AS258			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA				
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50	µA
I_I	A, B or $\overline{G}$	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
	$\overline{A}/B$					0.2	
I_{IH}	A, B or $\overline{G}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	$\overline{A}/B$					40	
I_{IL}	A, B or $\overline{G}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5	mA
	$\overline{A}/B$					−1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	'AS257	V_{CC} = 5.5 V	Outputs high		12.1	19.7	mA
			Outputs low		19	30.6	
			Outputs disabled		19.7	31.9	
	'AS258	V_{CC} = 5.5 V	Outputs high		8.4	13.5	
			Outputs low		15.2	24.6	
			Outputs disabled		15.5	25.2	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS257 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			SN74AS257		
			MIN	MAX	
t_{PLH}	A or B	Any Y	1	5.5	ns
t_{PHL}			1	6	
t_{PLH}	$\overline{A}$/B	Any Y	2	11	ns
t_{PHL}			2	10	
t_{PZH}	$\overline{G}$	Any Y	2	7.5	ns
t_{PZL}			2	9.5	
t_{PHZ}	$\overline{G}$	Any Y	1.5	6.5	ns
t_{PLZ}			2	7	

'AS258 switching characteristics (see Note 1)

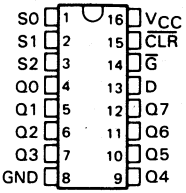
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			SN74AS258		
			MIN	MAX	
t_{PLH}	A or B	Any Y	1	5	ns
t_{PHL}			1	4	
t_{PLH}	$\overline{A}$/B	Any Y	2	9.5	ns
t_{PHL}			2	10	
t_{PZH}	$\overline{G}$	Any Y	2	8	ns
t_{PZL}			2	10	
t_{PHZ}	$\overline{G}$	Any Y	1.5	6	ns
t_{PLZ}			2	6.5	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

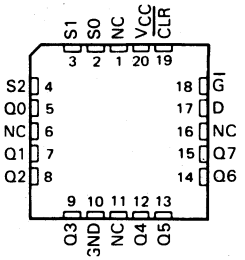
D2661, DECEMBER 1982 – REVISED MAY 1986

- **8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion with Storage**
- **Asynchronous Parallel Clear**
- **Active High Decoder**
- **Enable/Disable Input Simplifies Expansion**
- **Expandable for N-Bit Applications**
- **Four Distinct Functional Modes**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS259 . . . J PACKAGE
SN74ALS259 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS259 . . . FK PACKAGE
(TOP VIEW)



NC No internal connection

description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, enable $\overline{G}$ should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

The SN54ALS259 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS259 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

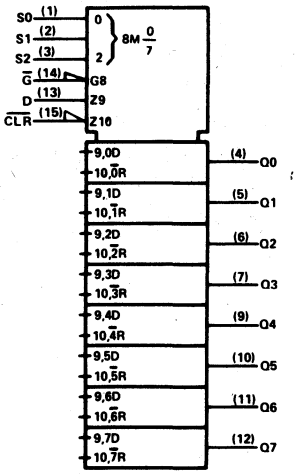
INPUTS $\overline{CLR}$	INPUTS $\overline{G}$	OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
H	L	D	Q_{iO}	Addressable Latch
H	H	Q_{iO}	Q_{iO}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

D = the level at the data input.
Q_{iO} = the level of Q_i (i = Q, 1, . . . 7, as appropriate) before the indicated steady-state input conditions were established.

LATCH SELECTION TABLE

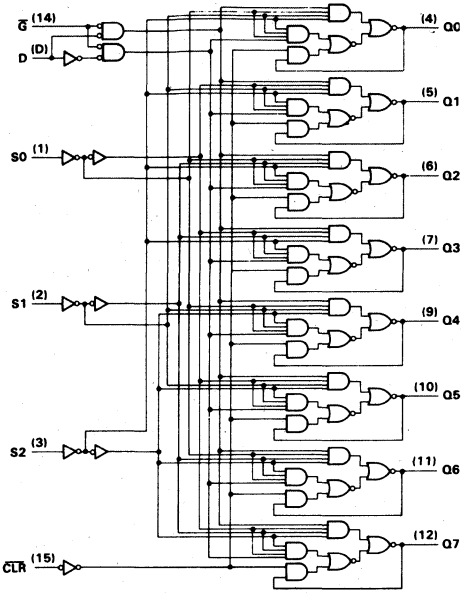
SELECT INPUTS S2	S1	S0	LATCH ADDRESSED
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS259 . . . . . −55°C to 125°C
SN74ALS259 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS259			SN74ALS259			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
t_w	Pulse duration	$\overline{G}$ low	20			15			ns
		$\overline{CLR}$ low	10			10			
t_{su}	Setup time	Data before $\overline{G}$↑	20			15			ns
		Address before $\overline{G}$↑	20			15			
t_h	Hold time	Data after $\overline{G}$↑	0			0			ns
		Address after $\overline{G}$↑	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

TEXAS INSTRUMENTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS259			SN74ALS259			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			14	22		14	22	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS259 switching characteristics (see Note 1)

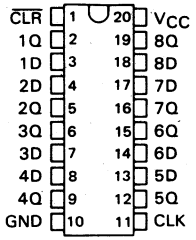
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS259	SN54ALS259		SN74ALS259		
			TYP	MIN	MAX	MIN	MAX	
t_{PHL}	Clear	Any Q	8	2	15	2	12	ns
t_{PLH}	Data	Any Q	10	4	22	4	19	ns
t_{PHL}			8	2	15	2	12	
t_{PLH}	Address	Any Q	15	4	26	4	22	ns
t_{PHL}			8	2	15	2	12	
t_{PLH}	Enable	Any Q	13	4	22	4	20	ns
t_{PHL}			8	2	16	2	13	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

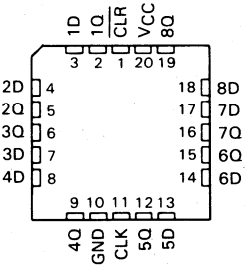
D2661, APRIL 1982 – REVISED MAY 1986

- Contains Eight Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-FLop
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS273 . . . J PACKAGE
SN74ALS273 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS273 . . . FK PACKAGE
(TOP VIEW)



description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

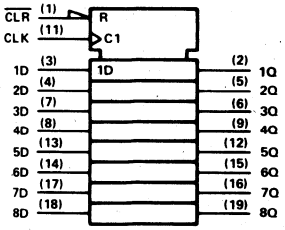
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The SN54ALS273 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS273 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

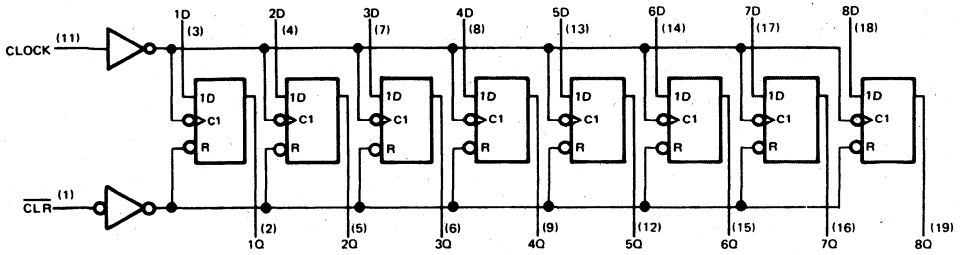
INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS273 . . . . . −55 °C to 125 °C
SN74ALS273 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS273			SN74ALS273			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		30	0		35	MHz
t_w	Pulse duration	$\overline{CLR}$ low	10			10			ns
		CLK high	16.5			14			
		CLK low	16.5			14			
t_{su}	Setup time before CLK↑	Data	10			10			ns
		Clear inactive state	15			15			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS273			SN74ALS273			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V			11	20		11	20	mA
I_{CCL}	V_{CC} = 5.5 V			19	29		19	29	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

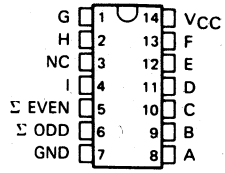
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS273		SN74ALS273		
			MIN	MAX	MIN	MAX	
f_{max}			30		35		MHz
t_{PHL}	$\overline{CLR}$	Any Q	4	24	4	18	ns
t_{PLH}	CLK	Any Q	2	20	2	12	ns
t_{PHL}			3	17	3	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, DECEMBER 1982 – REVISED MAY 1986

- **Generates Either Odd or Even Parity for Nine Data Lines**
- **Cascadable for n-Bits Parity**
- **Can Be Used to Upgrade Existing Systems Using MSI Parity Circuits**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS280, SN74AS280 . . . D OR N PACKAGE
(TOP VIEW)



description

These universal, monolithic, nine-bit parity generators/checkers utilize Advanced Schottky high-performance circuitry and feature odd and even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading.

These devices can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker. Although the 'ALS280 and 'AS280 are implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3. This permits the 'ALS280 and 'AS280 to be substituted for the '180 in existing designs to produce an identical function even if the devices are mixed with existing '180's.

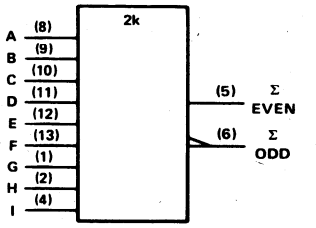
All 'AS280 inputs are buffered to lower the drive requirements.

The SN74' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

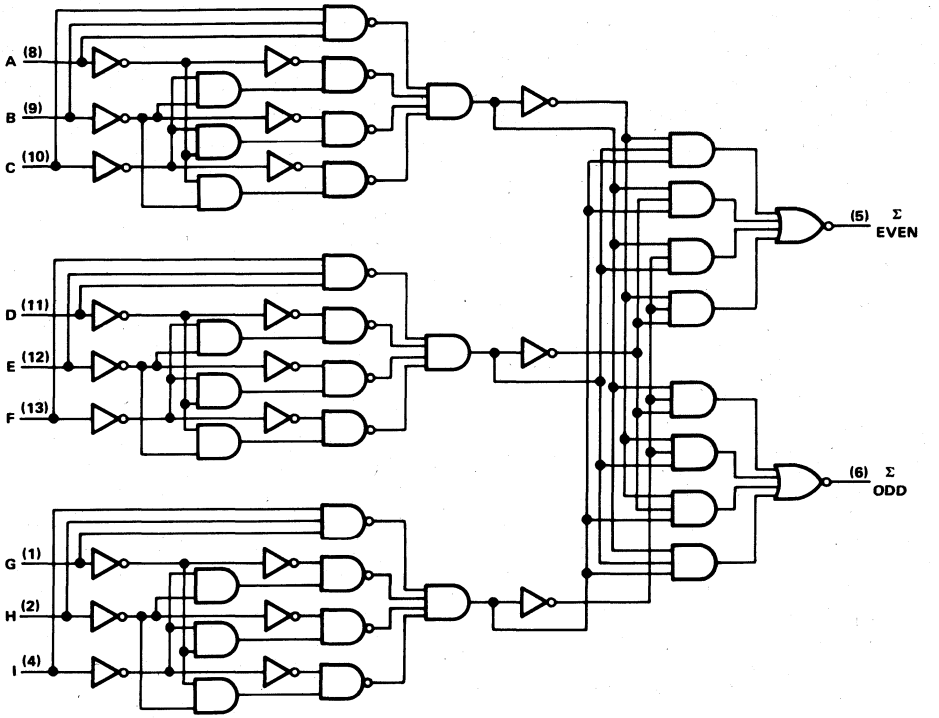
NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0,2,4,6,8	H	L
1,3,5,7,9	L	H

logic symbol†



† This symbol is an accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D and N packages.

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN74ALS280 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74ALS280			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−2.6	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS280			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA				
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			10	16	mA

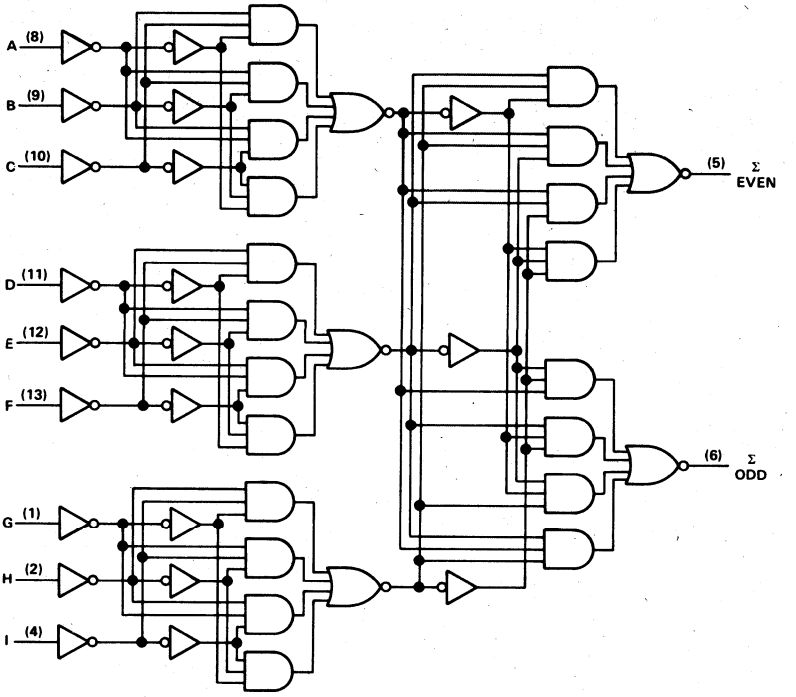
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX		UNIT
			'ALS280	SN74ALS280		
			TYP	MIN	MAX	
t_{PLH}	Any	∑ Even	12	3	20	ns
t_{PHL}			12	3	20	
t_{PLH}	Any	∑ Odd	12	3	20	ns
t_{PHL}			13	4	22	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN74AS280 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74AS280			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−2	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74AS280			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			25	35	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

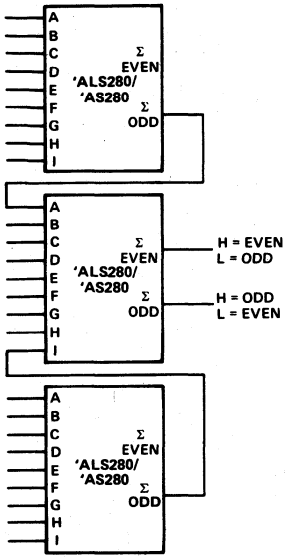
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX		UNIT
			SN74AS280		
			MIN	MAX	
t_{PLH}	Any	∑ Even	3	12	ns
t_{PHL}			3	11	
t_{PLH}	Any	∑ Odd	3	12	ns
t_{PHL}			3	11.5	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

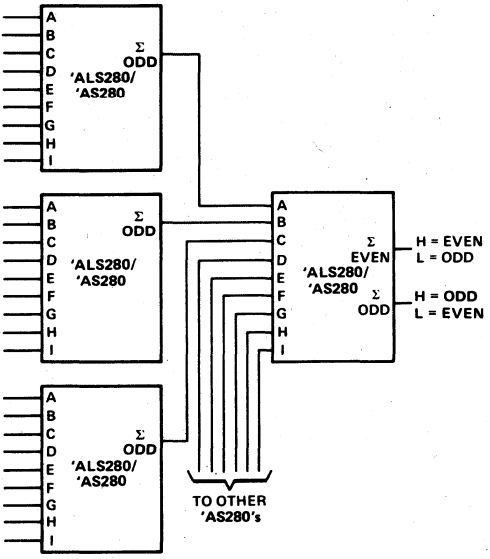
25-LINE PARITY/GENERATOR CHECKER



Three 'ALS280/'AS280 can be used to implement a 25-line parity generator/checker.

As an alternative, the Σ ODD outputs of two or three parity generators/checkers can be decoded with a 2-input ('S86 or 'LS86) or 3-input ('S135) exclusive-OR gate for 18- or 27-line parity applications.

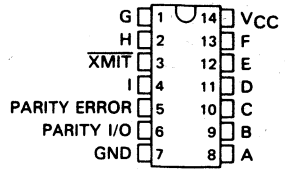
81-LINE PARITY/GENERATOR CHECKER



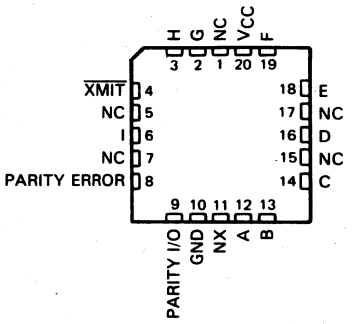
Longer word lengths can be implemented by cascading 'ALS280/'AS280. As shown here, parity can be generated for word lengths up to 81 bits.

- **Generates Either Odd or Even Parity for Nine Data Lines**
- **Cascadable for n-Bits Parity**
- **Direct Bus Connection for Parity Generation or for Checking by Using the Parity I/O Port**
- **Glitch-Free Bus During Power Up/Down**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS286 . . . J PACKAGE
SN74AS286 . . . D OR N PACKAGE
(TOP VIEW)



SN54AS286 . . . FK PACKAGE
(TOP VIEW)



NC No internal connection

description

The SN54AS286 and SN74AS286 universal nine-bit parity generators/checkers feature a local output for parity checking and a 48-milliampere bus-driving parity I/O port for parity generation/checking. The word-length capability is easily expanded by cascading.

The $\overline{\text{XMIT}}$ control input is implemented specifically to accommodate cascading. When $\overline{\text{XMIT}}$ is low the parity tree is disabled and PE will remain at a high logic level regardless of the input levels. When $\overline{\text{XMIT}}$ is high the parity tree is enabled. The Parity Error output will indicate a parity error when either an even number of inputs (A through I) are high and Parity I/O is forced to a low logic level, or when an odd number of inputs are high and Parity I/O is forced to a high logic level.

The I/O control circuitry was designed so that the I/O port will remain in the high-impedance state during power-up or power-down to prevent bus glitches.

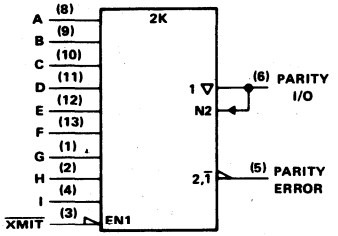
The SN54AS286 is characterized for operation over the full military range of −55°C to 125°C. The SN74AS286 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

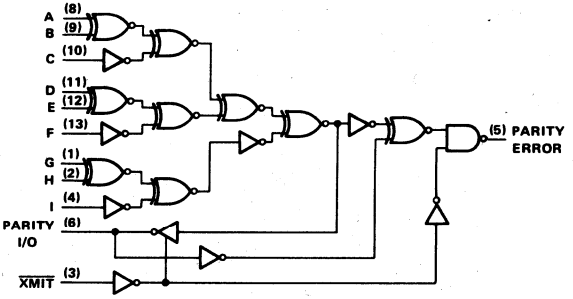
NUMBER OF INPUTS (A THRU I) THAT ARE HIGH	$\overline{XMIT}$	PARITY I/O	PARITY ERROR
0, 2, 4, 6, 8	l	H	H
1, 3, 5, 7, 9	l	L	H
0, 2, 4, 6, 8	h	h	H
	h	l	L
1, 3, 5, 7, 9	h	h	L
	h	l	H

h — high input level l — low input level
H — high output level L — low output level

logic symbol†



logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS286 . . . . . −55°C to 125°C
SN74AS286 . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 140°C

recommended operating conditions

			SN54AS286			SN74AS286			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	Parity error			−2			−2	mA
		Parity I/O			−12			−15	
I_{OL}	Low-level output current	Parity error			20			20	mA
		Parity I/O			32			48	
T_A	Operating free-air temperature		−55		125	0		70	°C

TEXAS INSTRUMENTS

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS286			SN74AS286			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	Parity I/O	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	2.9		2.4	3		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4			
V_{OL}	Parity error	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
	Parity I/O	V_{CC} = 4.5 V,	I_{OL} = 32 mA			0.5				
		V_{CC} = 4.5 V,	I_{OL} = 48 mA						0.5	
I_I	Parity I/O	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	All other inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	
I_{IH}	Parity I/O‡	V_{CC} = 5.5 V,	V_I = 2.7 V			50			50	μA
	All other inputs					20			20	
I_{IL}	Parity I/O‡	V_{CC} = 5.5 V,	V_I = 0.4 V			0.5			−0.5	mA
	All other inputs					0.5			−0.5	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	Transmit	V_{CC} = 5.5 V			30	43		30	43	mA
	Receive				35	50		35	50	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS286		SN74AS286		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any A thru I	Parity I/O	3	17	3	15	ns
t_{PHL}			3	15	3	14	
t_{PLH}	Any A thru I	Parity error	3	20	3	16.5	ns
t_{PHL}			3	18	3	16.5	
t_{PLH}	Parity I/O	Parity error	3	10	3	9	ns
t_{PHL}			3	10	3	9	
t_{PZH}	$\overline{XMIT}$	Parity I/O	3	14	3	13	ns
t_{PZL}			3	17	3	16	
t_{PHZ}			3	13	3	11.5	
t_{PLZ}			3	11	3	10	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

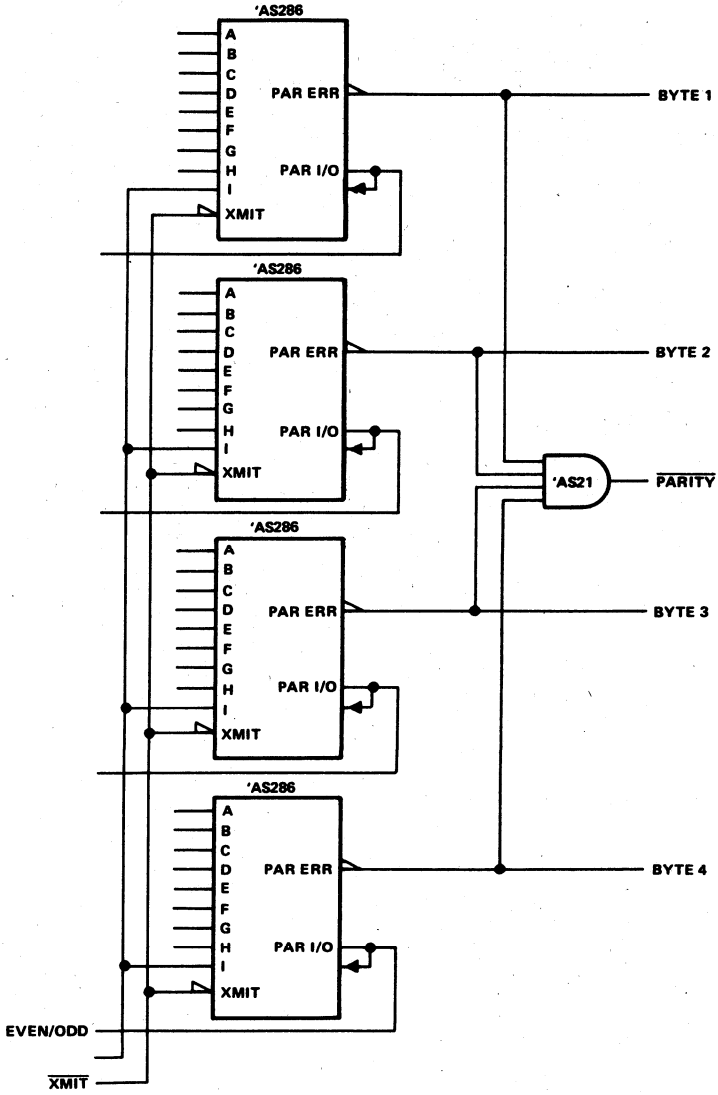


FIGURE 1. 32-BIT PARITY GENERATOR/CHECKER

Figure 1 shows a 32-bit parity generator/checker with output polarity-switching, parity error detection, and parity on every byte.

TYPICAL APPLICATION DATA

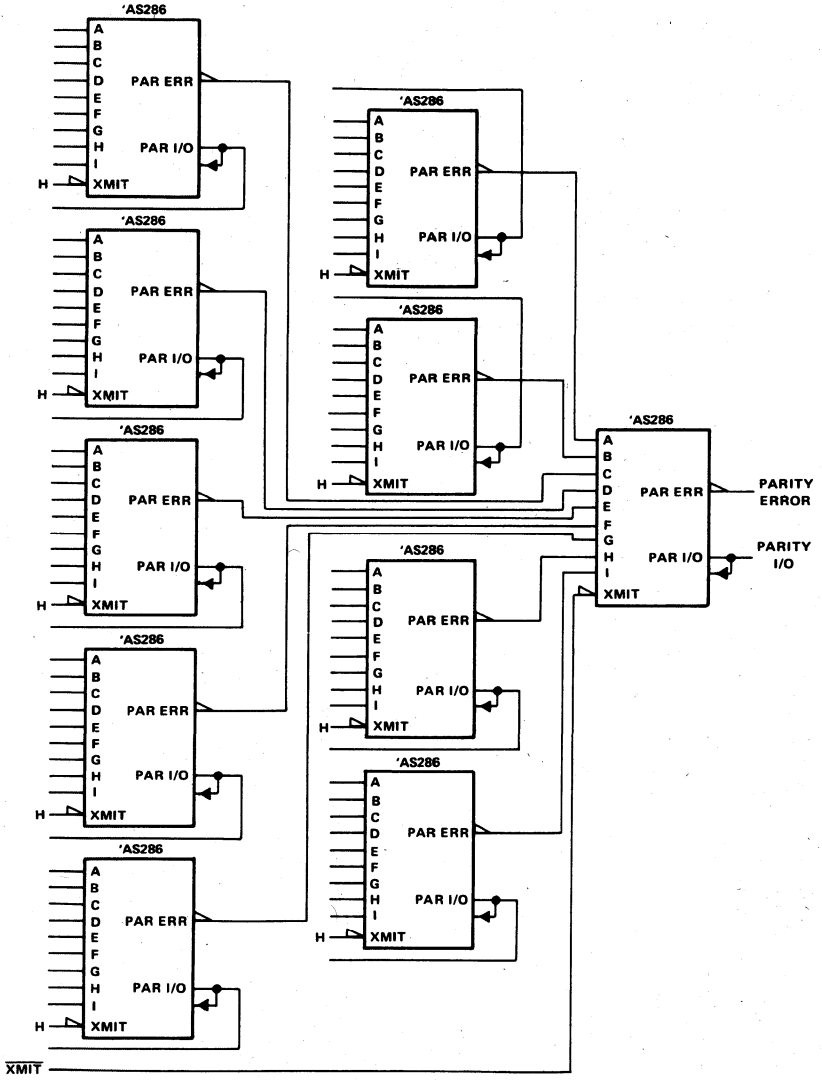


FIGURE 2. 90-BIT PARITY GENERATOR/CHECKER WITH PARITY ERROR DETECTION

In Figure 2, a 90-bit parity generator checker with the $\overline{\text{XMIT}}$ on the last stage is available for use with parity detection.

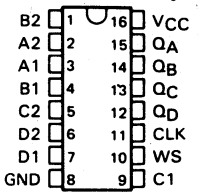
D2661, DECEMBER 1983 – REVISED MAY 1986

- **Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock**
- **Applications:**
  Dual Source for Operands and Constants in Arithmetic Processor; Can Release Processor Register Files for Acquiring New Data

  Implements Separate Registers Capable of Parallel Exchange of Contents, yet Retains External Load Capability

  Has Universal-Type Register for Implementing Various Shift Patterns, including Compound Left-Right Capability
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74AS298 . . . D OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
a1, a2, etc. = the level of steady-state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc. entered on the most-recent ↓ transition of the clock input.

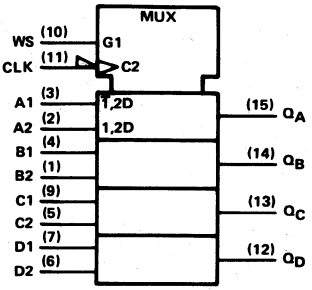
description

This quadruple two-input multiplexer with storage provides essentially the equivalent functional capabilities of two separate MSI functions ('AS157 and 'AS175) in a single 16-pin package.

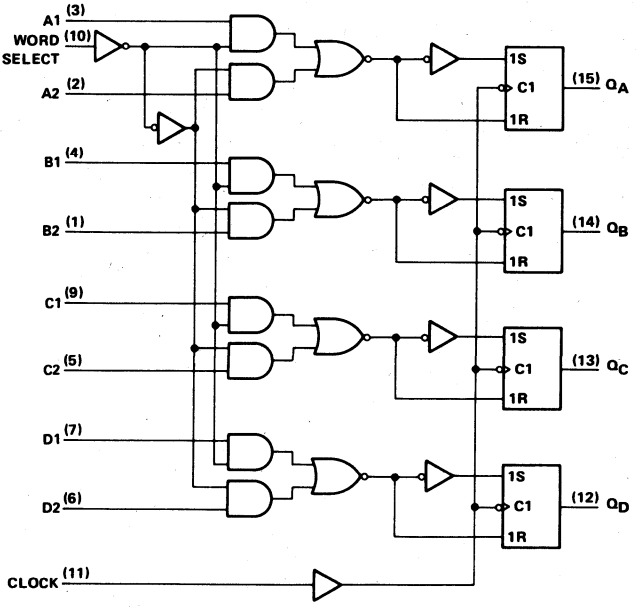
When the word-select (WS) input is low, Word 1 (A1, B1, C1, D1 is applied to the flip-flops. A high input to the word-select (WS) will cause the selection of Word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.

The SN74AS298 is characterized for operation from 0°C to 70°C.

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN74AS298 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN74AS298			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				20	mA
f_{clock}	Clock frequency		0		100	MHz
t_w	Pulse duration, CLK high or low		5			ns
t_{su}	Setup time before CLK ↓	Data	4.5			ns
		Word Select	13			
t_h	Hold time, data after CLK ↓	Data	3.5			ns
		Word Select	1			
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74AS298			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	WS	V_{CC} = 5.5 V,	V_I = 2.7 V			40	μA
	All other					20	
I_{IL}	WS	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.75	mA
	All other					−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CCH}		V_{CC} = 5.5 V			21	33	mA
I_{CCL}		V_{CC} = 5.5 V			22	36	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

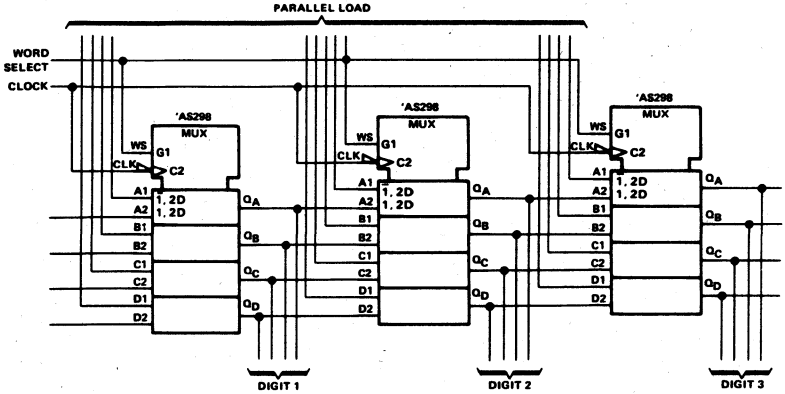
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX		UNIT
			SN74AS298		
			MIN	MAX	
f_{max}			100		MHz
t_{PLH}	CLK	Q	2	9	ns
t_{PHL}			1	11	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

This versatile multiplexer/register can be connected to operate as a shift register that can shift N-places in a single clock pulse.

The following figure illustrates a BCD shift register that will shift an entire 4-bit BCD digit in one clock pulse.



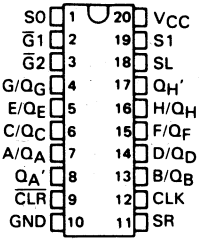
When the word-select input is high and the registers are clocked, the contents of register 1 is transferred (shifted) to register 2, etc. In effect, the BCD digits are shifted one position. In addition, this application retains a parallel-load capability which means that new BCD data can be entered in the entire register with one clock pulse. This arrangement can be modified to perform the shifting of binary data for any number of bit locations.

8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

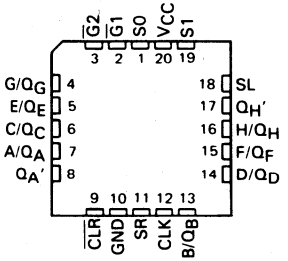
D2661, DECEMBER 1982 – REVISED MAY 1986

- **Multiplexed I/O Ports Provides Improved Bit Density**
- **Four Modes of Operation: Hold (Store), Shift Right, Shift Left, and Load Data**
- **Operates with Outputs Enabled or at High Impedance**
- **3-State Outputs Drive Bus Lines Directly**
- **Can Be Cascaded for N-Bit Word Lengths**
- **'ALS299 Has Direct Overriding Clear**
- **'ALS323 Has Synchronous Clear**
- **Application:**
  Stacked or Push-Down Registers, Buffer Storage, and Accumulator Registers
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS' . . . J PACKAGE
SN74ALS', SN74AS' . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS' . . . FK PACKAGE
(TOP VIEW)



description

These eight-bit universal registers feature multiplexed I/O ports to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines S0 and S1 high. This places the three-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs asynchronously on 'ALS299 and synchronously on 'ALS323 when $\overline{CLR}$ is low. Taking either of the output controls, $\overline{G1}$ or $\overline{G2}$ high disables the outputs but this has no effect on clearing, shifting, or storage of data.

The SN54' family is characterized for operation over the full military range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

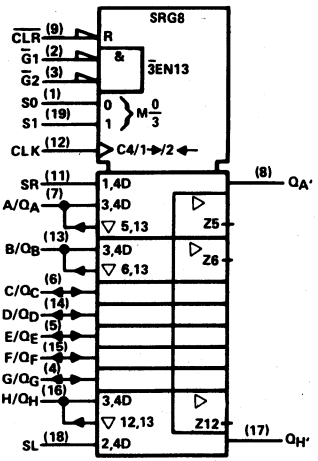
FUNCTION TABLE

MODE	INPUTS								I/O PORTS								OUTPUTS	
	$\overline{CLR}$	S1	S0	OUTPUT CONTROL $\overline{G1}$	OUTPUT CONTROL $\overline{G2}$	CLK	SL	SR	A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	Q_A'	Q_H'
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
('ALS299)	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
('AS299)	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Clear	L	X	L	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
('ALS323)	L	L	X	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
('AS323)	L	H	H	X	X	↑	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

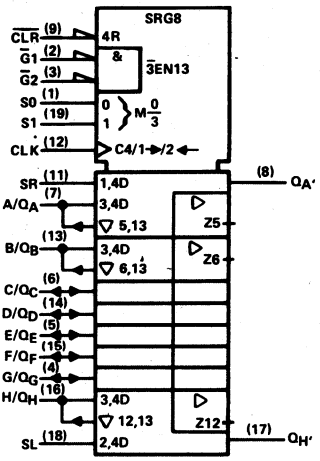
When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

logic symbols†

'ALS299



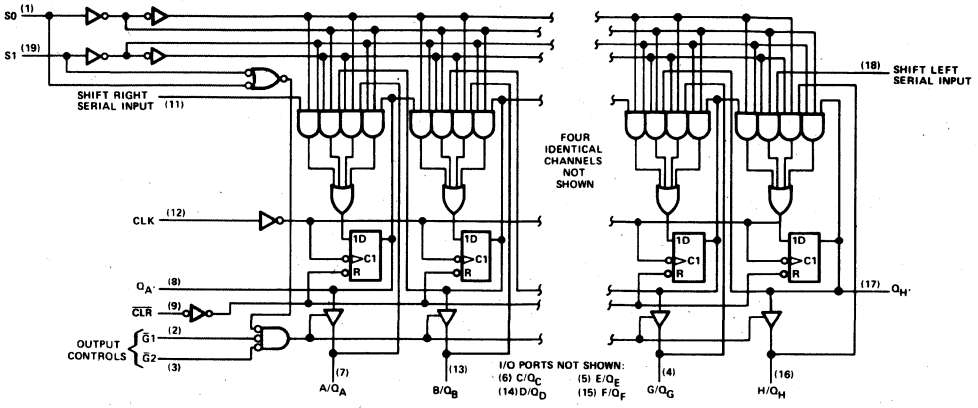
'ALS323



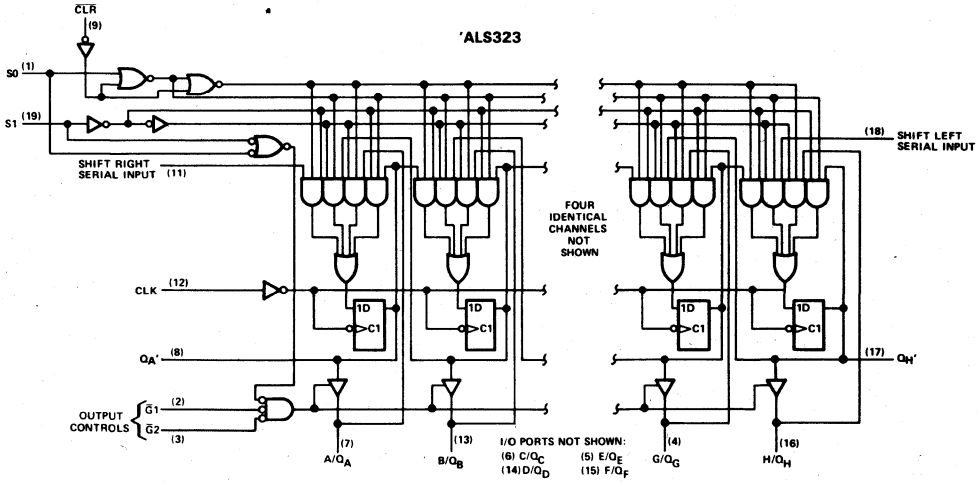
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagrams (positive logic)

'ALS299



'ALS323



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS' . . . . . −55°C to 125°C
SN74ALS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54ALS299 SN54ALS323			SN74ALS299 SN74ALS323			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
I_{OH}	High-level output current	$Q_{A'}$ or $Q_{H'}$				−0.4			−0.4	mA
		Q_A thru Q_H				−1			−2.6	
I_{OL}	Low-level output current	$Q_{A'}$ or $Q_{H'}$				4			8	mA
		Q_A thru Q_H				12			24	
f_{clock}	Clock frequency (at 50% duty cycle)			0		17	0		30	MHz
t_w	Pulse duration	CLK high or low		22			16.5			ns
		$\overline{CLR}$ low ('ALS299)		12			10			
t_{su}	Setup time before CLK↑	Select		25			20			ns
		Serial or Parallel data	High level	18			16			
			Low level	15			6			
		$\overline{CLR}$ inactive ('ALS299)		15			15			
		$\overline{CLR}$ active ('ALS323)		25			20			
		$\overline{CLR}$ inactive ('ALS323)		18			16			
t_h	Hold time after CLK↑	Select		0			0			ns
		Serial or parallel data		0			0			
T_A	Operating free-air temperature			−55		125	0		70°	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS299 SN54ALS323			SN74ALS299 SN74ALS323			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	Q_A thru Q_H	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	$Q_{A'}$ or $Q_{H'}$	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	Q_A thru Q_H	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	A thru H	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	Any other	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	
I_{IH}‡		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}‡	all other	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.15			−0.15	μA
						−0.15			−0.15	
I_O§	$Q_{A'}$, $Q_{H'}$	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
	Q_A thru Q_H			−30		−112	−30		−112	
I_{CC}		V_{CC} = 5.5 V	Outputs high		15	28		15	28	mA
			Outputs low		22	38		22	38	
			Outputs disabled		23	40		23	40	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡For I/O ports (Q_A through Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

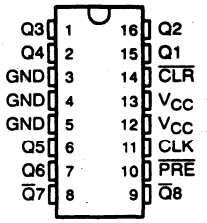
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS299 SN54ALS323		SN74ALS299 SN74ALS323		
			MIN	MAX	MIN	MAX	
f_{max}			17		30		MHz
t_{PLH}	CLK	Q_A thru Q_H	2	19	4	13	ns
t_{PHL}			4	25	7	19	
t_{PLH}	CLK	Q_A' or Q_H'	2	21	5	15	ns
t_{PHL}			4	22	8	18	
t_{PHL}	$\overline{CLR}$ ('ALS299 only)	Q_A thru Q_H	6	29	6	22	ns
		Q_A' or Q_H'	6	29	6	22	
t_{PZH}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H	5	22	6	16	ns
t_{PZL}			6	26	8	22	
t_{PZH}	S0, S1	Q_A thru Q_H	5	21	7	17	ns
t_{PZL}			6	26	8	22	
t_{PHZ}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H	1	15	1	8	ns
t_{PLZ}			5	38	5	15	
t_{PHZ}	S0, S1	Q_A thru Q_H	1	16	1	12	ns
t_{PLZ}			3	20	3	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D3543, JULY 1990

- **Maximum Output Skew of 1 ns**
- **Maximum Pulse Skew of 1 ns**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**

SN74AS303 . . . D OR N PACKAGE
(TOP VIEW)



description

The SN74AS303 contains eight flip-flops designed to have low skew between outputs. The eight outputs (six in-phase with CLK and two out-of-phase) toggle on successive CLK pulses. $\overline{PRE}$ and $\overline{CLR}$ inputs are provided to set the Q and $\overline{Q}$ outputs high or low independent of the CLK pin.

The 'AS303 has output and pulse skew parameters $t_{sk(o)}$ and $t_{sk(p)}$ to ensure performance as a clock driver when a divide-by-two function is required.

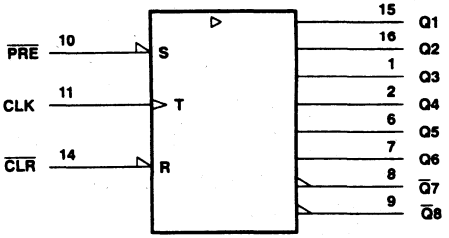
The SN74AS303 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{CLR}$	$\overline{PRE}$	CLK	Q1–Q6	$\overline{Q7}$–$\overline{Q8}$
L	H	X	L	H
H	L	X	H	L
L	L	X	L‡	L‡
H	H	↑	$\overline{Q}_0$	Q_0
H	H	L	Q_0	$\overline{Q}_0$

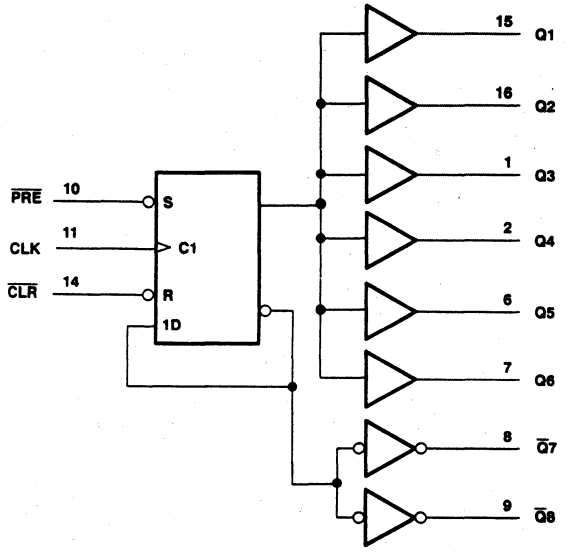
‡ This configuration will not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... 7 V
Input voltage, V_I ..... 7 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = – 18 mA			– 1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = – 2 mA	V_{CC}–2			V
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA	2	2.8		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			– 0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	– 50		– 150	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		40	70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current I_{OS}
NOTE 1: I_{CC} is measured with CLK and $\overline{PRE}$ grounded, then with CLK and $\overline{CLR}$ grounded.

timing requirements

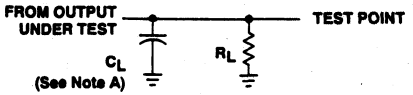
PARAMETER			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	80	MHz
t_w	Pulse duration	$\overline{CLR}$ or $\overline{PRE}$ low	5		ns
		CLK high	4		
		CLK low	6		
t_{su}	Setup time before CLK↑	$\overline{CLR}$ or $\overline{PRE}$ inactive	6		ns

switching characteristics over recommended operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
f_{max}§				80		MHz
t_{PLH}	CLK	Q, $\overline{Q}$	R_L = 500 Ω, C_L = 50 pF	2	9	ns
t_{PHL}				2	9	ns
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q, $\overline{Q}$	R_L = 500 Ω, C_L = 50 pF	3	12	ns
t_{PHL}				3	12	ns
$t_{sk(o)}$	CLK	Q	R_L = 500 Ω, C_L = 10 pF to 30 pF		1	ns
		$\overline{Q}$			1	
		Q, $\overline{Q}$			2	
$t_{sk(p)}$	CLK	Q, $\overline{Q}$	R_L = 500 Ω, C_L = 10 pF to 30 pF		1	ns
t_r					4.5	ns
t_f					3.5	ns

§ f_{max} minimum values are at C_L = 0 to 30 pF.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

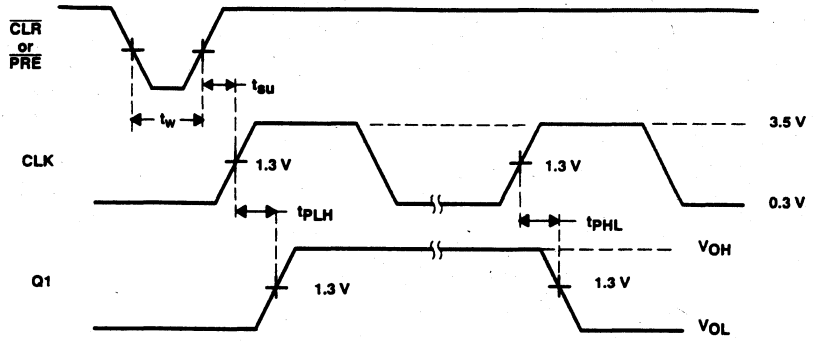
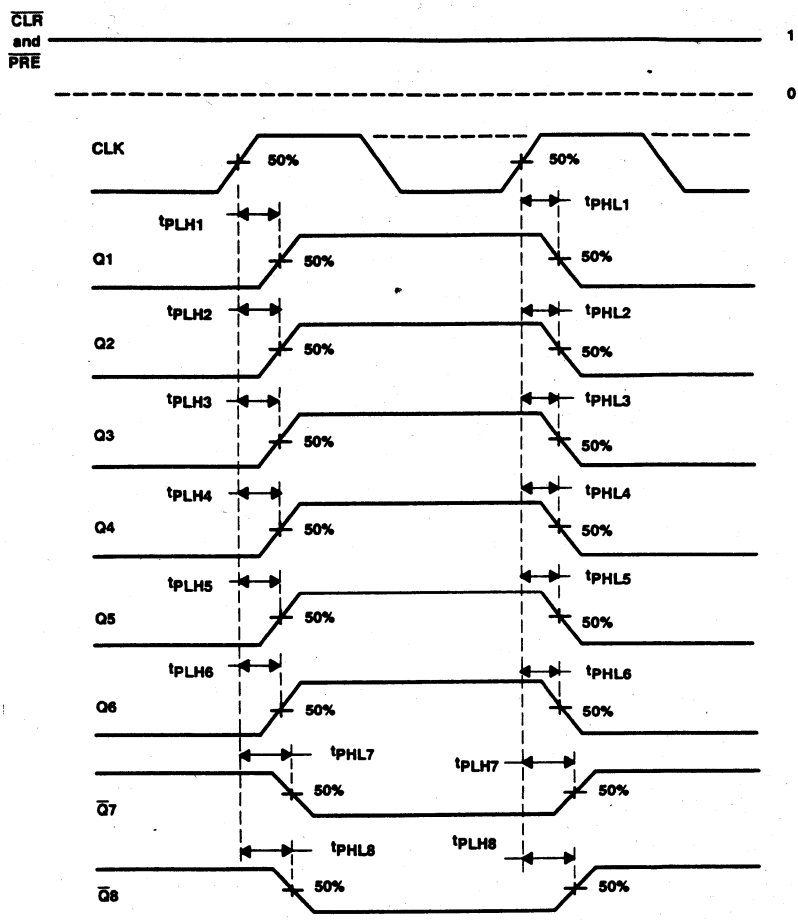


Figure 1. Load Circuit and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, t_r = 2.5 ns, t_f = 2.5 ns.



NOTES: A. $t_{sk(o)}$, CLK to Q, is calculated as the greater of:
1. The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4, 5, 6), and
2. the difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4, 5, 6).

B. $t_{sk(o)}$, CLK to $\overline{Q}$, is calculated as the greater of: $|t_{PLH7} - t_{PLH8}|$ and $|t_{PHL7} - t_{PHL8}|$.

C. $t_{sk(o)}$, CLK to Q and $\overline{Q}$, is calculated as the greater of:
1. The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4, 5, 6), t_{PHL7}, and t_{PHL8}, and
2. the difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4, 5, 6), t_{PLH7}, and t_{PLH8}.

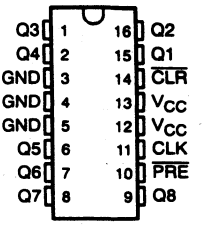
D. $t_{sk(p)}$ is calculated as the greater of $|t_{PLHn} - t_{PHLn}|$ (n = 1, 2, 3, . . ., 8).

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

D3555, JULY 1990

- **Maximum Output Skew of 1 ns**
- **Maximum Pulse Skew of 1 ns**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **Package Options Include Plastic "Small Outline" Packages, and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

The SN74AS304 contains eight flip-flops designed to have low skew between outputs. The eight outputs (in-phase with CLK) toggle on successive CLK pulses. $\overline{PRE}$ and $\overline{CLR}$ pins are provided to set the Q outputs high or low independent of the CLK input.

The SN74AS304 has output and pulse skew parameters $t_{sk(o)}$ and $t_{sk(p)}$ to ensure performances as a clock driver when a divide-by-two function is required.

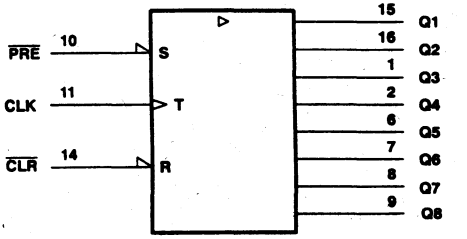
The SN74AS304 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{CLR}$	$\overline{PRE}$	CLK	Q1–Q8
L	H	X	L
H	L	X	H
L	L	X	L†
H	H	↑	$\overline{Q}_0$
H	H	L	Q_0

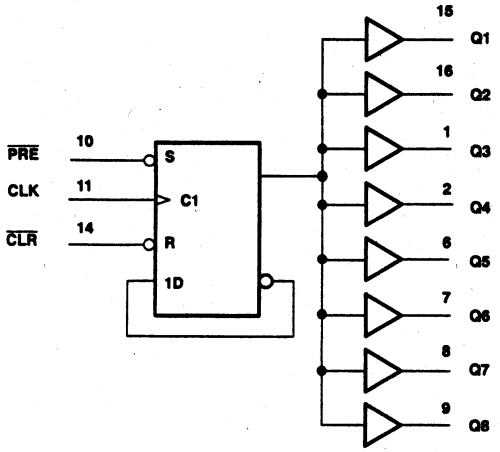
† This configuration will not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... 7 V
Input voltage, V_I ..... 7 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = – 18 mA			– 1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 2 mA	V_{CC}–2			V
	V_{CC} = 4.5 V,	I_{OH} = – 24.mA	2	2.8		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			– 0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	– 50		– 150	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		45	75	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with CLK and $\overline{PRE}$ grounded, then with CLK and $\overline{CLR}$ grounded.

timing requirements

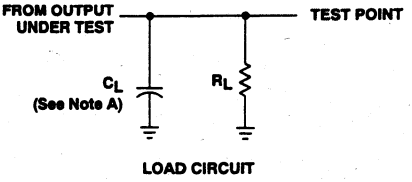
PARAMETER			MIN	NOM	MAX	UNIT
f_{clock}	Clock frequency		0		80	MHz
t_w	Pulse duration	CLK high	4			ns
		CLK low	6			
		$\overline{CLR}$ or $\overline{PRE}$ low	5			
t_{su}	Setup time before CLK↑	$\overline{CLR}$ or $\overline{PRE}$ inactive	6			ns

switching characteristics over recommended operating free-air temperature range (see Figure 1)

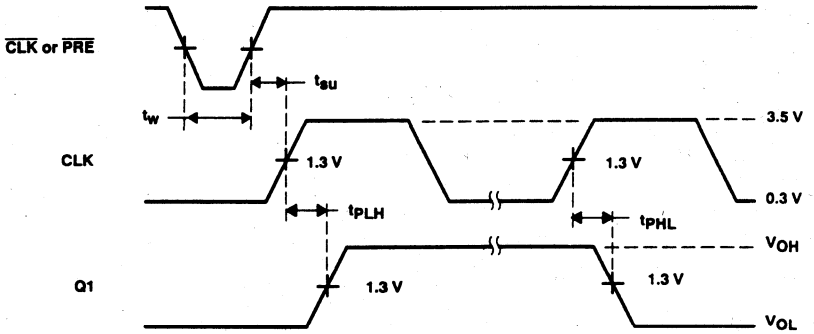
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}§				80			MHz
t_{PLH}	CLK	Q	R_L = 500 Ω, C_L = 50 pF	2	6	9	ns
t_{PHL}				2	6	9	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q	R_L = 500 Ω, C_L = 50 pF	3	7	12	ns
t_{PHL}				3	7	12	
$t_{sk(o)}$	CLK	Q	R_L = 500 Ω, C_L = 10 pF to 30 pF			1	ns
$t_{sk(p)}$	CLK	Q1, Q8	R_L = 500 Ω, C_L = 10 pF to 30 pF			1	ns
		Q2 to Q7				1.5	
t_r						4.5	ns
t_f						3.5	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ f_{max} minimum values are at C_L = 0 to 30 pF.

PARAMETER MEASUREMENT INFORMATION

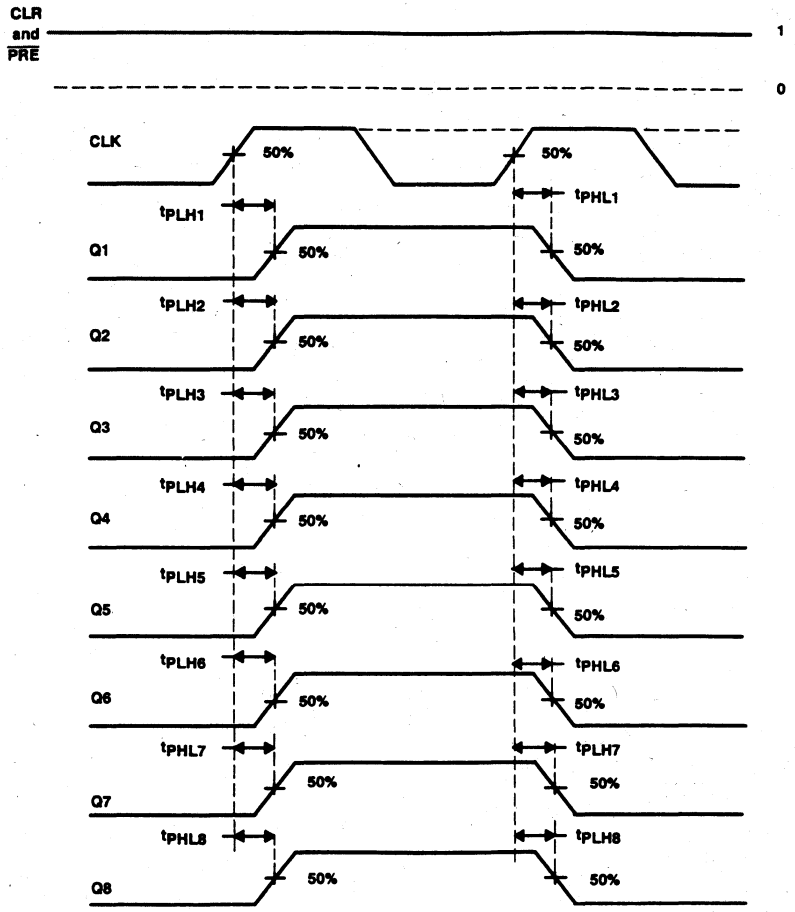


LOAD CIRCUIT



NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, t_r = 2.5 ns, t_f = 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms



NOTES: A. $t_{sk(o)}$, CLK to Q, is calculated as the greater of the following:
1. The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3 . . ., 8).
2. The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3 . . ., 8).
B. $t_{sk(p)}$ is defined at the greater of $| t_{PLHn} - t_{PHLn} |$ (n = 1, 2, 3, . . ., 8).

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

D3596, JUNE 1990 – REVISED SEPTEMBER 1990

- **Maximum Output Skew of 1 ns**
- **Maximum Pulse Skew of 1 ns**
- **Center Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**

description

The SN74AS305 contains eight flip-flops designed to have low skew between outputs. The eight outputs (four in-phase with CLK and four out-of-phase) toggle on successive CLK pulses. $\overline{PRE}$ and $\overline{CLR}$ inputs are provided to set the Q and $\overline{Q}$ outputs high or low independent of the CLK pin.

The SN74AS305 has output and pulse skew parameters $t_{sk(o)}$ and $t_{sk(p)}$ to guarantee performance as a clock driver when a divide-by-two function is required.

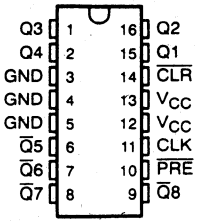
The SN74AS305 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

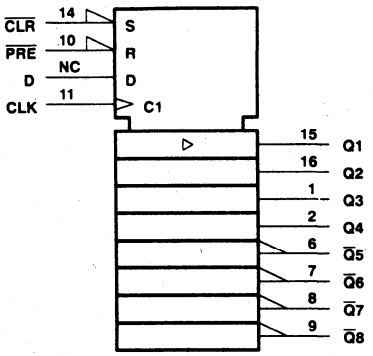
INPUTS			OUTPUTS	
$\overline{CLR}$	$\overline{PRE}$	CLK	Q1-Q4	$\overline{Q5}$-$\overline{Q8}$
L	H	X	L	H
H	L	X	H	L
L	L	X	L†	L†
H	H	L	Q_0	$\overline{Q}_0$
H	H	↑	$\overline{Q}_0$	Q_0

† This configuration will not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

D OR N PACKAGE
(TOP VIEW)

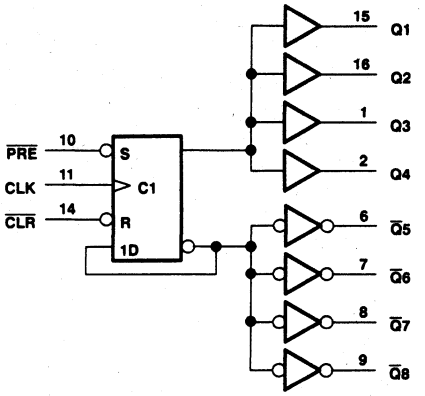


logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... 7 V
Input voltage, V_I ..... 7 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			– 24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = – 18 mA			– 1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = – 2 mA	V_{CC} – 2			V
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA	2	2.8		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7.0 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			– 0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	– 50		– 150	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		40	70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true shorst-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with CLK and $\overline{PRE}$ grounded, then with CLK and $\overline{CLR}$ grounded.

timing requirements

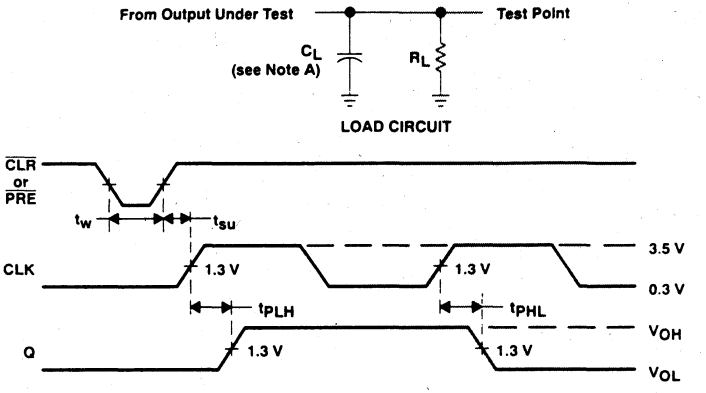
PARAMETER			MIN	NOM	MAX	UNIT
f_{clock}	Clock frequency		0		80	MHz
t_w	Pulse duration	CLK high	4			ns
		CLK low	6			
		$\overline{CLR}$ or $\overline{PRE}$ low	5			
t_{su}	Setup time before CLK↑	$\overline{CLR}$ or $\overline{PRE}$ inactive	6			ns

switching characteristics over recommended operating free-air temperature range

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}‡			R_L = 500 Ω, C_L = 50 pF, V_{CC} = 4.5 V to 5.5 V	80			MHz
t_{PLH}	CLK	Q, $\overline{Q}$		2	6	9	ns
t_{PHL}				2	6	9	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q, $\overline{Q}$		3	7	12	ns
t_{PHL}				3	7	12	
$t_{sk(O)}$	CLK	Q, $\overline{Q}$	R_L = 500 Ω, C_L = 10-30 pF, V_{CC} = 4.5 V to 5.5 V			1	ns
	CLK	Q1 thru $\overline{Q8}$				1.5	
$t_{sk(p)}$	CLK	Q1, $\overline{Q8}$				1.5	ns
	CLK	Q2 thru $\overline{Q7}$				2	
t_r						4.5	ns
t_f						3.5	ns

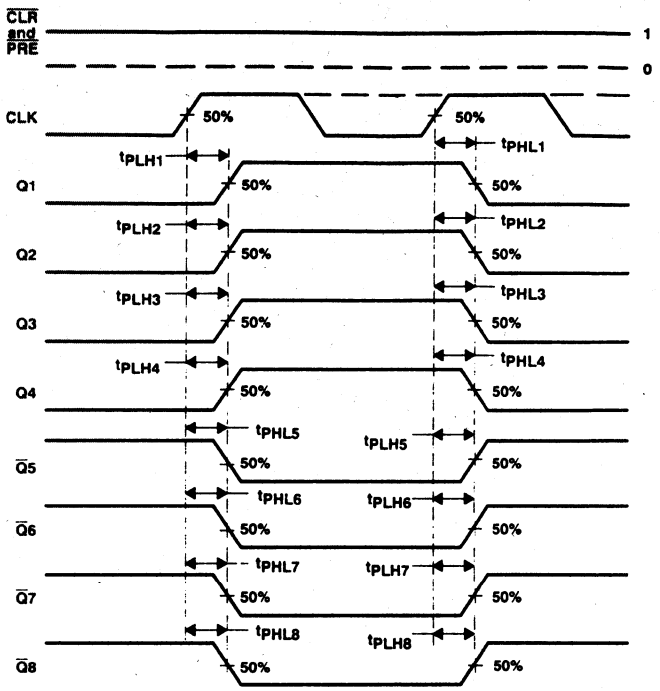
‡ f_{max} minimum values are at C_L = 0 to 30 pF.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, t_r = 2.5 ns, t_f = 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms



NOTES: A. $t_{sk(o)}$ CLK to Q are calculated as the greater of:
1) The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4),
2) the difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4).

B. $t_{sk(o)}$ CLK to $\overline{Q}$ are calculated as the greater of: 1) The difference between the fastest and slowest of t_{PLHn} (n = 5, 6, 7, 8), and 2) The difference between the fastest and slowest of t_{PHLn} (n = 5, 6, 7, 8)

C. $t_{sk(o)}$ CLK to Q and $\overline{Q}$ are calculated as the greater of:
1) The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4), t_{PHLn} (n = 5, 6, 7, 8) and
2) the difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4), t_{PLHn} (n = 5, 6, 7, 8).

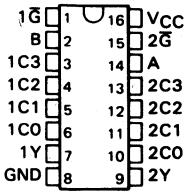
D. $t_{sk(p)}$ is calculated as the greater of $|t_{PLHn} - t_{PHLn}|$ (n = 1, 2, 3, . . . , 8).

Figure 2. Waveforms for Calculation of t_{sk}

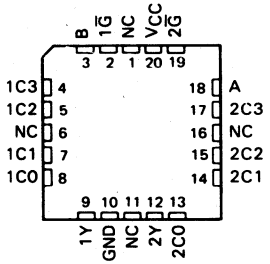
D2661, APRIL 1982 – REVISED MAY 1986

- **Inverting Version of 'ALS153**
- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Strobe (Enable) Line Provided for Cascading (N Lines to n Lines)**
- **Typical 'ALS352 Power per Multiplexer ... 16 mW**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS352 ... J PACKAGE
SN74ALS352 ... D OR N PACKAGE
(TOP VIEW)



SN54ALS352 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

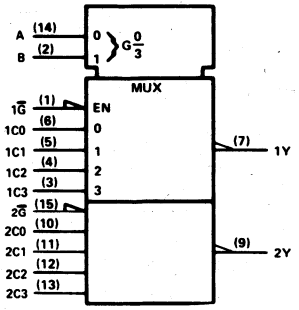
The SN54ALS352 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS352 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

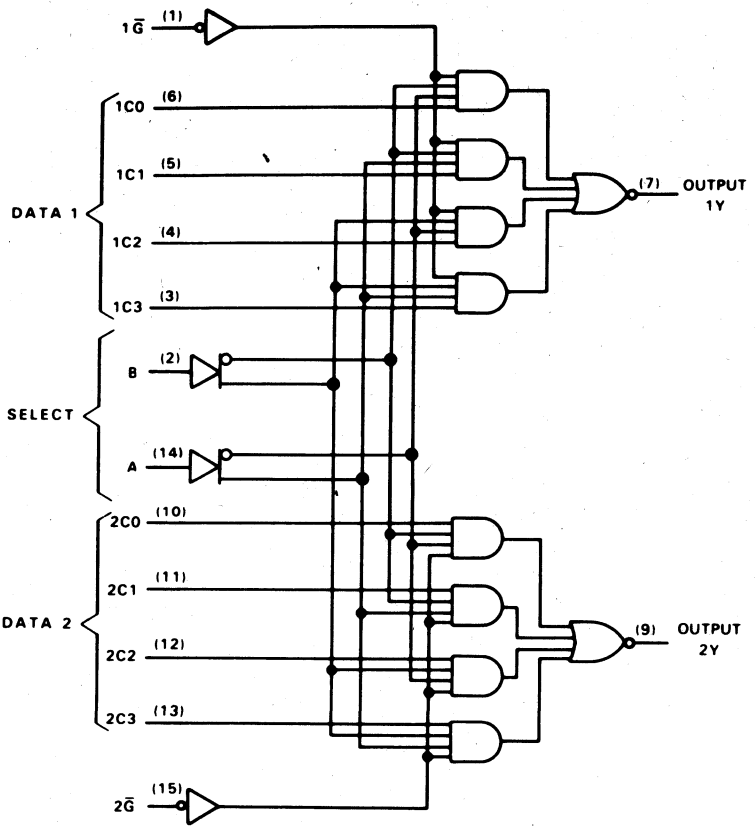
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

TEXAS INSTRUMENTS

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS352 . . . . . −55°C to 125°C
SN74ALS352 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS352			SN74ALS352			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS352			SN74ALS352			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		6.5	10		6.5	10	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with data and select inputs at 4.5 V, and G inputs grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS352		SN74ALS352		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	5	32	5	24	ns
t_{PHL}			5	24	5	21	
t_{PLH}	Data (Any C)	Y	3	24	3	18	ns
t_{PHL}			2	15	2	13	
t_{PLH}	$\overline{G}$	Y	4	26	4	18	ns
t_{PHL}			4	24	4	20	

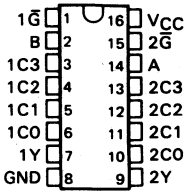
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

SN74AS353A
DUAL 1-OF-4 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

D2661, APRIL 1982 – REVISED MAY 1986

- **Inverting Version of 'AS253**
- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74AS353A . . . D OR N PACKAGE
(TOP VIEW)



description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

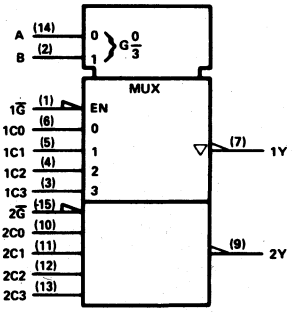
The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$). The output is disabled when its strobe is high.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

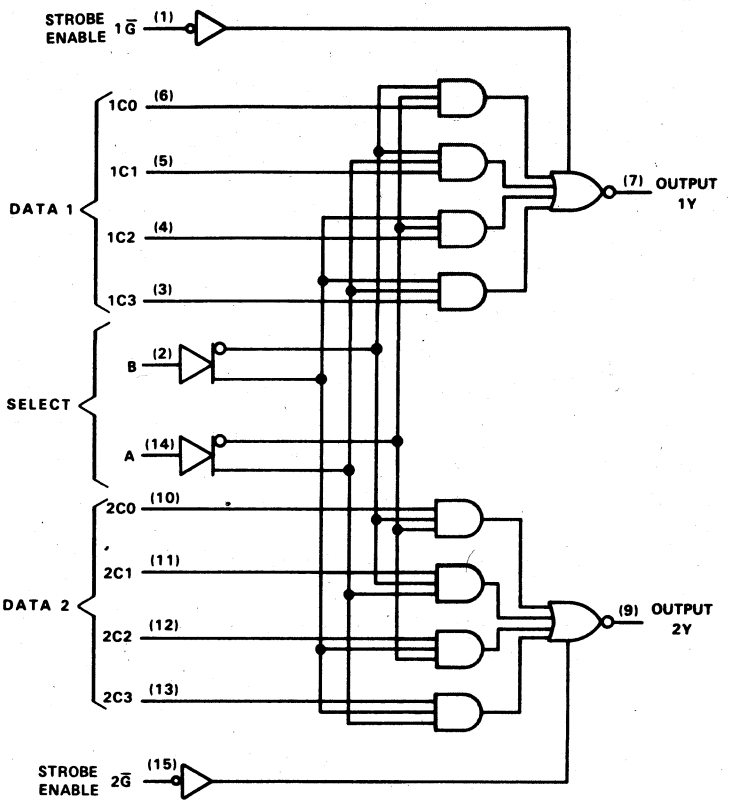
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D and N packages.

TEXAS INSTRUMENTS

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN74AS353A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74AS353A			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74AS353A			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA				
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50	µA
I_I	A, B	V_{CC} = 5.5 V,	V_I = 7 V			0.2	mA
	All others					0.1	
I_{IH}	A, B	V_{CC} = 5.5 V,	V_I = 2.7 V			40	µA
	All other					20	
I_{IL}	A, B	V_{CC} = 5.5 V,	V_I = 0.4 V			−1	mA
	All other					−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		15	24	mA
			Outputs low		19	31	
			Outputs disabled		18	30	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			SN74AS353		
			MIN	MAX	
t_{PLH}	A or B	Y	3	9	ns
t_{PHL}			4	12	
t_{PLH}	Data (Any C)	Y	3	7.5	ns
t_{PHL}			2	6	
t_{PZH}	Strobe	Y	3	7.5	ns
t_{PZL}			4	12.5	
t_{PHZ}	Strobe	Y	2	5.5	ns
t_{PLZ}			3	7.5	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982 – REVISED MAY 1986

- **8 Latches in a Single Package**
- **3-State Bus-Driving True Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **P-N-P Inputs Reduce D-C Loading on Data Lines**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

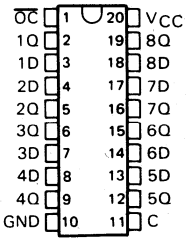
The eight latches of the 'ALS373 and 'AS373 are transparent D-type latches. While the enable (C) is high the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs.

A buffered output-control input ($\overline{OC}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

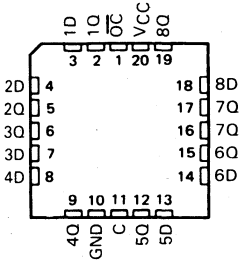
The output control $\overline{OC}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS373 and SN54AS373 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS373 and SN74AS373 are characterized for operation from 0°C to 70°C.

SN54ALS373, SN54AS373 . . . J PACKAGE
SN74ALS373, SN74AS373 . . . DW OR N PACKAGE
(TOP VIEW)



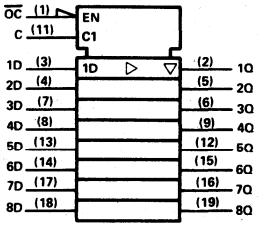
SN54ALS373, SN54AS373 . . . FK PACKAGE
(TOP VIEW)



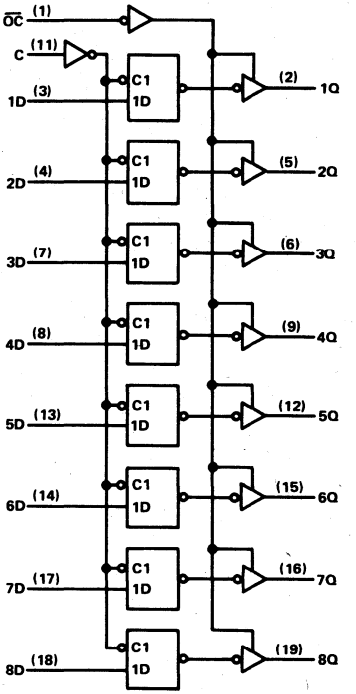
FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS373, SN54AS373 . . . . . −55°C to 125°C
SN74ALS373, SN74AS373 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS373			SN74ALS373			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
t_w	Pulse duration, enable C high	10			10			ns
t_{su}	Setup time, data before enable C↓	10			10			ns
t_h	Hold time, data after enable C↓	7			7			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS373			SN74ALS373			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		9	16		9	16	mA
		Outputs low		16	25		16	25	
		Outputs disabled		17	27		17	27	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS373		SN74ALS373		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	2	17	2	12	ns
t_{PHL}			1	19	4	16	
t_{PLH}	C	Any Q	6	29	6	22	ns
t_{PHL}			1	27	7	23	
t_{PZH}	$\overline{OC}$	Any Q	6	22	6	18	ns
t_{PZL}			5	24	5	20	
t_{PHZ}	$\overline{OC}$	Any Q	2	12	2	10	ns
t_{PLZ}			2	16	2	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54AS373			SN74AS373			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			32			48	mA
t_w	Pulse duration, enable C high	5.5			4.5			ns
t_{su}	Setup time, data before enable C↓	2			2			ns
t_h	Hold time, data after enable C↓	3			3			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS373			SN74AS373			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.27	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.32	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.02	−0.5		−0.02	−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		55	90		55	90	mA
		Outputs low		55	85		55	85	
		Outputs disabled		65	100		65	100	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS373		SN74AS373		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3	8	3.5	6	ns
t_{PHL}			3	7	3.5	6	
t_{PLH}	C	Any Q	6.5	14	6.5	11.5	ns
t_{PHL}			5	8	5	7.5	
t_{PZH}	$\overline{OC}$	Any Q	2	7.5	2	6.5	ns
t_{PZL}			4.5	10.5	4.5	9.5	
t_{PHZ}	$\overline{OC}$	Any Q	3	7.5	3	6.5	ns
t_{PLZ}			3	8	3	7	

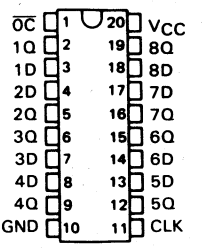
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN74ALS374A, SN74AS374, SN54ALS374A, SN54AS374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

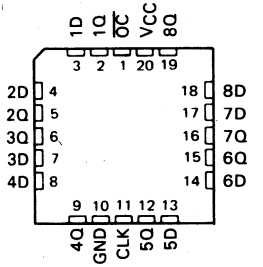
D2661, APRIL 1982 – REVISED MAY 1986

- **D-Type Flip-Flops In a Single Package**
- **3-State Bus-Driving True Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS374A, SN54AS374 ... J PACKAGE
SN74ALS374A, SN74AS374 ... DW OR N PACKAGE
(TOP VIEW)



SN54ALS374A, SN54AS374 ... FK PACKAGE
(TOP VIEW)



description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'ALS374A and 'AS374 are edge-triggered D-type flip-flops. On the positive transition of the clock the Q outputs will be set to the logic levels that were set up at the D inputs.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

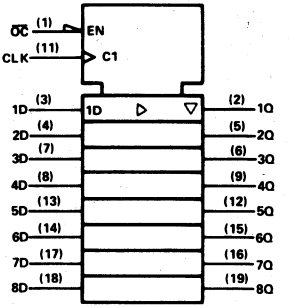
The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS374A and SN54AS374 are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS374A and SN74AS374 are characterized for operation from 0 °C to 70 °C.

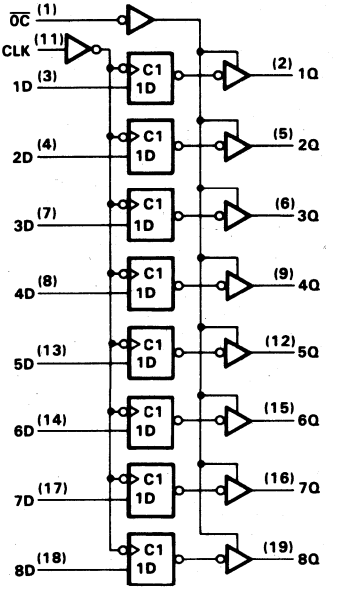
FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS374A, SN54AS374 . . . . . −55 °C to 125 °C
SN74ALS374A, SN74AS374 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS374A			SN74ALS374A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	high-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		30	0		35	MHz
t_w	Pulse duration	CLK high	16.5			14			ns
		CLK low	16.5			14			
t_{su}	Setup time, data before CLK↑		10			10			ns
t_h	Hold time, data after CLK↑		4			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS374A			SN74ALS374A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		11	19		11	19	mA
		Outputs low		19	28		19	28	
		Outputs disabled		20	31		20	31	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

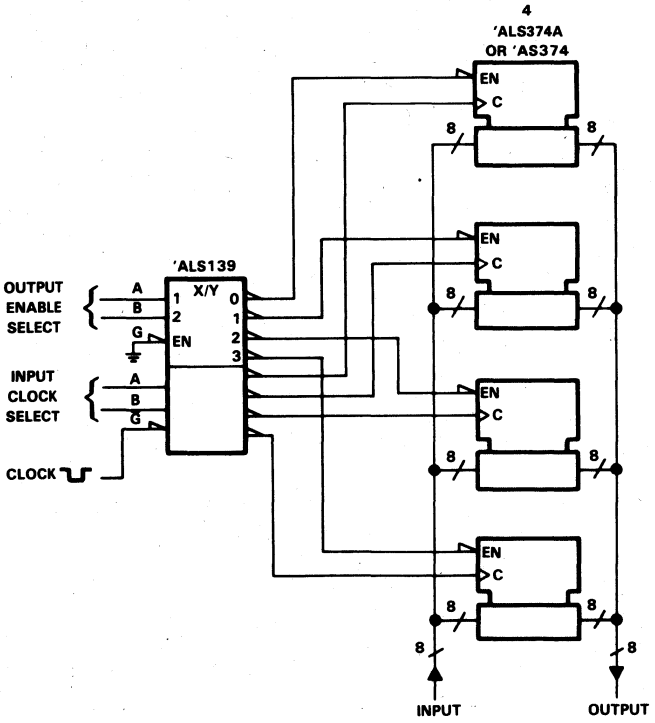
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS374A		SN74ALS374A		
			MIN	MAX	MIN	MAX	
f_{max}			30		35		MHz
t_{PLH}	CLK	Q	3	21	3	12	ns
t_{PHL}			5	19	5	16	
t_{PZH}	$\overline{OC}$	Q	3	27	3	17	ns
t_{PZL}			5	23	5	18	
t_{PHZ}	$\overline{OC}$	Q	1	12	1	10	ns
t_{PLZ}			2	33	2	18	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

EXPANDABLE 4-WORD BY 8-BIT GENERAL REGISTER FILE



TEXAS INSTRUMENTS

recommended operating conditions

			SN54AS374			SN74AS374			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency		0		100	0		125	MHz
t_w	Pulse duration	CLK high	5.5			4			ns
		CLK low	5			3			
t_{su}	Setup time data before CLK↑		3			2			ns
t_h	Hold time, data after CLK↑		3			2			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS374			SN74AS374			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.29	0.5				V
		V_{CC} = 4.5 V	I_{OL} = 48 mA					0.34	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	OC, CLK	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	Data					−3			−2	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		77	120		77	120	mA
			Outputs low		84	128		84	128	
			Outputs disabled		84	128		84	128	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

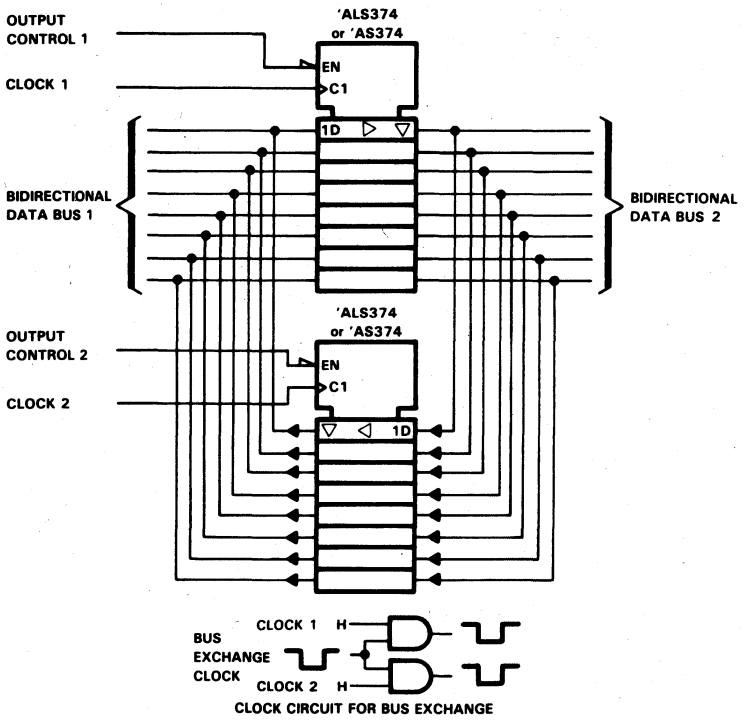
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS374		SN74AS374		
			MIN	MAX	MIN	MAX	
f_{max}			100		125		MHz
t_{PLH}	CLK	Q	3	11	3	8	ns
t_{PHL}			4	11.5	4	9	
t_{PZH}	$\overline{OC}$	Q	2	7	2	6	ns
t_{PZL}			3	11	3	10	
t_{PHZ}	$\overline{OC}$	Q	2	7	2	6	ns
t_{PLZ}			2	7	2	6	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

BIDIRECTIONAL BUS DRIVER



CLOCK CIRCUIT FOR BUS EXCHANGE

TEXAS INSTRUMENTS

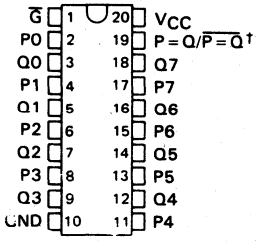
D2661, JUNE 1982 – REVISED MAY 1986

- **Compares Two 8-Bit Words**
- **Choice of Totem-Pole or Open-Collector Outputs**
- **'ALS518, 'ALS520 Have 20-kΩ Pull-up Resistors on Q Inputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

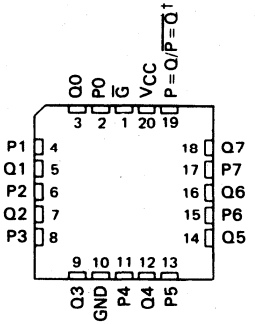
TYPE	INPUT PULL-UP RESISTOR	OUTPUT FUNCTION AND CONFIGURATION
'ALS518	Yes	P = Q open-collector
'ALS519	No	P = Q open-collector
'ALS520	Yes	$\overline{P = Q}$ totem-pole
'ALS521†	No	$\overline{P = Q}$ totem-pole

† 'ALS521 is identical to 'ALS688

SN54ALS' . . . J PACKAGE
SN74ALS' . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS520 FK PACKAGE
(TOP VIEW)



† P = Q for 'ALS518 and 'ALS519 and $\overline{P = Q}$ for 'ALS520 and 'ALS521.

description

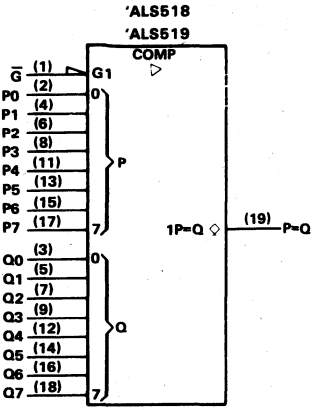
These identity comparators perform comparisons on two eight-bit binary or BCD words. The 'ALS518 and 'ALS519 provide P = Q outputs, while the 'ALS520 and the 'ALS521 provide $\overline{P = Q}$ outputs. The 'ALS518 and the ALS519 have open-collector outputs. The 'ALS518 and 'ALS520 feature 20-kΩ pull-up termination resistors on the Q inputs for analog or switch data.

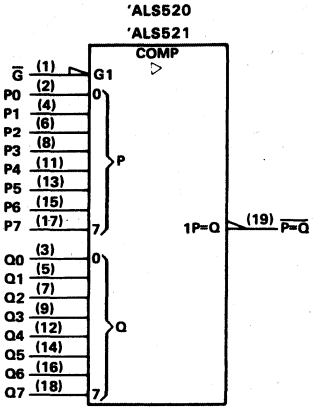
The SN54ALS520 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS518 through SN74ALS521 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

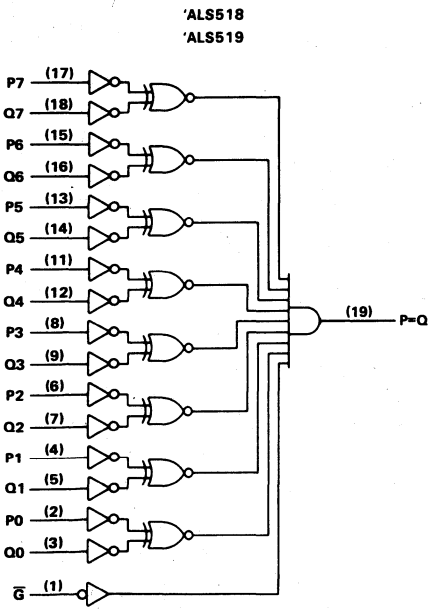
INPUTS		OUTPUTS	
DATA P, Q	ENABLE G	P = Q	$\overline{P = Q}$
P = Q	L	H	L
P > Q	L	L	H
P < Q	L	L	H
X	H	L	H

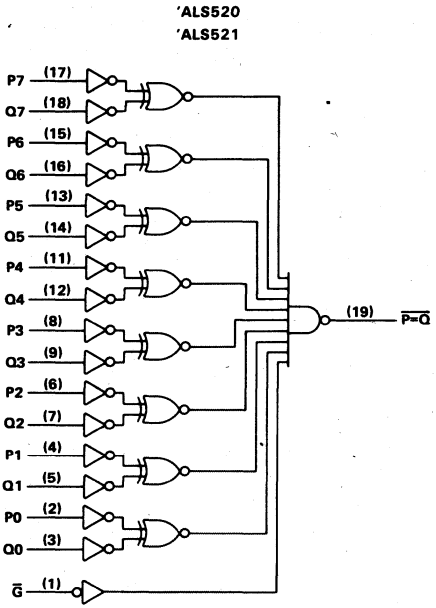
logic symbols†





logic diagrams (positive logic)





†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Q inputs of 'ALS518 . . . . . V_{CC} +0.5 V or 5.5 V, whichever is less
All other inputs . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN74ALS518, SN74ALS519 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74ALS518 SN74ALS519			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			5.5	V
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS518 SN74ALS519			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
I_{OH}		V_{CC} = 5.5 V,	V_{OH} = 5.5 V			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
I_I	'ALS518 Q inputs	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	mA
	All other inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1	
I_{IH}	'ALS518 Q inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			−0.2	mA
	All other inputs					20	µA
I_{IL}	'ALS518 Q inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.6	mA
	All other inputs					−0.1	
I_{CC}	'ALS518	V_{CC} = 5.5 V,	See Note 1		11	17	mA
	'ALS519				11	17	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
Note 1: I_{CC} is measured with $\overline{G}$ grounded, P and Q at 4.5 V.

'ALS518, 'ALS519 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, RL = 680 Ω, T_A = MIN to MAX		UNIT
			SN74ALS518 SN74ALS519		
			MIN	MAX	
t_{PLH}	P or Q	P = Q	15	33	ns
t_{PHL}			3	15	
t_{PLH}	$\overline{G}$	P = Q	15	33	ns
t_{PHL}			3	15	

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Q inputs of 'ALS520 . . . . . V_{CC} + 0.5 V or 5.5 V, whichever is less
All other inputs . . . . . 7 V
Operating free-air temperature range: SN54ALS520 . . . . . −55°C to 125°C
SN74ALS520, SN74ALS521 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS520			SN74ALS520 SN74ALS521			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS520			SN74ALS520 SN74ALS521			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 24 mA					0.35	0.5	
I_I	'ALS520 Q inputs	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	All other inputs	V_{CC} = 5.5 V	V_I = 7 V			0.1			0.1	
I_{IH}	'ALS520 Q inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			−0.2			−0.2	mA
	All other inputs					20			20	μA
I_{IL}	'ALS520 Q inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.6			−0.6	mA
	All other inputs					−0.1			−0.1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS520	V_{CC} = 5.5 V,	See Note 1		12	19		12	19	mA
	'ALS521							12	19	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with $\overline{G}$ grounded and P and Q inputs at 4.5 V.

'ALS520, 'ALS521 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS520		SN74ALS520 SN74ALS521		
			MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	$\overline{P=Q}$	3	19	3	12	ns
t_{PHL}			3	25	5	20	
t_{PLH}	$\overline{G}$	$\overline{P=Q}$	2	18	2	12	ns
t_{PHL}			5	23	5	22	

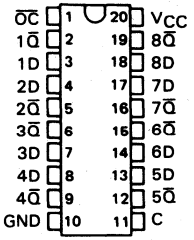
NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

SN74ALS533A, SN74AS533A
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

D2661, APRIL 1982 – REVISED MAY 1986

- **8-Latches In a Single Package**
- **3-State Bus-Driving Inverting Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **P-N-P Inputs Reduce D-C Loading on Data Lines**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS533A, SN74AS533A . . . DW OR N PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers. I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'ALS533A and 'AS533A are transparent D-type latches. While the enable (C) is high, the $\overline{Q}$ outputs will follow the complements of the D inputs. When the enable is taken low, the $\overline{Q}$ outputs will be latched at the inverses of the levels that were set up at the D inputs. The 'ALS533A and 'AS533A are functionally equivalent to the 'ALS373 and 'AS373 except for having inverted outputs.

A buffered output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

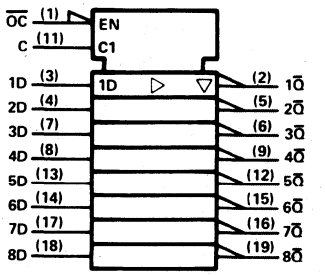
The SN74ALS533A and SN74AS533A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH LATCH)

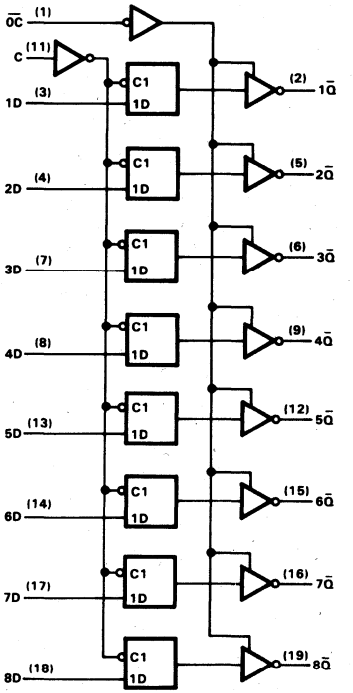
INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

TEXAS INSTRUMENTS

logic symbol†



logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN74ALS533A, SN74AS533A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74ALS533A			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			-2.6	mA
I_{OL}	Low-level output current			24	mA
t_w	Pulse duration, enable C high	15			ns
t_{su}	Setup time, data before enable C ↓	15			ns
t_h	Hold time, data after enable C ↓	7			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS533A			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = -18 mA			-1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = -0.4 mA	V_{CC}-2			V
	V_{CC} = 4.5 V,	I_{OH} = -1 mA				
	V_{CC} = 4.5 V,	I_{OH} = -2.6 mA	2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_I = 0.4 V			-20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			-0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	-30		-112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		10	17	mA
		Outputs low		17	26	
		Outputs disabled		18.5	28	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			SN74ALS533A		
			MIN	MAX	
t_{PLH}	D	$\overline{Q}$	4	19	ns
t_{PHL}			4	13	
t_{PLH}	C	Any $\overline{Q}$	5	23	ns
t_{PHL}			4	18	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	1	17	ns
t_{PZL}			4	18	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	2	10	ns
t_{PLZ}			2	16	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN74AS533A			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			48	mA
t_w	Pulse duration, enable C high	2			ns
t_{su}	Setup time, data before enable C ↓	2			ns
t_h	Hold time, data after enable C ↓	3			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74AS533A			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −12 mA				
	V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.34	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V		−0.02	−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		62	100	mA
		Outputs low		64	100	
		Outputs disabled		71	110	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			SN74AS533A		
			MIN	MAX	
t_{PLH}	D	$\overline{Q}$	4	7.5	ns
t_{PHL}			4	7	
t_{PLH}	C	Any $\overline{Q}$	5	9	ns
t_{PHL}			4	8	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	2	6.5	ns
t_{PZL}			4	9.5	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	2	6.5	ns
t_{PLZ}			3	7	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN74ALS534A, SN74AS534, SN54ALS534
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D2661, APRIL 1982 – REVISED FEBRUARY 1989

- **3-State Bus-Driving Inverting Outputs**
- **Buffered Control Inputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

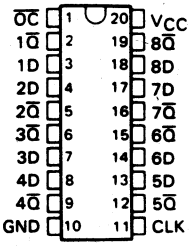
The eight flip-flops of the 'ALS534 and 'AS534 are edge-triggered D-type flip-flops. On the positive transition of the clock, the $\overline{Q}$ outputs will be set to the complement of the logic states that were set up at the D inputs. The 'ALS534 and 'AS534 are functionally equivalent to the 'ALS374 and 'AS374 except for having inverted outputs.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

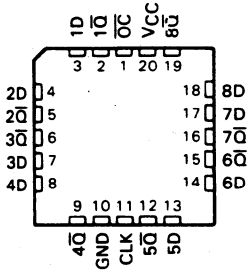
The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS534 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS534A and SN74AS534 are characterized for operation from 0°C to 70°C.

SN54ALS534 . . . J PACKAGE
SN74ALS534A, SN74AS534 . . . DW OR N PACKAGE
(TOP VIEW)



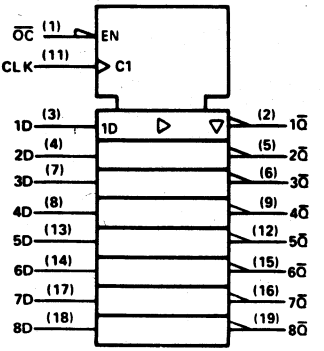
SN54ALS534 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE (EACH FLIP-FLOP)

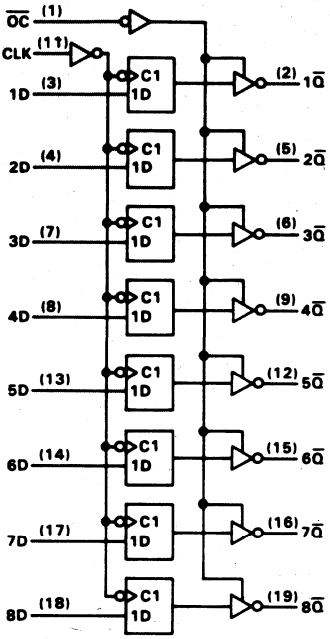
INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS534 . . . . . −55°C to 125°C
SN74ALS534A, SN74AS534 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS534			SN74ALS534A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		30	0		35	MHz
t_w	Pulse duration	CLK high	16.5			14			ns
		CLK low	16.5			14			
t_{su}	Setup time, data before CLK↑		10			10			ns
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS534			SN74ALS534A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	CLK, $\overline{OC}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	D					−0.2			−0.2	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		11	19		11	19	mA
			Outputs low		19	28		19	28	
			Outputs disabled		10	31		20	31	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS534		SN74ALS534A		
			MIN	MAX	MIN	MAX	
f_{max}			30		35		MHz
t_{PLH}	CLK	Any $\overline{Q}$	3	15	3	12	ns
t_{PHL}			5	18	4	16	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	5	19	3	17	ns
t_{PZL}			7	20	4	18	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	2	12	1	10	ns
t_{PLZ}			2	16	2	14	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

			SN74AS534			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−15	mA
I_{OL}	Low-level output current				48	mA
f_{clock}	Clock frequency		0		125	MHz
t_w	Pulse duration	CLK high	4			ns
		CLK low	3			
t_{su}	Setup time, data before CLK ↑		2			ns
t_h	Hold time, data after CLK ↑		2			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74AS534			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA				
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.34	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	$\overline{OC}$, CLK	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5	mA
	D					−2	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		77	120	mA
			Outputs low		84	128	
			Outputs disabled		84	128	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

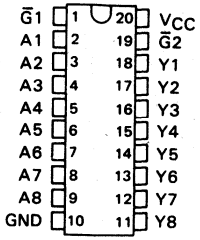
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			SN74AS534		
			MIN	MAX	
f_{max}			125		MHz
t_{PLH}	CLK	Any $\overline{Q}$	3	8	ns
t_{PHL}			4	9	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	2	6	ns
t_{PZL}			3	10	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	2	6	ns
t_{PLZ}			2	6	

NOTE 1: Load circuit and voltage waveforms are shown in Sectin 1.

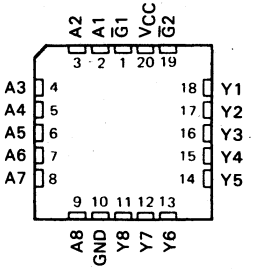
D2661, APRIL 1982 – REVISED MAY 1986

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce D-C Loading**
- **Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS541 . . . J PACKAGE
SN74ALS540, SN74ALS541 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS541 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed to have the performance of the popular SN54ALS240/SN74ALS240 series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

The three-state control gate is a 2-input NOR such that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

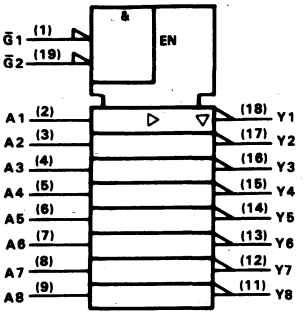
The 'ALS540 provides inverted data and the 'ALS541 provides true data at the outputs.

The -1 versions of the SN74ALS540 and SN74ALS541 parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 miliamperes. There are no -1 versions of the SN54ALS541.

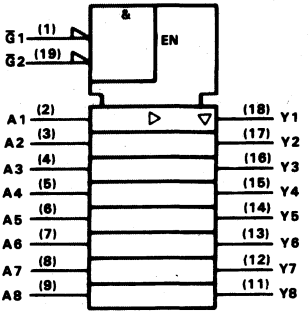
The SN54ALS541 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS540 and SN74ALS541 are characterized for operation from 0°C to 70°C.

logic symbols†

'ALS540

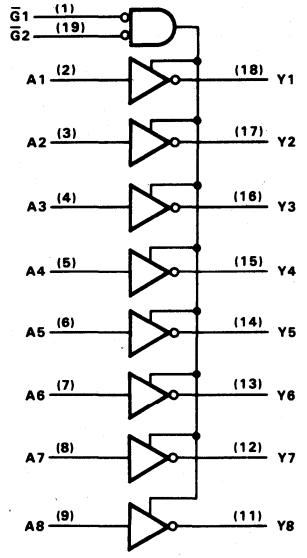


'ALS541

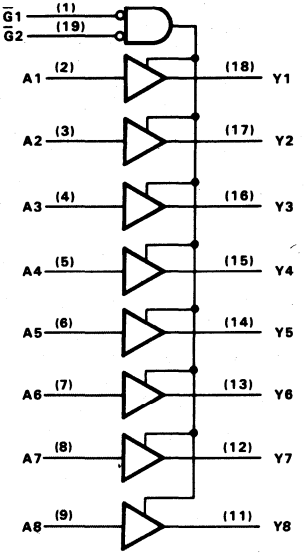


logic diagrams (positive logic)

'ALS540



'ALS541



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS541 . . . . . −55°C to 125°C
SN74ALS540, SN74ALS541 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS541			SN74ALS540 SN74ALS541			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48 mA limit applies for the SN74ALS540-1 and SN74ALS541-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS541			SN74ALS540 SN74ALS541			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA¶					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS540	V_{CC} = 5.5 V	Outputs high					5	10	mA
			Outputs low					13	22	
			Outputs disabled					11	19	
	'ALS541	V_{CC} = 5.5 V	Outputs high		6	14		6	14	mA
			Outputs low		15	25		15	25	
			Outputs disabled		13.5	22		13.5	22	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
¶ I_{OL} = 48 mA for −1 versions.

'ALS540 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			'ALS540	SN74ALS540		
			TYP	MIN	MAX	
t_{PLH}	A	Y	7.5	2	12	ns
t_{PHL}			5.6	2	9	
t_{PZH}	$\overline{G}$	Y	9	5	15	ns
t_{PZL}			12.5	8	20	
t_{PHZ}	$\overline{G}$	Y	4	1	10	ns
t_{PZL}			7	2	12	

'ALS541 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS541	SN54ALS541		SN74ALS541		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	8.7	4	17	4	14	ns
t_{PHL}			7	2	12	2	10	
t_{PZH}	$\overline{G}$	Y	9	5	18	5	15	ns
t_{PZL}			12.5	8	24	8	20	
t_{PHZ}	$\overline{G}$	Y	4	1	12	1	10	ns
t_{PLZ}			7	2	14	2	12	

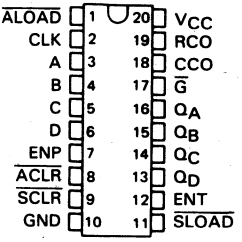
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN74ALS561A, SN54ALS561A
SYNCHRONOUS 4-BIT COUNTERS WITH 3-STATE OUTPUTS

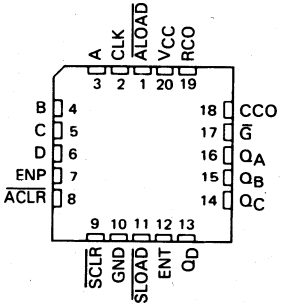
D2661, DECEMBER 1982 – REVISED MAY 1986

- **Carry Output for n-Bit Cascading**
- **Buffer-Type Outputs Drive Bus Lines Directly**
- **Choice of Asynchronous or Synchronous Load or Clear**
- **Internal Look-Ahead for Fast Cascading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS561A . . . J PACKAGE
SN74ALS561A . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS561A . . . FK PACKAGE
(TOP VIEW)



description

The 'ALS561A binary counter is programmable and offers synchronous and asynchronous clearing as well as synchronous and asynchronous loading. All synchronous functions are executed on the positive-going edge of the clock.

The clear function is initiated by applying a low level to either Asynchronous Clear ($\overline{ACLR}$) or Synchronous Clear ($\overline{SCLR}$). Asynchronous (direct) clearing overrides all other functions of the device, while synchronous clearing overrides only the other synchronous functions. Data is loaded from the A, B, C, and D inputs by applying a low level to Asynchronous Load ($\overline{ALOAD}$) or by the combination of a low level at Synchronous Load ($\overline{SLOAD}$) and a positive-going clock transition. The counting function is enabled only when Enable P (ENP), Enable T (ENT), $\overline{ACLR}$, $\overline{ALOAD}$, $\overline{SCLR}$, and $\overline{SLOAD}$ are all high.

A high level at the Output Enable ($\overline{G}$) forces the Q outputs into the high-impedance state, and a low level enables those outputs. Counting is independent of $\overline{G}$. ENT is fed forward to enable the Ripple Carry Output (RCO) to produce a high-level pulse while the count is maximum (15). The Clocked Carry Output (CCO) produces a high-level pulse for a duration equal to that of the low level of the clock when RCO is high and the counter is enabled (both ENP and ENT are high); otherwise, CCO is low. CCO does not have the glitches commonly associated with a ripple-carry output. Cascading is normally accomplished by connecting RCO or CCO of the fist counter to ENT of the next counter. However, for very-high-speed counting, RCO should be used for cascading since CCO does not become active until the clock returns to the low level.

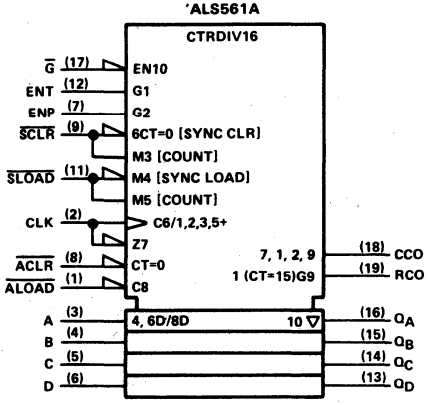
The SN54ALS516A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS561A is characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS

FUNCTION TABLE

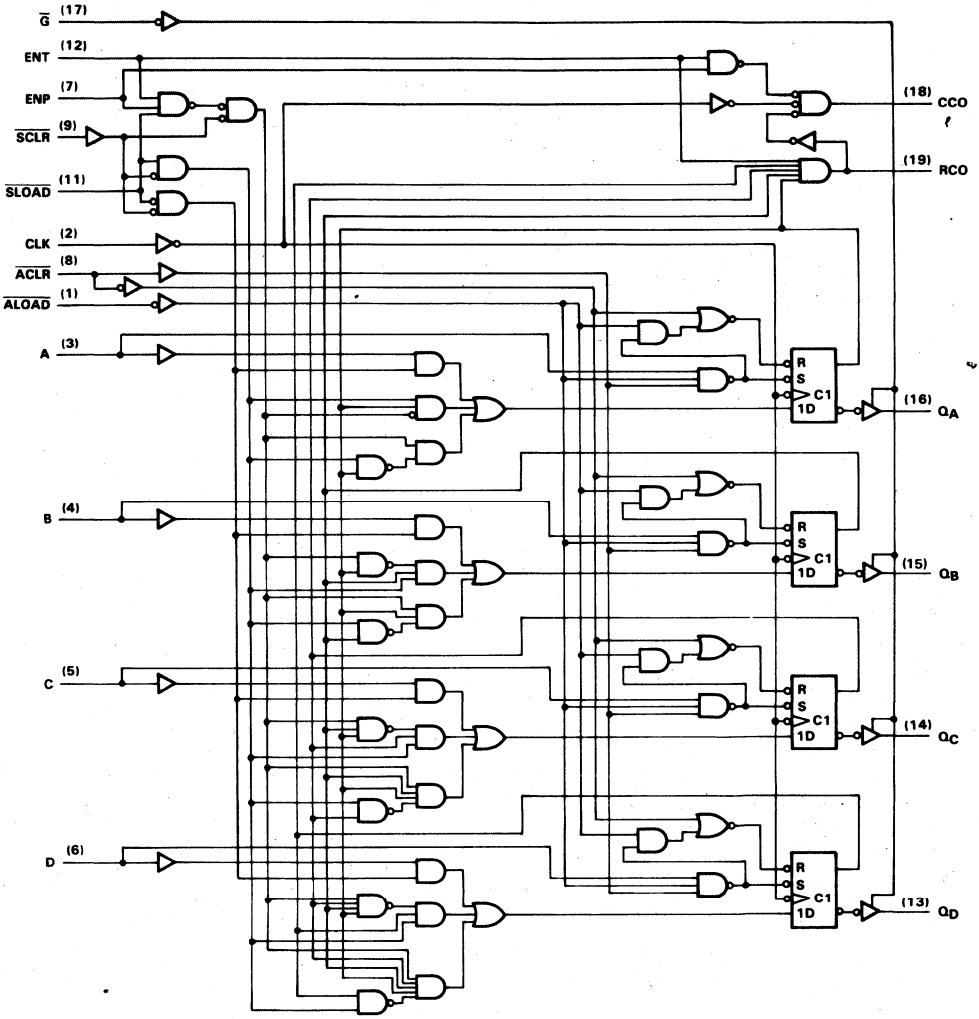
INPUTS								OPERATION
$\overline{G}$	$\overline{ACLR}$	$\overline{ALOAD}$	$\overline{SCLR}$	$\overline{SLOAD}$	ENT	ENP	CLK	
H	X	X	X	X	X	X	X	Q Outputs Disabled
L	L	X	X	X	X	X	X	Asynchronous Clear
L	H	L	X	X	X	X	X	Asynchronous Load
L	H	H	L	X	X	X	↑	Synchronous Clear
L	H	H	H	L	X	X	↑	Synchronous Load
L	H	H	H	H	H	H	↑	Count
L	H	H	H	H	L	X	X	Inhibit Counting
L	H	H	H	H	X	L	X	Inhibit Counting

logic symbol †



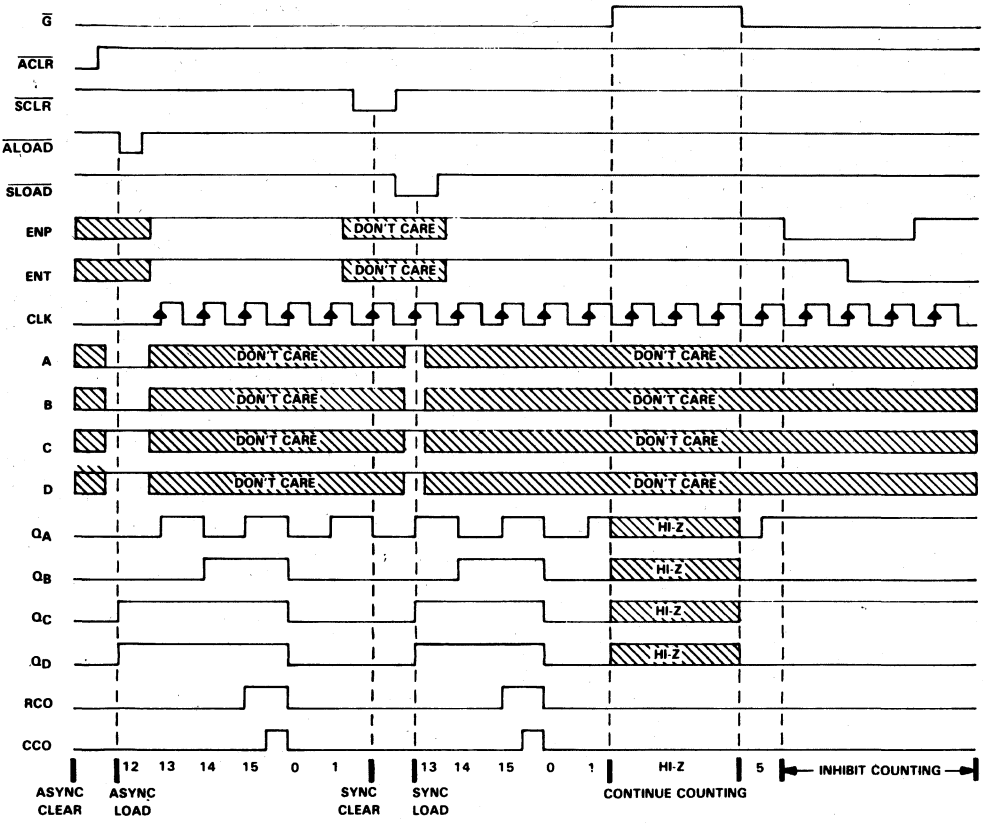
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

'ALS561A logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

'ALS561A typical load, count, and inhibit sequences



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS561A . . . . . −55°C to 125°C
SN74ALS561A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54ALS561A			SN74ALS561A			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
I_{OH}	High-level output current	Q outputs				−7			−2.6	mA
		CCO and RCO				−0.4			−0.4	
I_{OL}	Low-level output current	Q outputs				12			24	mA
		CCO and RCO				4			8	
f_{clock}	Clock frequency			0		25	0		30	MHz
t_w	Pulse duration	$\overline{ACLR}$ or $\overline{ALOAD}$ low		20			15			ns
		CLK high		20			16.5			
		CLK low		20			16.5			
t_{su}	Setup time before CLK ↑	ENP, ENT	High	25			20			ns
			Low	25			20			
		Data at A, B, C, D		25			20			
		$\overline{SCLR}$	Low	21			15			
			High (inactive)	35			30			
		$\overline{SLOAD}$	Low	20			15			
			High (inactive)	35			30			
		$\overline{ACLR}$ or $\overline{ALOAD}$ inactive		10			10			
t_h	Hold time after CLK ↑ for data, ENP, ENT, $\overline{SCLR}$, or $\overline{SLOAD}$			0			0			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS561A			SN74ALS561A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
	CCO and RCO	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	ENT and ENP	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	Other inputs					0.1			0.1	
I_{IH}	ENT and ENP	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	Other inputs					20			20	
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	CCO and RCO	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
	Q			−30		−112	−30		−112	
I_{CC}		V_{CC} = 5.5 V	Outputs high		17	27		17	27	mA
			Outputs low		21	33		21	33	
			Outputs disabled		22	36		22	36	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS561A		SN74ALS561A		
			MIN	MAX	MIN	MAX	
f_{max}			25		30		MHz
t_{PLH}	CLK	Any Q	4	15	4	12	ns
t_{PHL}			5	21	5	18	
t_{PLH}	CLK	RCO	9	35	9	29	ns
t_{PHL}			8	29	8	24	
t_{PLH}	CLK	CCO	8	31	8	26	ns
t_{PHL}			5	20	5	16	
t_{PLH}	$\overline{ALOAD}$	Any Q	10	38	10	35	ns
t_{PHL}			7	27	7	23	
t_{PLH}	$\overline{ALOAD}$	RCO	15	50	15	40	ns
t_{PHL}			12	35	12	30	
t_{PLH}	$\overline{ALOAD}$	CCO	25	65	25	55	ns
t_{PHL}			12	42	12	33	
t_{PLH}	A, B, C, or D	Any Q	8	35	8	30	ns
t_{PHL}			7	27	7	22	
t_{PLH}	ENT	RCO	5	20	5	16	ns
t_{PHL}			4	18	4	14	
t_{PLH}	ENT	CCO	12	35	12	32	ns
t_{PHL}			4	15	4	12	
t_{PLH}	ENP	CCO	5	22	5	18	ns
t_{PHL}			4	14	4	12	
t_{PHL}	$\overline{ACLR}$	Any Q	7	28	7	22	ns
t_{PZH}	$\overline{G}$	Any Q	5	24	5	19	ns
t_{PZL}			8	28	8	23	
t_{PHZ}	$\overline{G}$	Any Q	2	12	2	10	ns
t_{PLZ}			4	20	4	15	

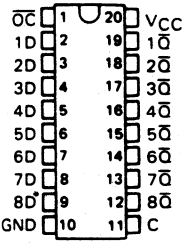
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN74ALS563B
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982 – REVISED JANUARY 1989

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus Structured Pinout**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS563B . . . DW OR N PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type latches. While the enable (C) is high the Q outputs will follow the complements of data (D) inputs. When the enable is taken low the output will be latched at the inverses of the levels that were set up at the D inputs.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high-logic level provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control (OC) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS563A is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS563B is characterized for operation from 0 °C to 70 °C.

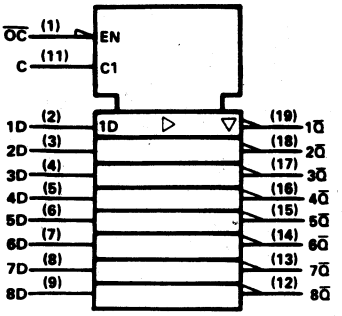
The SN74ALS563B is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(EACH LATCH)

INPUTS			OUTPUT
ENABLE			
$\overline{OC}$	C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

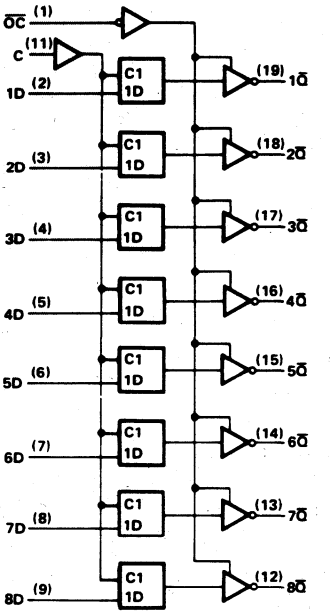
TEXAS INSTRUMENTS

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN74ALS563B . . . . . 0°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74ALS563B			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−2.6	mA
I_{OL}	Low-level output current			24	mA
t_w	Pulse duration, enable C high	15			ns
t_{su}	Setup time, data before enable C ↓	10			ns
t_h	Hold time, data after enable C ↓	10			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS563B			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OL} = −1 mA				
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2,7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_O*	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		10	17	mA
		Outputs low		16	26	
		Outputs disabled		17	29	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
* The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			'ALS563	SN74ALS563B		
			TYP	MIN	MAX	
t_{PLH}	D	Q	10	3	18	ns
t_{PHL}			8	3	14	
t_{PLH}	C	Q	8	6	22	ns
t_{PHL}			14	6	21	
t_{PZH}	OC	Q	8	3	18	ns
t_{PZL}			10	4	18	
t_{PHZ}	OC	Q	5	1	10	ns
t_{PLZ}			7	1	15	

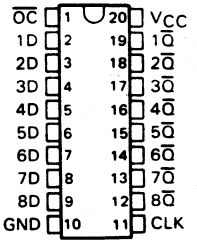
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

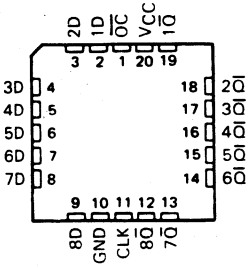
D2661, APRIL 1982 – REVISED JANUARY 1989

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus Structured Pinout**
- **Buffered Control Inputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS564A ... J PACKAGE
SN74ALS564B ... DW OR N PACKAGE
(TOP VIEW)



SN54ALS564A ... FK PACKAGE
(TOP VIEW)



description

These 8-bit registers feature inverting three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight-bit edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock.

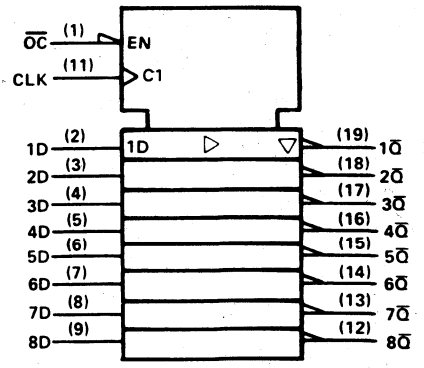
The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS564A is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS564B is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE
(EACH FLIP-FLOP)

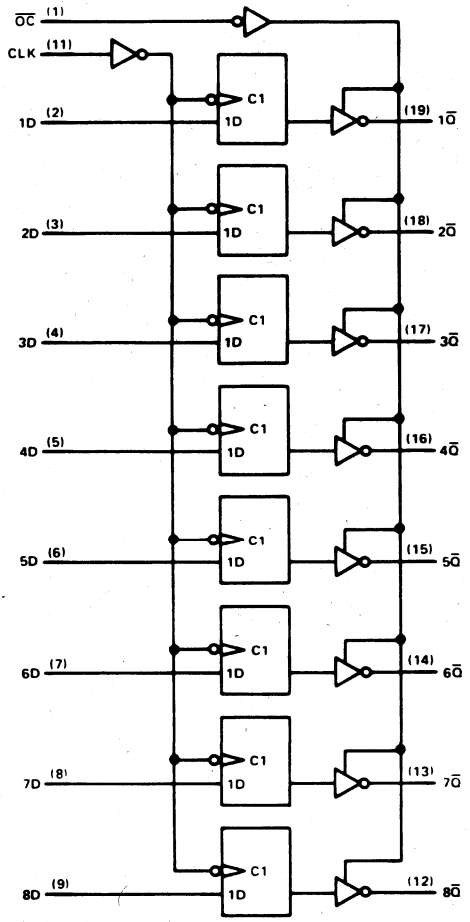
INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS564A . . . . . −55 °C to 125 °C
SN74ALS564B . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS564A			SN74ALS564B			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		25	0		30	MHz
t_w	Pulse duration	CLK high	16.5			14			ns
		CLK low	16.5			14			
t_{su}	Setup time, data before CLK↑		15			15			ns
t_h	Hold time, data after CLK↑		4			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS564A			SN74ALS564B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O*	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		10	18		10	18	mA
		Outputs low		15	24		15	24	
		Outputs disabled		16	30		16	30	

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
* The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25 °C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'ALS564	SN54ALS564A		SN74ALS564B		
			TYP	MIN	MAX	MIN	MAX	
f_{max}			50	25		30		MHz
tPLH	CLK	Any $\overline{Q}$	9	4	15	3	14	ns
tPHL			9	4	15	4	14	
tPZH	$\overline{OC}$	Any $\overline{Q}$	11	4	21	3	18	ns
tPZL			11	4	21	4	18	
tPHZ	$\overline{OC}$	Any $\overline{Q}$	6	2	12	1	10	ns
tPLZ			8	3	17	2	15	

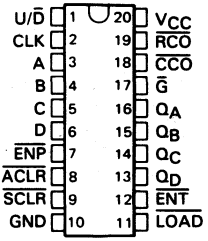
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN74ALS568A, SN74ALS569A, SN54ALS569A
SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

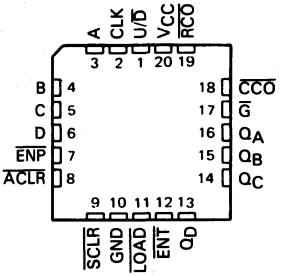
D2661, APRIL 1982 – REVISED MAY 1986

- **3-State Q Outputs Drive Bus Lines Directly**
- **Counter Operation Independent of 3-State Output**
- **Fully Synchronous Clear, Count, and Load**
- **Asynchronous Clear Also Provided**
- **Fully Cascadable**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS569A . . . J PACKAGE
SN74ALS568A, SN74ALS569A . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS569A . . . FK PACKAGE
(TOP VIEW)



description

The 'ALS568A decade counters and 'ALS569A binary counters are programmable, count up or down, and offer both synchronous and asynchronous clearing. All synchronous functions are executed on the positive-going edge of the clock.

The clear function is initiated by applying a low level to either Asynchronous Clear ($\overline{\text{ACLR}}$) or Synchronous Clear ($\overline{\text{SCLR}}$). Asynchronous (direct) clearing overrides all other functions of the device, while synchronous clearing overrides only the other synchronous functions. Data is loaded from the A, B, C, and D inputs by holding Load ($\overline{\text{LOAD}}$) low during a positive-going clock transition. The counting function is enabled only when Enable P ($\overline{\text{ENP}}$) and Enable T ($\overline{\text{ENT}}$) are low and $\overline{\text{ACLR}}$, $\overline{\text{SCLR}}$, and $\overline{\text{LOAD}}$ are high. The Up/Down (U/$\overline{\text{D}}$) input controls the direction of the count. These counters count up when U/$\overline{\text{D}}$ is high and count down when U/$\overline{\text{D}}$ is low.

A high level at the Output Enable ($\overline{\text{G}}$) forces the Q outputs into the high-impedance state, and a low level enables those outputs. Counting is independent of $\overline{\text{G}}$. $\overline{\text{ENT}}$ is fed forward to enable the Ripple Carry Output ($\overline{\text{RCO}}$) to produce a low-level pulse while the count is zero (all Q outputs low) when counting down or maximum (9 or 15) when counting up. The Clocked Carry Output ($\overline{\text{CCO}}$) produces a low level pulse for a duration equal to that of the low level of the clock when $\overline{\text{RCO}}$ is low and the counter is enabled (both $\overline{\text{ENP}}$ and $\overline{\text{ENT}}$ are low); otherwise, $\overline{\text{CCO}}$ is high. $\overline{\text{CCO}}$ does not have the glitches commonly associated with a ripple-carry output. Cascading is normally accomplished by connecting $\overline{\text{RCO}}$ or $\overline{\text{CCO}}$ of the first counter to $\overline{\text{ENT}}$ of the next counter. However, for very-high-speed counting, $\overline{\text{RCO}}$ should be used for cascading since $\overline{\text{CCO}}$ does not become active until the clock returns to the low level.

The SN54ALS569A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS568A and SN74ALS569A are characterized for operation from 0°C to 70°C.

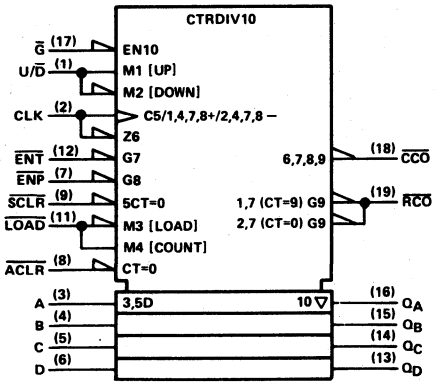
TEXAS INSTRUMENTS

FUNCTION TABLE

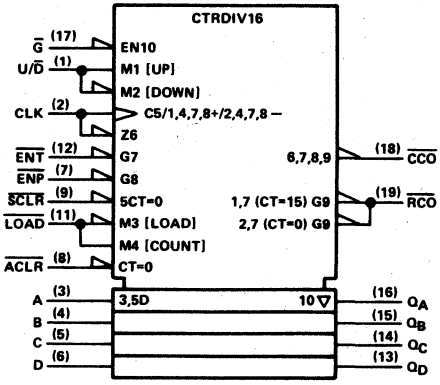
INPUTS								OPERATION
$\overline{G}$	$\overline{ACLR}$	$\overline{SCLR}$	$\overline{LOAD}$	$\overline{ENT}$	$\overline{ENP}$	U/$\overline{D}$	CLK	
H	X	X	X	X	X	X	X	Q Outputs Disabled
L	L	X	X	X	X	X	X	Asynchronous Clear
L	H	L	X	X	X	X	↑	Synchronous Clear
L	H	H	L	X	X	X	↑	Load
L	H	H	H	L	L	H	↑	Count Up
L	H	H	H	L	L	L	↑	Count Down
L	H	H	H	H	X	X	X	Inhibit Count
L	H	H	H	X	H	X	X	Inhibit Count

logic symbols†

'ALS568A

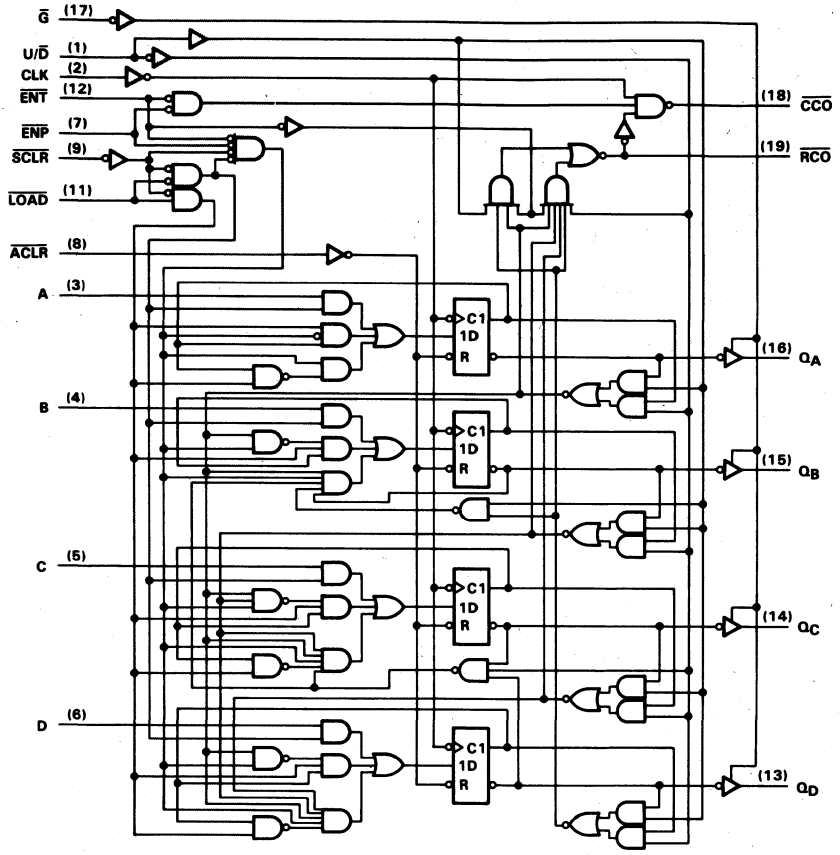


'ALS569A



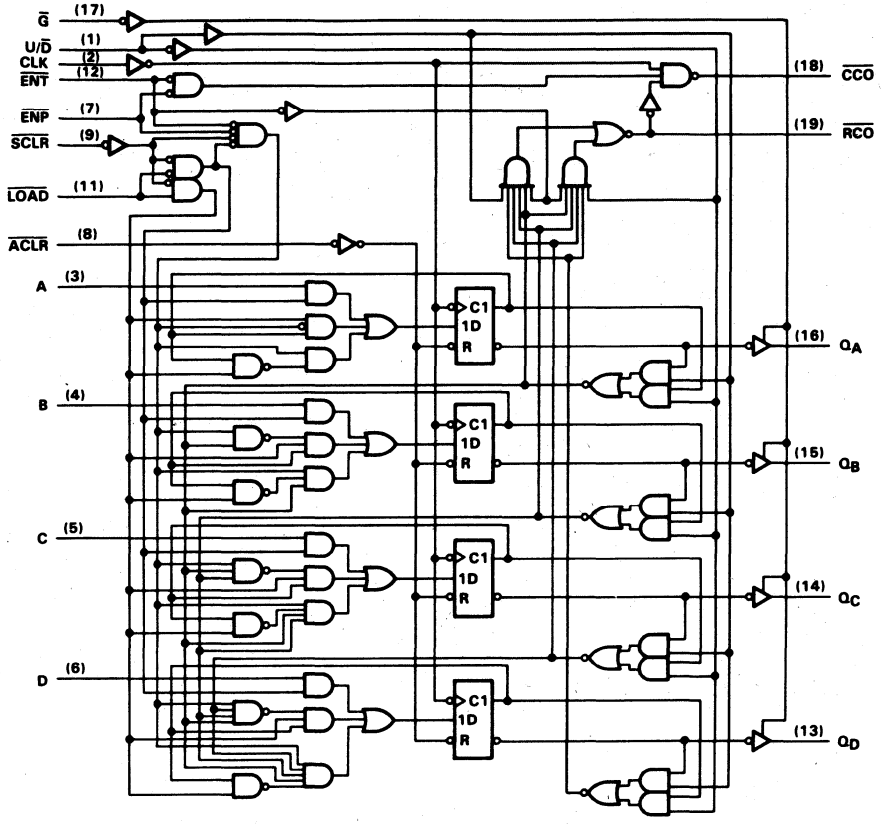
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

LS568A logic diagram (positive logic)



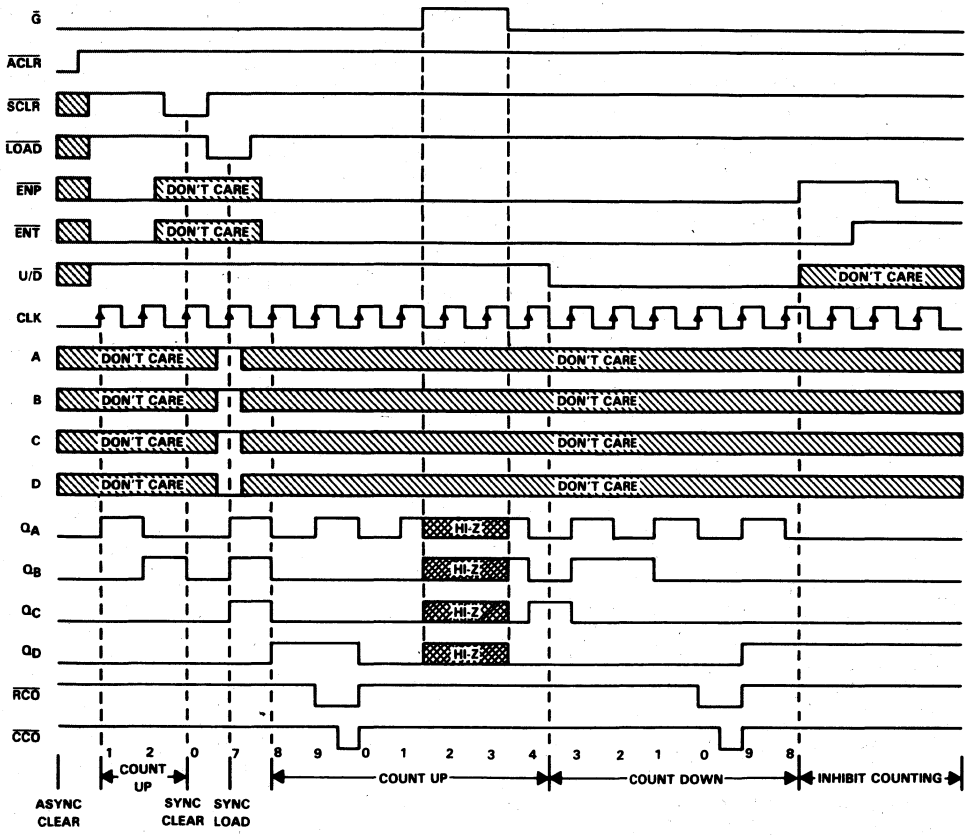
Pin numbers shown are for DW, J, and N packages.

'ALS569A logic diagram (positive logic)

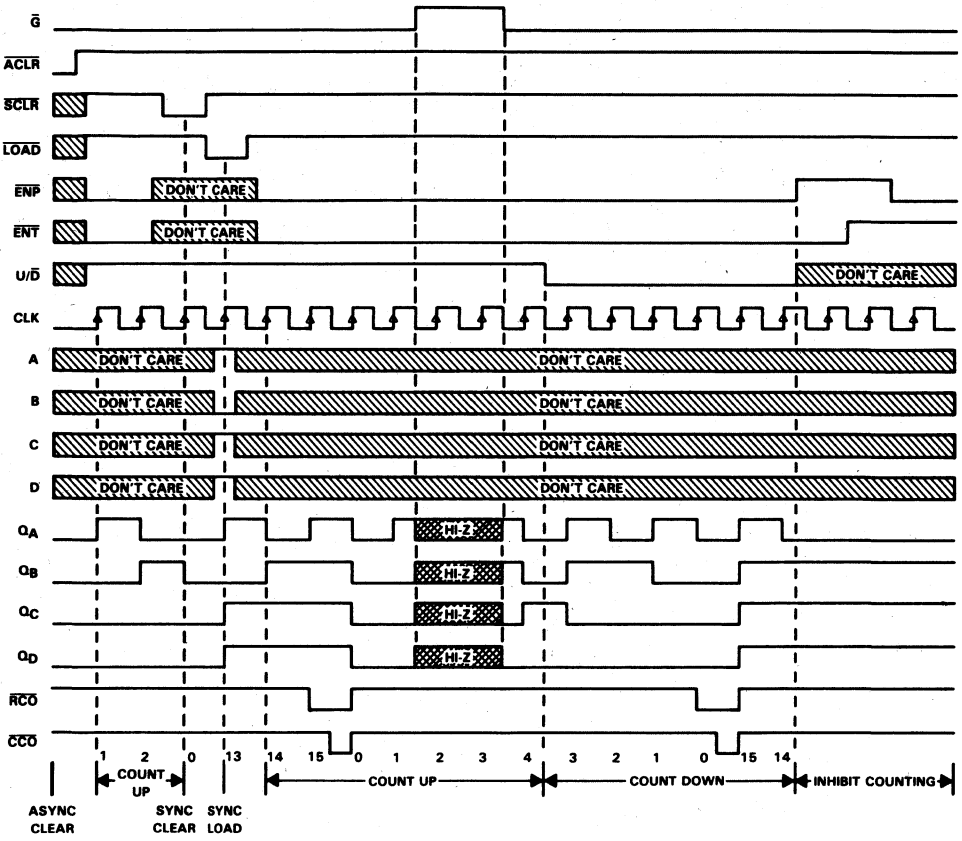


Pin numbers shown are for DW, J, and N packages.

'ALS568A typical load, count, and inhibit sequences



'ALS569A typical load, count, and inhibit sequences



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS569A . . . . . −55°C to 125°C
SN74ALS568A, SN74ALS569A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54ALS569A			SN74ALS568A SN74ALS569A			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltge					0.7			0.8	C
I_{OH}	High-level output current	Q outputs				−1			−2.6	mA
		$\overline{CCO}$ and $\overline{RCO}$				−0.4			−0.4	
I_{OL}	Low-level output current	Q outputs				12			24	mA
		$\overline{CCO}$ and $\overline{RCO}$				4			8	
f_{clock}	Clock frequency	'ALS568A		0		18	0		20	MHz
		'ALS569A		0		22	0		30	
t_w	Pulse duration	$\overline{ALCR}$ or $\overline{LOAD}$ low		20			15			ns
		'ALS568A	CLK high				25			
			CLK low				25			
		'ALS569A	CLK high	20			16.5			
			CLK low	20			16.5			
t_{su}	Setup time before CLK ↑	Data at A, B, C, D		25			20			ns
		$\overline{ENP}$, $\overline{ENT}$	High	35			30			
			Low	25			20			
		$\overline{SCLR}$	Low	20			15			
			High (inactive)	35			30			
		$\overline{LOAD}$	Low	20			15			
			High (inactive)	35			30			
		$\overline{U/D}$		35			30			
		$\overline{ACLR}$ inactive		10			10			
t_h	Hold time after CLK↑ for any input			0			0			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS569A			SN74ALS568A SN74ALS569A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
	$\overline{CCO}$ and $\overline{RCO}$	V_{CC} = 4.5 V,	I_{OH} = 4 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	$\overline{CCO}$ and $\overline{RCO}$	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
	Q outputs			−30		−112	−30		−112	
I_{CC}		V_{CC} = 5.5 V	Outputs high		16	26		16	26	mA
			Outputs low		20	32		20	32	
			Outputs disabled		20	32		20	32	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS569A		SN74ALS568A SN74ALS569A		
			MIN	MAX	MIN	MAX	
f_{max}	'ALS568A		18		20		MHz
	'ALS569A		22		30		
t_{PLH}	CLK	Any Q	4	21	4	13	ns
t_{PHL}			7	19	7	16	
t_{PLH}	CLK	$\overline{RCO}$	12	37	12	28	ns
t_{PHL}			10	28	10	19	
t_{PLH}	CLK	$\overline{CCO}$	5	17	5	13	ns
t_{PHL}			6	30	6	25	
t_{PLH}	U/$\overline{D}$	$\overline{RCO}$	9	31	9	23	ns
t_{PHL}			9	33	9	19	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	6	21	6	15	ns
t_{PHL}			4	20	4	13	
t_{PLH}	$\overline{ENT}$	$\overline{CCO}$	5	18	5	13	ns
t_{PHL}			9	32	9	23	
t_{PLH}	$\overline{ENP}$	$\overline{CCO}$	4	18	4	12	ns
t_{PHL}			5	18	5	14	
t_{PHL}	$\overline{ACLR}$	Any Q	9	25	9	20	ns
t_{PZH}	$\overline{G}$	Any Q	6	23	6	18	ns
t_{PZL}			6	29	6	24	
t_{PHZ}	$\overline{G}$	Any Q	1	12	1	10	ns
t_{PLZ}			3	29	3	13	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982 – REVISED SEPTEMBER 1989

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Choice of True or Inverting Logic**

  'ALS573, 'AS573A True Outputs
  'ALS580, 'AS580 Inverting Outputs
- **Package-Options Include Ceramic Chip Carriers in Addition to Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

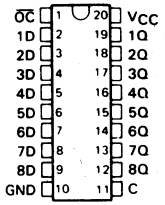
The eight latches are transparent D-type latches. While the enable (C) is high the outputs (Q or Q) will respond to the data (D) inputs. When the enable is taken low the outputs will be latched to retain the data that was set up.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

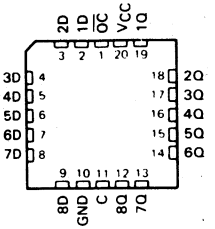
The output control (OC) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are at high impedance.

The SN54ALS' and SN54AS' devices are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS' and SN74AS' devices are characterized for operation from 0°C to 70°C.

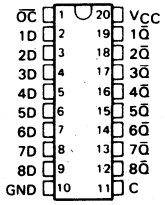
SN54ALS573B, SN54AS573A . . . J PACKAGE
SN74ALS573C, SN74AS573 . . . DW OR N PACKAGE
(TOP VIEW)



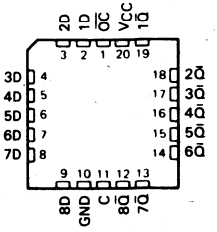
SN54ALS573B, SN54AS573A . . . FK PACKAGE
(TOP VIEW)



SN54ALS580A . . . J PACKAGE
SN74ALS580B, SN74AS580 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS580A . . . FK PACKAGE
(TOP VIEW)



TEXAS INSTRUMENTS

FUNCTION TABLES

'ALS573, 'AS573A
(EACH LATCH)

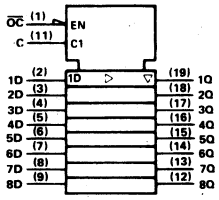
INPUTS			OUTPUT
ENABLE			
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

'ALS580, 'AS580
(EACH LATCH)

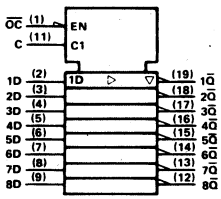
INPUTS			OUTPUT
ENABLE			
$\overline{OC}$	C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic symbols†

'ALS573, 'AS573A



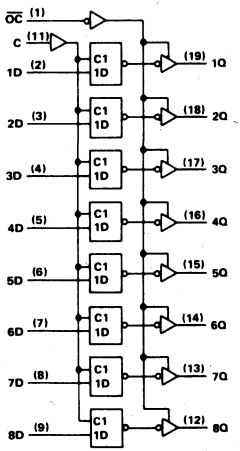
'ALS580, 'AS580



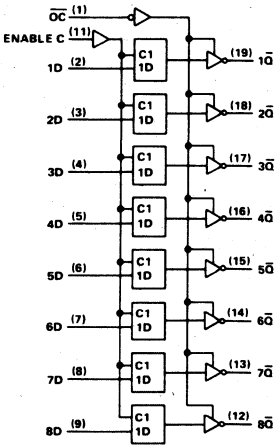
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

'ALS573, 'AS573A



'ALS580, 'AS580



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range; SN54ALS573B, SN54ALS580A . . . . . −55°C to 125°C
SN74ALS573C, SN74ALS580B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS573B SN54ALS580A			SN74ALS573C SN74ALS580B			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration, enable C high	'ALS573	10			10			ns
		'ALS580	15			15			
t_{su}	Setup time, data before enable C↓		10			10			ns
t_h	Hold time, data after enable C↓	'ALS573	7			7			ns
		'ALS580	10			10			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS573B SN54ALS580A			SN74ALS573C SN74ALS580B			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V,			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS573	V_{CC} = 5.5 V	Outputs high		10	17		10	17	mA
			Outputs low		15	24		15	24	
			Outputs disabled		16	27		16	27	
	'ALS580		Outputs high		10	17		10	17	
			Outputs low		16	26		16	26	
			Outputs disabled		17	29		17	29	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS573 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS573	SN54ALS573B		SN74ALS573C		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	7	2	15	2	14	ns
t_{PHL}			7	2	15	2	14	
t_{PLH}	C	Q	12	8	25	6	20	ns
t_{PHL}			12	8	20	6	19	
t_{PZH}	$\overline{OC}$	Q	9	4	21	3	18	ns
t_{PZL}			11	4	21	4	18	
t_{PHZ}	$\overline{OC}$	Q	5	2	12	1	10	ns
t_{PLZ}			7	3	18	1	15	

'ALS580 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS580	SN54ALS580A		SN74ALS580B		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	10	3	21	3	18	ns
t_{PHL}			8	3	15	3	14	
t_{PLH}	C	$\overline{Q}$	8	8	29	6	22	ns
t_{PHL}			14	8	22	6	21	
t_{PZH}	$\overline{OC}$	$\overline{Q}$	8	4	21	3	18	ns
t_{PZL}			10	4	21	4	18	
t_{PHZ}	$\overline{OC}$	$\overline{Q}$	5	2	12	1	10	ns
t_{PLZ}			7	3	18	1	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS573A . . . . . −55°C to 125°C
SN74AS573A, SN74AS580 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS573A			SN74AS573A SN74AS580			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			15	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration, enable C high	'AS573A	5.5			4.5			ns
		'AS580				2			
t_{su}	Setup time, data before enable C↓		2			2			ns
t_h	Hold time, data after enable C↓		3			3			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS573A			SN74AS573A SN74AS580			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.28	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.33	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V,			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS573A	V_{CC} = 5.5 V	Outputs high		56	93		56	93	mA
			Outputs low		55	90		55	90	
			Outputs disabled		65	106		65	106	
	'AS580		Outputs high					62	100	
			Outputs low					65	106	
			Outputs disabled					71	115	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS573A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS573A		SN74AS573A		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3	11	3	8	ns
t_{PHL}			3	8	3	7	
t_{PLH}	C	Q	6	16.5	6	13	ns
t_{PHL}			4	9	4	7.5	
t_{PZH}	$\overline{OC}$	Q	2	8	2	6.5	ns
t_{PZL}			4	11	4	9.5	
t_{PHZ}	$\overline{OC}$	Q	2	8	2	6.5	ns
t_{PLZ}			2	8	2	7	

Note 1: Load circuit and voltage waveforms are shown in Section 1.

'AS580 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			SN74AS580		
			MIN	MAX	
t_{PLH}	D	$\overline{Q}$	3	7.5	ns
t_{PHL}			3	7	
t_{PLH}	C	$\overline{Q}$	5	9	ns
t_{PHL}			4	8	
t_{PZH}	$\overline{OC}$	$\overline{Q}$	2	6.5	ns
t_{PZL}			4	9.5	
t_{PHZ}	$\overline{OC}$	$\overline{Q}$	2	6.5	ns
t_{PLZ}			2	7	

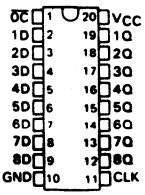
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN74ALS574B, SN74ALS575A, SN74AS574, SN74AS575
SN54ALS574A, SN54AS574, SN54AS575
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

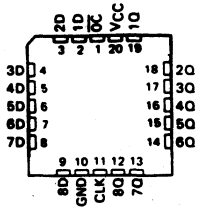
D2661, JUNE 1982 – REVISED JANUARY 1989

- **3-State Buffer-Type Noninverting Outputs Drive Bus-Lines Directly**
- **Bus Structured Pinout**
- **Buffered Control Inputs**
- **'ALS575 and 'AS575 Have Synchronous Clear**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

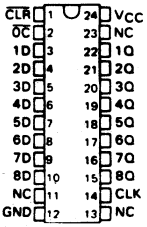
SN54ALS574A, SN54AS574 ... J PACKAGE
SN74ALS574B, SN74AS574 ... DW OR N PACKAGE
(TOP VIEW)



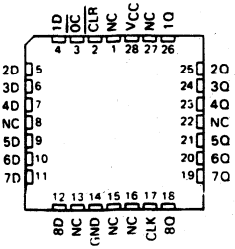
SN54ALS574A, SN54AS574 ... FK PACKAGE
(TOP VIEW)



SN54AS575 ... JT PACKAGE
SN74ALS575A, SN74AS575 ... DW OR NT PACKAGE
(TOP VIEW)



SN54AS575 ... FK PACKAGE
SN74ALS575A, SN74AS575 ... FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

These 8-bit registers feature three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock. The 'ALS575A and 'AS575 may be synchronously cleared by taking the $\overline{CLR}$ input low.

The output-control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS' and SN54AS' devices are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS' and SN74AS' devices are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLES

'ALS574, 'AS574
(EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

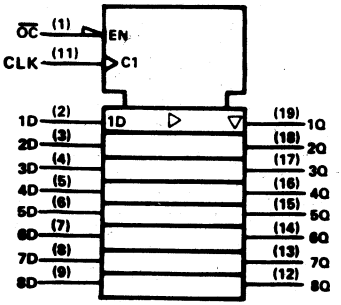
'ALS575, 'AS575
(EACH FLIP-FLOP)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	Q
L	L	↑	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

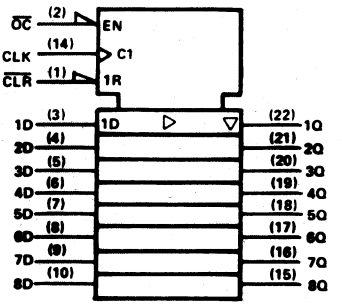
TEXAS INSTRUMENTS

logic symbols†

'ALS574, 'AS574



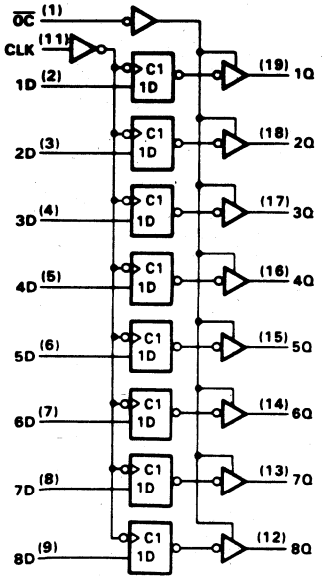
'ALS575, 'AS575



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

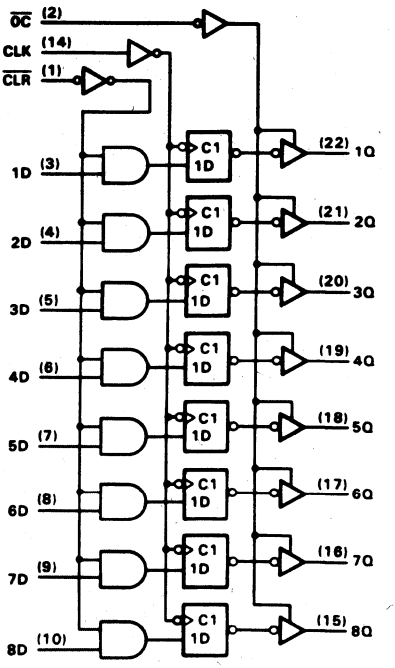
logic diagrams (positive logic)

'ALS574, 'AS574



Pin numbers shown are for DW, J, and N packages.

'ALS575, 'AS575



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS574A . . . . . −55°C to 125°C
SN74ALS574B, SN74ALS575A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS574A			SN74ALS574B SN74ALS575A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency	'ALS574	0		28	0		35	MHz
		'ALS575				0		30	
t_w	Pulse duration	'ALS574 CLK high or low	16.5			14			ns
		'ALS575 CLK high or low	20			16.5			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		'ALS575 $\overline{CLR}$				15			
t_h	Hold time after CLK↑	Data	4			0			ns
		'ALS575 $\overline{CLR}$				0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS574A			SN74ALS574B SN74ALS575A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O*		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS574	V_{CC} = 5.5 V	Outputs high		11	18		11	18	mA
			Outputs low		17	27		17	27	
			Outputs disabled		17	28		17	28	
	'ALS575		Outputs high		10	17		10	17	
			Outputs low		15	24		15	24	
			Outputs disabled		16	30		16	30	

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
* The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS574 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25 °C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS574	SN54ALS574A		SN74ALS574B		
			TYP	MIN	MAX	MIN	MAX	
fmax			50	28		35		MHz
tPLH	CLK	Q	8	4	22	3	14	ns
tPHL			8	4	17	4	14	
tPZH	$\overline{OC}$	Q	9	4	21	3	18	ns
tPZL			12	4	26	4	18	
tPHZ	$\overline{OC}$	Q	5	2	16	1	10	ns
tPLZ			5	2	25	2	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			'ALS575			SN74ALS575A		
				TYP		MIN	MAX	
f_{max}			40	50		30		MHz
t_{PLH}	CLK	Q		8	11	4	14	ns
t_{PHL}				9	11.5	4	14	
t_{PZH}	$\overline{OC}$	Q		11	14	4	18	ns
t_{PZL}				12	15	4	18	
t_{PHZ}	$\overline{OC}$	Q		6	8	2	10	ns
t_{PZL}				8	11	3	13	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS574, SN54AS575 . . . . . −55 °C to 125 °C
SN74AS574, SN74AS575 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

				SN54AS574 SN54AS575			SN74AS574 SN74AS575			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current					−12			−15	mA
I_{OL}	Low-level output current					32			48	mA
f_{clock}	Clock frequency			0		100	0		125	MHz
t_w	Pulse duration	CLK high		5			4			ns
		CLK low		4			2			
t_{su}	Setup time before CLK↑	Data		3			2			ns
		'ALS575	$\overline{CLR}$ high or low	6.5			5.5			
t_h	Hold time after CLK↑	Data		3			2			ns
		'ALS575	$\overline{CLR}$	0			0			
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS574 SN54AS575			SN74AS574 SN74AS575			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.29	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.34	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			‡20			20	μA
I_{IL}	$\overline{OC}$, CLK, $\overline{CLR}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	D					−3			−2	
I_O*		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS574	V_{CC} = 5.5 V	Outputs high		73	116		73	116	mA
			Outputs low		85	134		85	134	
			Outputs disabled		84	134		84	134	
	'ALS575		Outputs high		78	126		78	126	
			Outputs low		89	142		89	142	
			Outputs disabled		88	142		88	142	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

* The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS574 SN54AS575		SN74AS574 SN74AS575		
			MIN	MAX	MIN	MAX	
f_{max}			100		125		MHz
t_{PLH}	CLK	Any Q	3	11	3	8	ns
t_{PHL}			4	11	4	9	
t_{PZH}	$\overline{OC}$	Any Q	2	7	2	6	ns
t_{PZL}			3	11	3	10	
t_{PHZ}	$\overline{OC}$	Any Q	2	7	2	6	ns
t_{PLZ}			2	7	2	6	

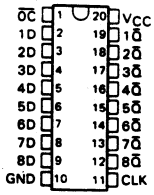
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

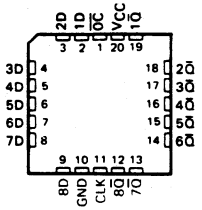
D2661, DECEMBER 1982 – REVISED JANUARY 1989

- **3-State Buffer-Type Inverting Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Buffered Control Inputs**
- **'ALS577A has Synchronous Clear**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

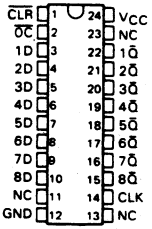
SN54ALS576A, SN54AS576 ... J PACKAGE
SN74ALS576B, SN74AS576 ... DW OR N PACKAGE
(TOP VIEW)



SN54ALS576A, SN54AS576 ... FK PACKAGE
(TOP VIEW)



SN74ALS577A ... DW OR NT PACKAGE
(TOP VIEW)



description

These 8-bit registers feature three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight-bit edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock.

The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS' and SN54AS' devices are characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS' and SN74AS' devices are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLES

'ALS576, 'AS576
(EACH FLIP-FLOP)

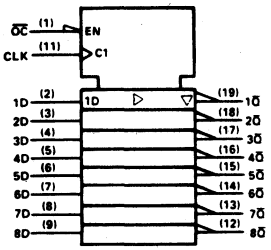
INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

'ALS577A
(EACH FLIP-FLOP)

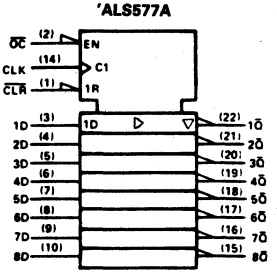
INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	$\overline{Q}$
L	L	↑	X	H
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

logic symbols†

'ALS576, 'AS576



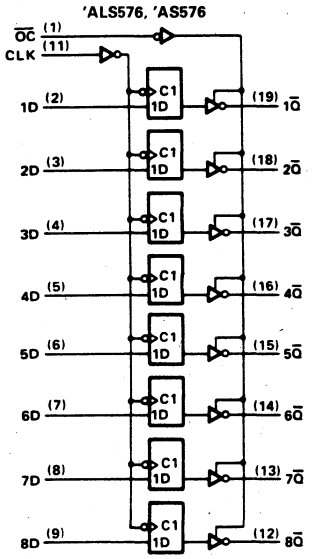
'ALS577A



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

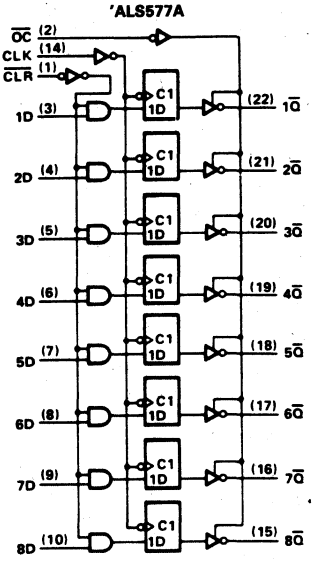
logic diagrams (positive logic)

'ALS576, 'AS576



Pin numbers shown are for DW, J, and N packages.

'ALS577A



Pin numbers shown are for DW, JT, and NT packages.

TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS', SN54AS' . . . . . −55 °C to 125 °C
SN74ALS', SN74AS' . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS576A			SN74ALS576B SN74ALS577A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency	'ALS576B	0		25	0		30	MHz
		'ALS577A				0		30	
t_w	Pulse duration	CLK high or low 'ALS576B	20			16.5			ns
		CLK high or low 'ALS577A				16.5			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		$\overline{CLR}$ ('ALS577A)				15			
t_h	Hold time after CLK↑	Data	4			0			ns
		$\overline{CLR}$ ('ALS577A)				0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS576A			SN74ALS576B SN74ALS577A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O*	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		10	18		10	18	mA
		Outputs low		15	24		15	24	
		Outputs disabled		16	30		16	30	

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
* The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS576 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'ALS576	SN54ALS576A		SN74ALS576B		
			TYP	MIN	MAX	MIN	MAX	
f_{max}			50	25		30		MHz
t_{PLH}	CLK	Any $\overline{Q}$	9	4	15	3	14	ns
t_{PHL}			9	4	15	4	14	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	11	4	21	3	18	ns
t_{PZL}			11	4	21	4	18	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$ 'ALS576	6	2	12	1	10	ns
t_{PLZ}		Any $\overline{Q}$	8	3	17	2	15	

'ALS577A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†		UNIT
			'ALS577A			SN74ALS577A		
			MIN	TYP	MAX	MIN	MAX	
f_{max}			40	50		30		MHz
t_{PLH}	CLK	Any $\overline{Q}$		9	11	4	14	ns
t_{PHL}				9	11.5	4	14	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$		11	15	4	18	ns
t_{PZL}				11	15	4	18	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$ 'ALS577		6	8	2	10	ns
t_{PLZ}		Any $\overline{Q}$		8	12	3	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

			SN54AS576			SN74AS576			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency		0		100	0		125	MHz
t_w	Pulse duration	CLK high	5			4			ns
		CLK low	4			2			
t_{su}	Setup time before CLK ↑	Data	3			2			ns
t_h	Hold time after CLK ↑	Data	3			2			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS576			SN74AS576			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.29	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.33	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	µA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	D	V_{CC} = 5.5 V,	V_I = 0.4 V			−3			−2	mA
	All other					−0.5			−0.5	
I_O*		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS576	V_{CC} = 5.5 V	Outputs high		77	125		77	125	mA
			Outputs low		84	135		84	135	
			Outputs disabled		84	135		84	135	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
* The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS576		SN74AS576		
			MIN	MAX	MIN	MAX	
f_{max}			100		125		MHz
tPLH	CLK	Any $\overline{Q}$	3	11	3	8	ns
tPHL			4	11	4	9	
tPZH	$\overline{OC}$	Any $\overline{Q}$	2	7	2	6	ns
tPZL			3	11	3	10	
tPHZ	$\overline{OC}$	Any $\overline{Q}$	2	7	2	6	ns
tPLZ			2	7	2	6	

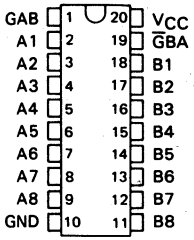
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, DECEMBER 1982 – REVISED OCTOBER 1991

- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Local Bus-Latch Capability**
- **Choice of True or Inverting Logic**
- **Choice of 3-State or Open-Collector Outputs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	OUTPUT	LOGIC
'ALS620A	3-State	Inverting
'ALS621A	Open-Collector	True
'ALS623A, 'AS623	3-State	True

SN74ALS', SN74AS' . . . DW OR N PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the octal bus transceivers the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

The -1 versions of the SN74ALS' parts are identical to their standard versions except that the recommended maximum I_{OL} is increased to 48 mA.

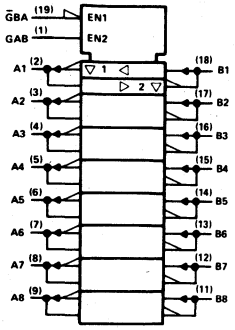
The SN74' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

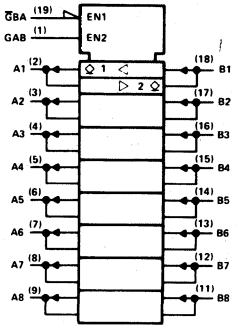
ENABLE INPUTS		OPERATION	
$\overline{G}$BA	GAB	'ALS620A	'ALS621A, 'ALS623A 'AS623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

logic symbols†

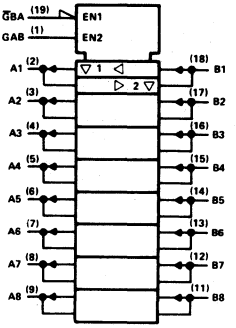
'ALS620A



'ALS621A



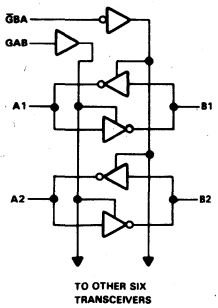
'ALS623A, 'AS623



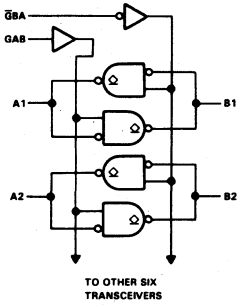
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagrams (positive logic)

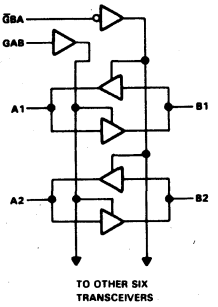
'ALS620A



'ALS621A



'ALS623A, 'AS623



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN74ALS620A, SN74ALS623A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74ALS620A SN74ALS623A			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			24	mA
				48†	
T_A	Operating free-air temperature	0		70	°C

† The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS623A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS620A SN74ALS623A			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA				
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA		0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	A or B ports §					20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
	A or B ports §					−0.1	
I_O†		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	'ALS620A	V_{CC} = 5.5 V	Outputs high		24	34	mA
			Outputs low		31	44	
			Outputs disabled		33	47	
	'ALS623A	V_{CC} = 5.5 V	Outputs high		32	43	
			Outputs low		39	50	
			Outputs disabled		42	55	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
† The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS620A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			SN74ALS620A		
			MIN	MAX	
t_{PLH}	A	B	2	10	ns
t_{PHL}			2	10	
t_{PLH}	B	A	2	10	ns
t_{PHL}			2	10	
t_{PZH}	$\overline{G}$BA	A	3	17	ns
t_{PZL}			5	25	
t_{PHZ}	$\overline{G}$BA	A	2	12	ns
t_{PLZ}			3	18	
t_{PZH}	GAB	B	3	18	ns
t_{PZL}			5	25	
t_{PHZ}	GAB	B	2	12	ns
t_{PLZ}			3	18	

'ALS623A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			SN74ALS623A		
			MIN	MAX	
t_{PLH}	A	B	2	13	ns
t_{PHL}			3	11	
t_{PLH}	B	A	2	13	ns
t_{PHL}			3	11	
t_{PZH}	$\overline{G}$BA	A	5	22	ns
t_{PZL}			5	22	
t_{PHZ}	$\overline{G}$BA	A	2	16	ns
t_{PLZ}			2	19	
t_{PZH}	GAB	B	5	22	ns
t_{PZL}			5	22	
t_{PHZ}	GAB	B	2	16	ns
t_{PLZ}			2	19	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range: SN74ALS621A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74ALS621A			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage			5.5	V
I_{OL}	Low-level output current			24	mA
				48†	
T_A	Operating free-air temperature	0		70	°C

† The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS621A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONTITIONS		SN74ALS621A			UNIT
				MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA		0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	A or B ports §					20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
	A or B ports §					−0.1	
I_{CC}		V_{CC} = 5.5 V	Outputs high		29	40	mA
			Outputs low		35	48	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'ALS621A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX		UNIT
			SN74ALS621A		
			MIN	MAX	
t_{PLH}	A	B	10	33	ns
t_{PHL}			5	20	
t_{PLH}	B	A	10	33	ns
t_{PHL}			5	20	
t_{PLH}	$\overline{G}BA$	A	10	39	ns
t_{PHL}			12	35	
t_{PLH}	GAB	B	10	39	ns
t_{PHL}			12	35	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN74AS623 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74AS623			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74AS623			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA				
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA		0.35	0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	A or B ports ‡					70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5	mA
	A or B ports ‡					−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		57	93	mA
			Outputs low		116	189	
			Outputs disabled		71	116	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS623 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			SN74AS623		
			MIN	MAX	
t_{PLH}	A	B	1	9	ns
t_{PHL}			1	8	
t_{PLH}	B	A	1	9	ns
t_{PHL}			1	8.5	
t_{PZH}	$\overline{G}$BA	A	2	11	ns
t_{PZL}			2	10	
t_{PHZ}	$\overline{G}$BA	A	1	7.5	ns
t_{PLZ}			1	11.5	
t_{PZH}	GAB	B	2	11.5	ns
t_{PZL}			2	11	
t_{PHZ}	GAB	B	1	7	ns
t_{PLZ}			1	9	

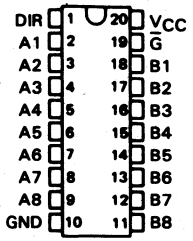
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN74ALS638A, SN74ALS639A, SN74AS638A, SN74AS639
OCTAL BUS TRANSCEIVERS

D2661, DECEMBER 1983 – REVISED MARCH 1987

- **Bidirectional Bus Transceivers in High-Density 20-Pin Packages**
- **Choice of True or Inverting Logic**
- **A Bus Outputs are Open-Collector; B Bus Outputs are 3-State**
- **Package Options Include Small Outline (SO) and Plastic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS', SN74AS' . . . DW OR N PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between open-collector and 3-state buses. The devices transmit data from the A bus (open-collector) to the B bus (3-state) or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are isolated.

DEVICE	A OUTPUT	B OUTPUT	LOGIC
'ALS638A, 'AS638A	Open-Collector	3-State	Inverting
'ALS639A, 'AS639	Open-Collector	3-State	True

The −1 versions of the SN74ALS' parts are identical to the standard versions except that recommended maximum of I_{OL} is increased to 48 milliamperes.

The SN74' family is characterized for operation from 0°C to 70°C.

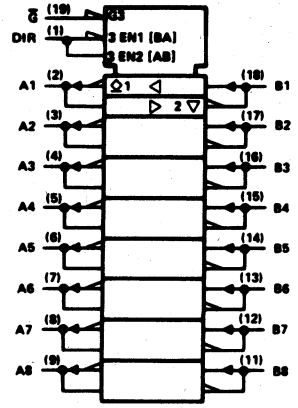
FUNCTION TABLE

CONTROL INPUTS		OPERATION	
$\overline{G}$	DIR	'ALS638A 'AS638A	'ALS639A 'AS639
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation

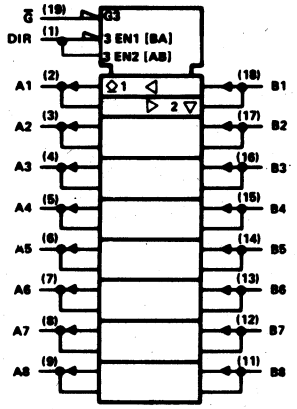
TEXAS INSTRUMENTS

logic symbols

'ALS638A, 'AS638A



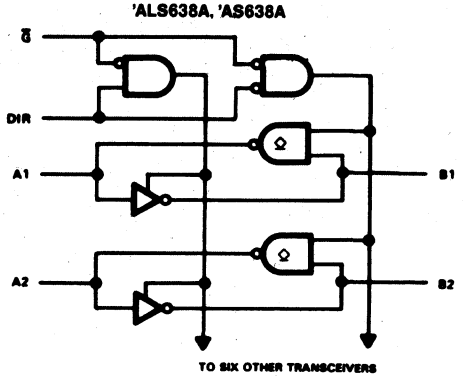
'ALS639A, 'AS639



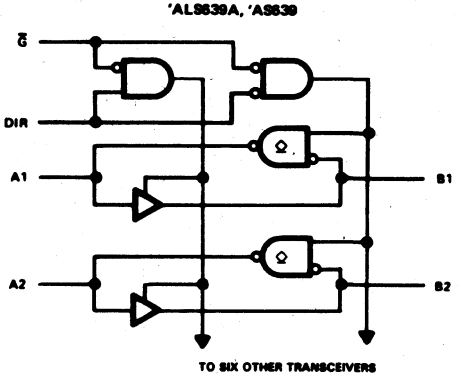
Pin numbers shown are for J and N packages.

functional block diagrams (positive logic)

'ALS638A, 'AS638A



'ALS639A, 'AS639



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
A bus I/O ports . . . . . 7 V
B bus I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN74ALS638A, SN74ALS639A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN74ALS638A SN74ALS639A			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage	A ports			5.5	V
I_{OH}	High-level output current	B ports			−15	mA
I_{OL}	Low-level output current	A or B ports			24	mA
					48†	
T_A	Operating free-air temperature		0		70	°C

† The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS638A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS638A SN74ALS639A			UNIT
				MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
I_{OH}	A ports	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1	mA
V_{OH}	B ports	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA				
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2			
V_{OL}	A or B ports	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA		0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	A or B ports §					20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
	A or B ports §					−0.1	
I_O†	B ports	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	'ALS638A	V_{CC} = 5.5 V	Outputs high		18	30	mA
			Outputs low		26	41	
			Outputs disabled		16	30	
	'ALS639A		Outputs high		25	40	
			Outputs low		30	50	
			Outputs disabled		33	54	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
† The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS638A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T_A = MIN to MAX		UNIT
			SN74ALS638A		
			MIN	MAX	
t_{PLH}	A	B	2	12	ns
t_{PHL}			2	12	
t_{PLH}	B	A	8	25	ns
t_{PHL}			8	30	
t_{PLH}	$\overline{G}$	A	5	25	ns
t_{PHL}			10	45	
t_{PZH}	$\overline{G}$	B	5	20	ns
t_{PZL}			5	22	
t_{PHZ}	$\overline{G}$	B	2	10	ns
t_{PLZ}			3	15	

'ALS639A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T_A = MIN to MAX		UNIT
			SN74ALS639A		
			MIN	MAX	
t_{PLH}	A	B	2	12	ns
t_{PHL}			2	12	
t_{PLH}	B	A	10	30	ns
t_{PHL}			5	22	
t_{PLH}	$\overline{G}$	A	10	30	ns
t_{PHL}			10	35	
t_{PZH}	$\overline{G}$	B	6	21	ns
t_{PZL}			8	25	
t_{PHZ}	$\overline{G}$	B	2	10	ns
t_{PLZ}			3	16	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
A bus I/O ports . . . . . 7 V
B bus I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN74AS638A, SN74AS639 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN74AS638A SN74AS639			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage	A ports			5.5	V
I_{OH}	High-level output current	B ports			−15	mA
I_{OL}	Low-level output current	A or B ports			64	mA
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74AS638A SN74AS639			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
I_{OH}	A ports	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1	mA
V_{OH}	B ports	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA				
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4			
V_{OL}	A or B ports	V_{CC} = 4.5 V,	I_{OL} = 48 mA				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA		0.35	0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	A or B ports ‡					50	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5	mA
	A or B ports ‡					−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	'AS638A	V_{CC} = 5.5 V	Outputs high		24	54	mA
			Outputs low		75	122	
			Outputs disabled		37	61	
	'AS639		Outputs high		56	92	
			Outputs low		95	154	
			Outputs disabled		62	100	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS638A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T_A = MIN to MAX		UNIT
			SN74AS638A		
			MIN	MAX	
t_{PLH}	A	B	2	7	ns
t_{PHL}			2	6.5	
t_{PLH}	B	A	5	20	ns
t_{PHL}			2	7	
t_{PLH}	$\overline{G}$	A	5	19	ns
t_{PHL}			2	9	
t_{PZH}	$\overline{G}$	B	2	8	ns
t_{PZL}			2	10	
t_{PHZ}	$\overline{G}$	B	2	7	ns
t_{PLZ}			2	10	

'AS639 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T_A = MIN to MAX		UNIT
			SN74AS639A		
			MIN	MAX	
t_{PLH}	A	B	2	9.5	ns
t_{PHL}			2	9	
t_{PLH}	B	A	5	22	ns
t_{PHL}			2	9	
t_{PLH}	$\overline{G}$	A	5	21.5	ns
t_{PHL}			2	11.5	
t_{PZH}	$\overline{G}$	B	2	10.5	ns
t_{PZL}			2	10.5	
t_{PHZ}	$\overline{G}$	B	2	7	ns
t_{PLZ}			2	10.5	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

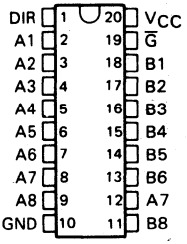
SN74ALS640B, SN74ALS641A, SN74ALS642A, SN74ALS645A, SN74AS640, SN74AS641, SN74AS645
SN54ALS640B, SN54ALS645A, SN54AS640, SN54AS645
OCTAL BUS TRANSCEIVERS

D2661, DECEMBER 1983 – REVISED APRIL 1987

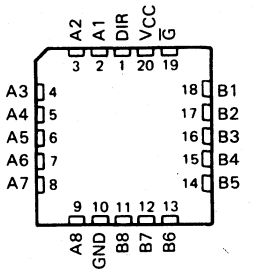
- **Bidirectional Bus Transceivers in High-Density 20-Pin Packages**
- **Choice of True or Inverting Logic**
- **Choice of 3-State or Open-Collector Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE		OUTPUT	LOGIC
'ALS640B,	'AS640	3-State	Inverting
'ALS641A,	'AS641	Open-Collector	True
'ALS642A,		Open-Collector	Inverting
'ALS645A,	'AS645	3-State	True

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are effectively isolated.

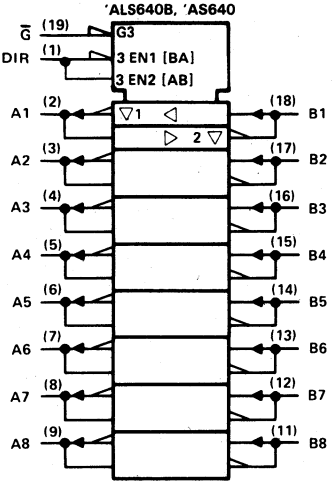
The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes.

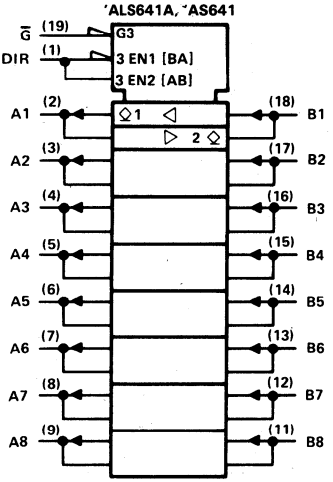
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

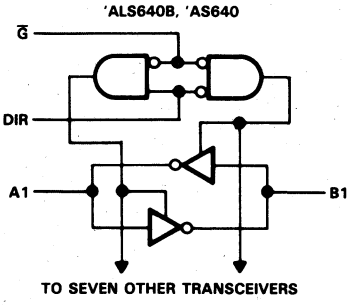
CONTROL INPUTS		OPERATION	
$\overline{G}$	DIR	'ALS640B, 'AS640 'ALS642A	'ALS641A, 'AS641 'ALS645A, 'AS645
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation

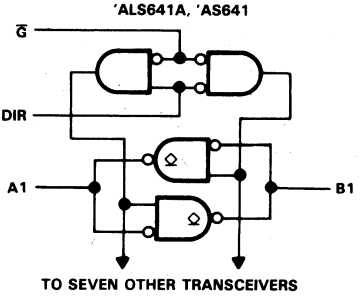
logic symbols†





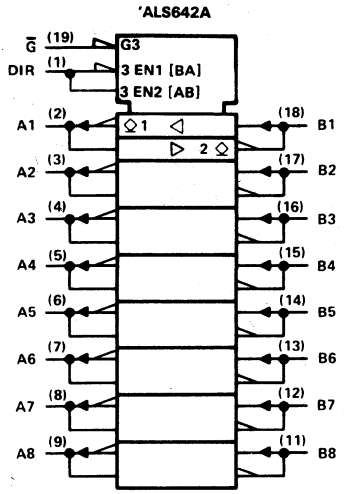
logic diagrams (positive logic)



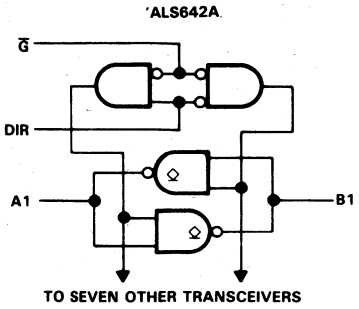


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic symbol†

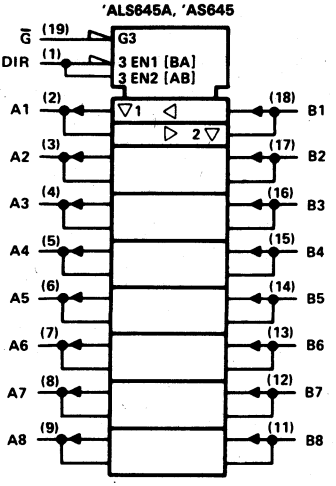


logic diagram (positive logic)

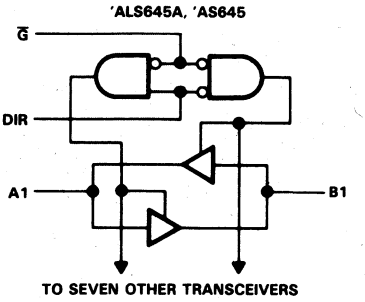


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW and N packages.

logic symbol†



logic diagram (positive logic)



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS640B, SN54ALS645A . . . . . −55°C to 125°C
SN74ALS640B, SN74ALS645A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS640B SN54ALS645A			SN74ALS640B SN74ALS645A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low -level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

† The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS640B-1 and SN74ALS645A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS'			SN74ALS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
	A or B ports §					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports §					−0.1			−0.1	
I_O†		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS640B	V_{CC} = 5.5 V	Outputs high		19	50		19	45	mA
			Outputs low		27	60		27	55	
			Outputs disabled		28	55		28	50	
	'ALS645A		Outputs high		30	48		30	45	
			Outputs low		36	60		36	55	
			Outputs disabled		38	63		38	58	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
† The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS640B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS640B		SN74ALS640B		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	14	2	11	ns
t_{PHL}			2	13	2	10	
t_{PZH}	$\overline{G}$	A or B	4	25	4	21	ns
t_{PZL}			5	27	5	24	
t_{PHZ}	$\overline{G}$	A or B	2	12	2	10	ns
t_{PLZ}			3	20	3	15	

'ALS645A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS645A		SN74ALS645A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	19	3	10	ns
t_{PHL}			1	14	3	10	
t_{PZH}	$\overline{G}$	A or B	2	30	5	20	ns
t_{PZL}			2	29	5	20	
t_{PHZ}	$\overline{G}$	A or B	2	14	2	10	ns
t_{PLZ}			2	30	4	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range: SN74ALS641A, SN74ALS642A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74ALS641A			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output current			5.5	V
I_{OL}	Low-level output current			24	mA
				48†	
T_A	Operating free-air temperature	0		70	°C

† The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS641A-1 and SN74ALS642A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS641A			UNIT
				MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA		0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	A or B ports §					20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
	A or B ports §					−0.1	
I_{CC}	'ALS641A	V_{CC} = 5.5 V	Outputs high		25	37	mA
			Outputs low		33	47	
	'ALS642A		Outputs high		8	15	
			Outputs low		18	28	
	'AS644A		Outputs high		16	29	
			Outputs low		25	40	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'ALS641A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX		UNIT
			SN74ALS641A		
			MIN	MAX	
t_{PLH}	A or B	B or A	5	25	ns
t_{PHL}			3	18	
t_{PLH}	$\overline{G}$	A or B	8	30	ns
t_{PHL}			8	30	
t_{PLH}	DIR	A or B	8	32	ns
t_{PHL}			8	32	

'ALS642A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX		UNIT
			SN74ALS642A		
			MIN	MAX	
t_{PLH}	A	B	10	30	ns
t_{PHL}			5	22	
t_{PLH}	$\overline{G}$ or DIR	A or B	10	30	ns
t_{PHL}			15	38	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS640, SN54AS645 . . . . . −55°C to 125°C
SN74AS640, SN74AS645 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS640 SN54AS645			SN74AS640 SN74AS645			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS'			SN74AS'			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.30	0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.35	0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
	A or B ports ‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports ‡					−0.75			−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{CC}	'AS640	V_{CC} = 5.5 V	Outputs high		37	58		37	58	mA
			Outputs low		78	123		78	123	
			Outputs disabled		51	80		51	80	
	'AS645		Outputs high		62	97		62	97	
			Outputs low		95	149		95	149	
			Outputs disabled		79	123		79	123	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS640 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS640		SN74AS640		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	8	2	7	ns
t_{PHL}			2	7	2	6	
t_{PZH}	$\overline{G}$	A or B	2	10	2	8	ns
t_{PZL}			2	12	2	10	
t_{PHZ}	$\overline{G}$	A or B	2	9	2	8	ns
t_{PLZ}			2	16	2	13	

'AS645 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS645		SN74AS645		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	11	2	9.5	ns
t_{PHL}			2	10.5	2	9	
t_{PZH}	$\overline{G}$	A or B	2	12	2	11	ns
t_{PZL}			2	12	2	10	
t_{PHZ}	$\overline{G}$	A or B	2	8	2	7	ns
t_{PLZ}			2	13	2	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range: SN74AS641 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74AS641			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output current			5.5	V
I_{OL}	Low-level output current			64	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74AS641			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA		0.35	0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	A or B ports ‡					70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5	mA
	A or B ports ‡					−0.75	
I_{CC}		V_{CC} = 5.5 V	Outputs high		50	82	mA
			Outputs low		84	136	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

switching characteristics (see Note 1)

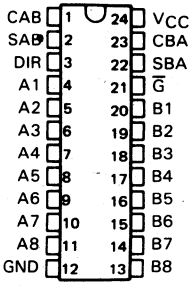
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX		UNIT
			SN74AS641		
			MIN	MAX	
t_{PLH}	A or B	B or A	5	21	ns
t_{PHL}			1	7.5	
t_{PLH}	$\overline{G}$	A or B	5	21	ns
t_{PHL}			1	9	
t_{PLH}	DIR	A or B	5	22	ns
t_{PHL}			1	10	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

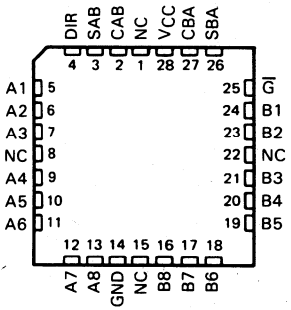
- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Choice of True or Inverting Data Paths**
- **3-State Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

DEVICE	OUTPUT	LOGIC
'ALS646, 'AS646	3-State	True
'ALS648, 'AS648	3-State	Inverting

SN54ALS', SN54AS' . . . JT PACKAGE
SN74ALS', SN74AS' . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

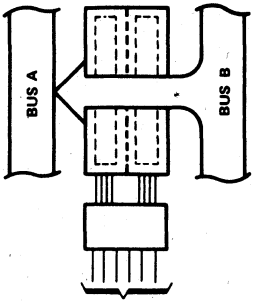
These devices consist of bus transceiver circuits, with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low). In the isolation mode (control $\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

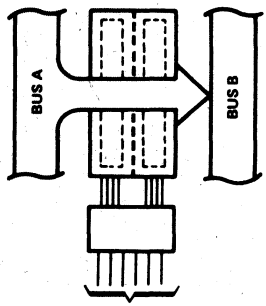
The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes.

The SN54' familiy is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.



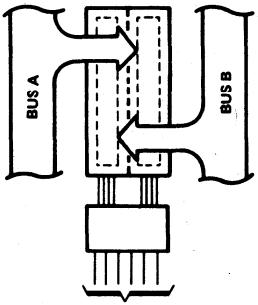
(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



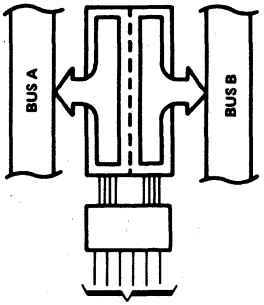
(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	HorL	X	H
L	H	HorL	X	H	X

TRANSFER
STORED DATA
TO A OR B

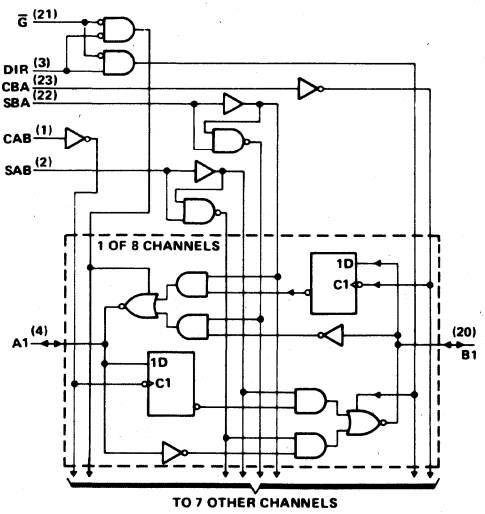
FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'ALS646, 'AS646	'ALS648, 'AS648
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Store $\overline{A}$ Data to B Bus

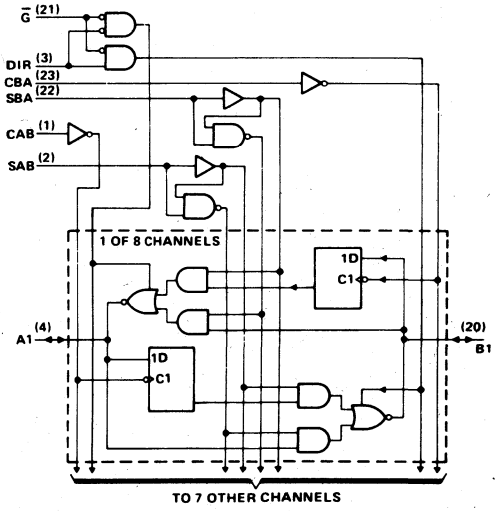
†The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

functional block diagrams (positive logic)

'ALS646, 'AS646



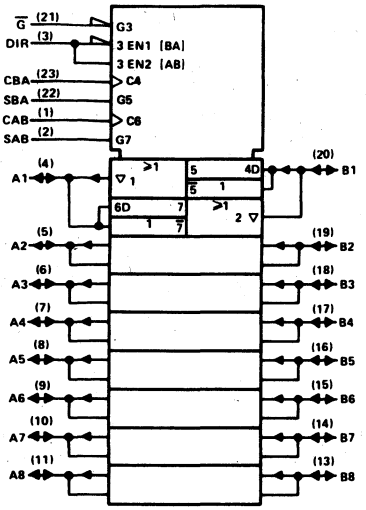
'ALS648, 'AS648



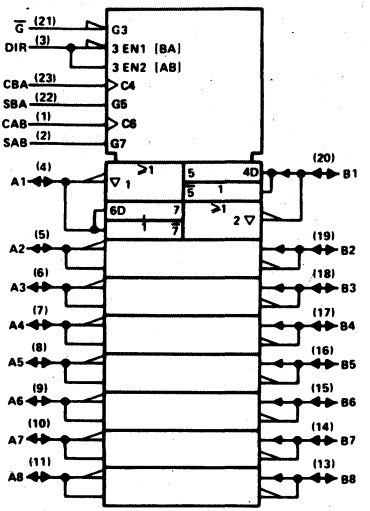
Pin numbers shown are for DW, JT, and NT packages.

logic symbols†

'ALS646, 'AS646



'ALS648, 'AS648



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS646 . . . . . −55°C to 125°C
SN74ALS646 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS646			SN74ALS646			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
f_{clock}	Clock frequency	0		35	0		40	MHz
t_w	Pulse duration, clocks high or low	14.5			12.5			ns
t_{su}	Setup time, A before CAB↑ or B before CBA↑	15			10			ns
t_h	Hold time, A after CAB↑ or B after CBA↑	1			0			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS646-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS646			SN74ALS646			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 version)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	A or B ports§					−0.2			−0.2	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		47	76		47	76	mA
			Outputs low		55	88		55	88	
			Outputs disabled		55	88		55	88	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS646 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS646		SN74ALS646		
			MIN	MAX	MIN	MAX	
f_{max}			35		40		MHz
t_{PLH}	CBA or CAB	A or B	10	35	10	30	ns
t_{PHL}			5	20	5	17	
t_{PLH}	A or B	B or A	5	22	5	20	ns
t_{PHL}			3	15	3	12	
t_{PLH}	SBA or SAB† (with A or B low)	A or B	10	40	15	35	ns
t_{PHL}			5	23	5	20	
t_{PLH}	SBA or SAB† (with A or B high)	A or B	8	30	8	25	ns
t_{PHL}			5	24	5	20	
t_{PZH}	$\overline{G}$	A or B	3	20	3	17	ns
t_{PZL}			5	22	5	20	
t_{PHZ}	$\overline{G}$	A or B	1	12	1	10	ns
t_{PLZ}			1	20	2	16	
t_{PZH}	DIR	A or B	5	38	8	30	ns
t_{PZL}			5	30	5	25	
t_{PHZ}	DIR	A or B	1	12	1	10	ns
t_{PLZ}			2	21	2	16	

†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: Load circuit and voltage waveforms are shown in Figure 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS648 . . . . . −55°C to 125°C
SN74ALS648 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS648			SN74ALS648			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
f_{clock}	Clock frequency	0		35	0		40	MHz
t_w	Pulse duration, clocks high or low	14.5			12.5			ns
t_{su}	Setup time, A before CAB↑ or B before CBA↑	15			10			ns
t_h	Hold time, A after CAB↑ or B after CBA↑	0			0			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS648			SN74ALS648			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 version)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	A or B ports§					−0.2			−0.2	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		47	76		47	76	mA
			Outputs low		57	88		57	88	
			Outputs disabled		57	88		57	88	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS648 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS648		SN74ALS648		
			MIN	MAX	MIN	MAX	
f_{max}			35		40		MHz
t_{PLH}	CBA or CAB	A or B	8	39	8	33	ns
t_{PHL}			5	23	5	20	
t_{PLH}	A or B	B or A	3	20	3	17	ns
t_{PHL}			2	12	2	10	
t_{PLH}	SBA or SAB† (with A or B low)	A or B	5	44	5	39	ns
t_{PHL}			4	26	4	22	
t_{PLH}	SBA or SAB† (with A or B high)	A or B	6	30	6	25	ns
t_{PHL}			6	25	6	21	
t_{PZH}	$\overline{G}$	A or B	4	25	4	22	ns
t_{PZL}			4	25	4	22	
t_{PHZ}	$\overline{G}$	A or B	1	12	1	10	ns
t_{PLZ}			2	21	2	15	
t_{PZH}	DIR	A or B	4	35	4	27	ns
t_{PZL}			3	25	3	19	
t_{PHZ}	DIR	A or B	1	17	1	14	ns
t_{PLZ}			2	22	2	15	

†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: Load circuit and voltage waveforms are shown in Figure 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS646 . . . . . −55°C to 125°C
SN74AS646, SN74AS648 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS646			SN74AS646			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency		0		75	0		90	MHz
t_w	Pulse duration	Clock high	6			5			ns
		Clock low	7			6			
t_{su}	Setup time, A before CAB↑ or B before CBA↑		7			6			ns
t_h	Hold time, A after CAB↑ or B after CBA↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS646			SN74AS646			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.50				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.50	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports§					−0.75			−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS646	V_{CC} = 5.5 V	Outputs high		120	196		120	195	mA
			Outputs low		130	211		130	211	
			Outputs disabled		130	211		130	211	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS646 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS646		SN74AS646		
			MIN	MAX	MIN	MAX	
f_{max}			75		90		MHz
t_{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	11.5	2	9	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SAB†	A or B	2	13.5	2	11	ns
t_{PHL}			2	11	2	9	
t_{PZH}	$\overline{G}$	A or B	2	11	2	9	ns
t_{PZL}			3	15	3	14	
t_{PHZ}	$\overline{G}$	A or B	2	11	2	9	ns
t_{PLZ}			2	11	2	9	
t_{PZH}	DIR	A or B	3	21	3	16	ns
t_{PZL}			3	24	3	18	
t_{PHZ}	DIR	A or B	2	12	2	10	ns
t_{PLZ}			2	12	2	10	

recommended operating conditions

			SN74AS648			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−15	mA
I_{OL}	Low-level output current				48	mA
f_{clock}	Clock frequency		0		90	MHz
t_w	Pulse duration	Clock high	5			ns
		Clock low	6			
t_{su}	Setup time, A before CAB↑ or B before CBA↑		6			ns
t_h	Hold time, A after CAB↑ or B after CBA↑		0			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74AS648			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA				
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.50	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	A or B ports ‡					70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5	mA
	A or B ports §					−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		110	185	mA
			Outputs low		120	195	
			Outputs disabled		120	195	

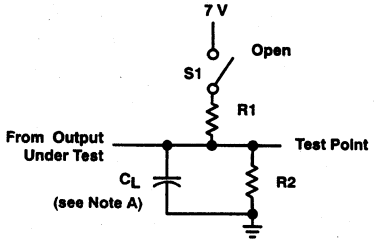
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			SN74AS648		
			MIN	MAX	
f_{max}			90		MHz
t_{PLH}	CBA or CAB	A or B	2	8.5	ns
t_{PHL}			2	9	
t_{PLH}	A or B	B or A	2	8	ns
t_{PHL}			1	7	
t_{PLH}	SBA or SAB†	A or B	2	11	ns
t_{PHL}			2	9	
t_{PZH}	$\overline{G}$	A or B	2	9	ns
t_{PZL}			3	15	
t_{PHZ}	$\overline{G}$	A or B	2	9	ns
t_{PLZ}			2	9	
t_{PZH}	DIR	A or B	3	16	ns
t_{PZL}			3	18	
t_{PHZ}	DIR	A or B	2	10	ns
t_{PLZ}			2	10	

†These parameters are measured with the internal output state of the storage register opposite of that of the bus input.
NOTE 1: Load circuit and voltage waveforms are shown in Figure 1.

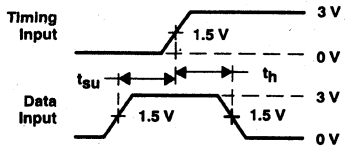
PARAMETER MEASUREMENT INFORMATION



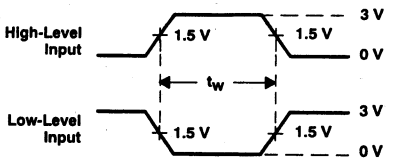
LOAD CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION TABLE

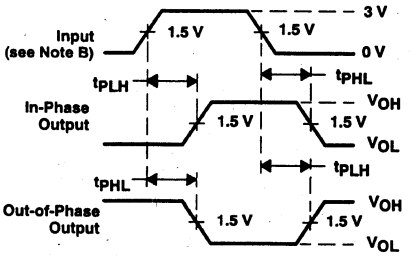
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



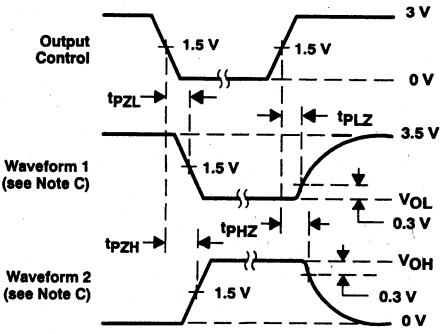
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

Notes: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. Waveform 1 is for an output with internal conditions such that the otuput is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

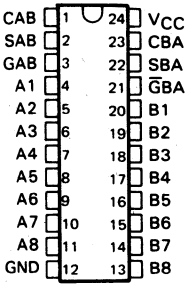
OCTAL BUS TRANSCEIVERS AND REGISTERS

D2661, DECEMBER 1983 – REVISED JANUARY 1990

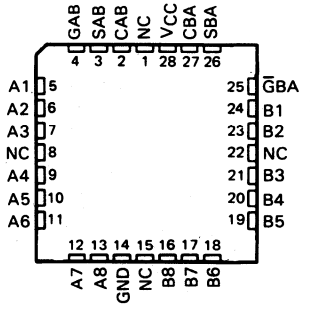
- **Bus Transceivers/Registers**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Choice of True and Inverting Data Paths**
- **Choice of 3-State or Open-Collector Outputs to A Bus**
- **Package Options Include Plastic "Small Outline" Packages, Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

DEVICE	A OUTPUT	B OUTPUT	LOGIC
'ALS651, 'AS651	3-State	3-State	Inverting
'ALS652, 'AS652	3-State	3-State	True
'ALS653	Open-Collector	3-State	Inverting
'ALS654	Open-Collector	3-State	True

SN54ALS', SN54AS' . . . JT PACKAGE
SN74ALS', SN74AS' . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

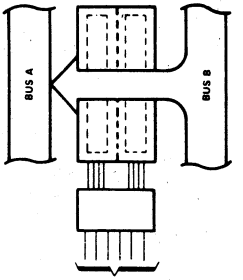
description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and $\overline{\text{GBA}}$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data, and a high selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{\text{GBA}}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

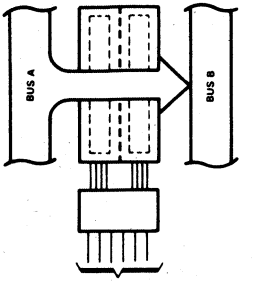
The -1 versions of the SN74ALS651 through SN74ALS653 are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54' series.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.



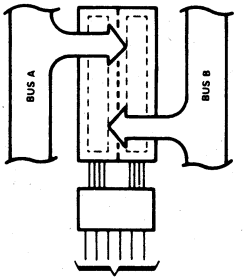
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



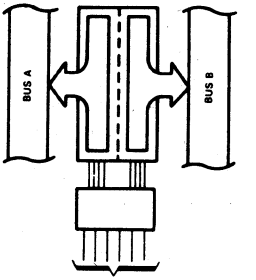
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A AND/OR B



GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER
STORED DATA
TO A AND/OR B

Figure 1. Bus Transfer Diagram

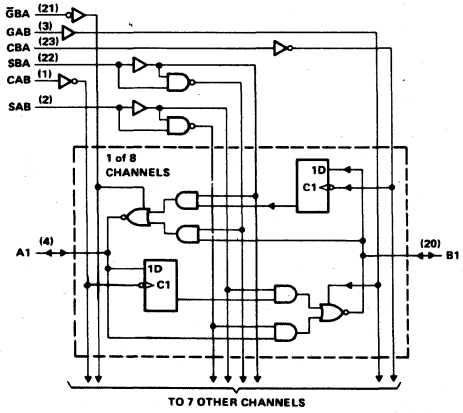
FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION	
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'ALS651, 'ALS653 'AS651	'ALS652, 'ALS654 'AS652
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified†	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified†	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

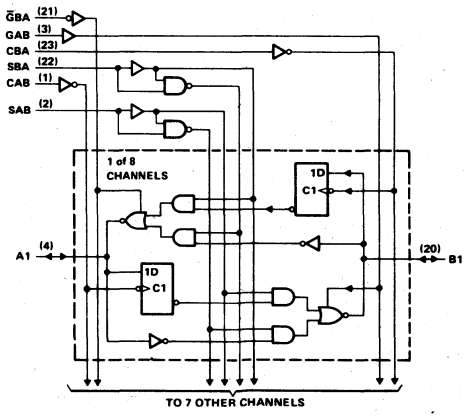
†The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
‡Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.

logic diagram (positive logic)

'ALS651, 'AS651, 'ALS653



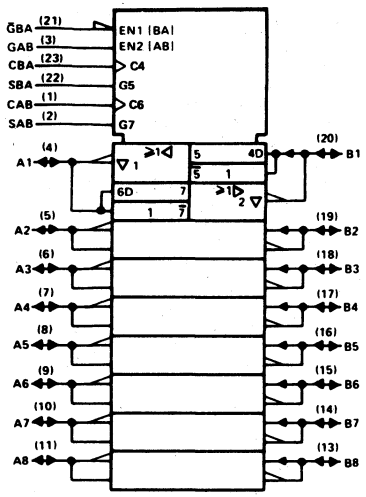
'ALS652, 'AS652, 'ALS654



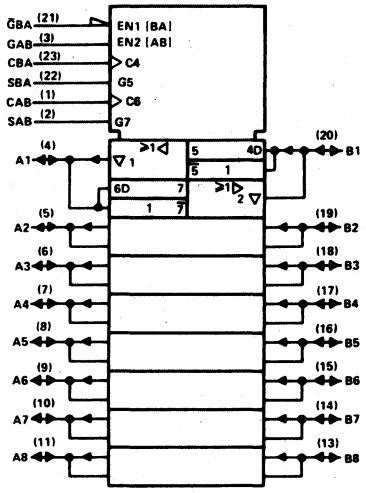
Pin numbers shown are for DW, JT, and NT packages.

logic symbols†

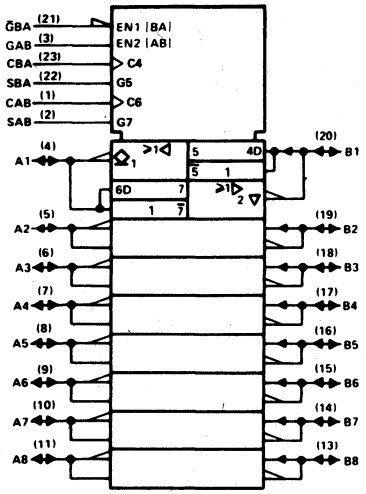
'ALS651, 'AS651



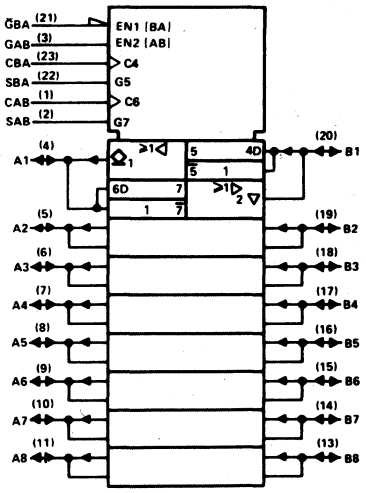
'ALS652, 'AS652



'ALS653



'ALS654



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS652 . . . . . −55°C to 125°C
SN74ALS651, SN74ALS652 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

'ALS651 recommended operating conditions

			SN74ALS651			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−15	mA
I_{OL}	Low-level output current				24	mA
					48†	
f_{clock}	Clock frequency		0		40	MHz
t_w	Pulse duration	CBA or CAB high	12.5			ns
		CBA or CAB low	12.5			
t_{su}	Setup time before CAB↑ or CBA↑	A or B	10			ns
t_h	Hold time after CAB↑ or CBA↑	A or B	0			ns
T_A	Operating free-air temperature		0		70	°C

'ALS652 recommended operating conditions

			SN54ALS652			SN74ALS652			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				12			24	mA
								48†	
f_{clock}	Clock frequency		0		35	0		40	MHz
t_w	Pulse duration	CBA or CAB high	14.5			12.5			ns
		CBA or CAB low	14.5			12.5			
t_{su}	Setup time before CAB↑ or CBA↑	A or B	15			10			ns
t_h	Hold time after CAB↑ or CBA↑	A or B	5			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†The 48-mA limit applies for the SN74ALS651-1 and SN74ALS652-1 and if V_{CC} is maintained between 4.75 V and 5.25 V.

'ALS651 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS651			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA				
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
		V_{CC} = 4.75 V, I_{OL} = 48 mA (−1 versions)					
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	A or B ports ‡					20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
	A or B ports ‡					−0.2	
I_O§	B ports	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	'ALS651	V_{CC} = 5.5 V	Outputs high		42	68	mA
			Outputs low		52	82	
			Outputs disabled		52	82	

'ALS652 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS652			SN74ALS652			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
		V_{CC} = 4.75 V, I_{OL} = 48 mA (−1 versions)								
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
	A or B ports‡					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	A or B ports‡					−0.2			−0.2	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS652	V_{CC} = 5.5 V	Outputs high		47	76		47	76	mA
			Outputs low		55	88		55	88	
			Outputs disabled		55	88		55	88	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS651 switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			SN74ALS651		
			MIN	MAX	
f_{max}			40		MHz
t_{PLH}	CBA or CAB	A or B	10	32	ns
t_{PHL}			5	17	
t_{PLH}	A or B	B or A	4	18	ns
t_{PHL}			2	10	
t_{PLH}	SBA or SAB† (with A or B high)	A or B	13	38	ns
t_{PHL}			7	21	
t_{PLH}	SBA or SAB† (with A or B low)	A or B	8	25	ns
t_{PHL}			7	21	
t_{PZH}	$\overline{G}$BA	A	5	20	ns
t_{PZL}			5	18	
t_{PHZ}	$\overline{B}$BA	A	2	9	ns
t_{PLZ}			3	12	
t_{PZH}	GAB	B	7	22	ns
t_{PZL}			7	21	
t_{PHZ}	GAB	B	2	12	ns
t_{PLZ}			2	14	

'ALS652 switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS652		SN74ALS652		
			MIN	MAX	MIN	MAX	
f_{max}			35		40		MHz
t_{PLH}	CBA or CAB	A or B	10	35	10	30	ns
t_{PHL}			5	20	5	17	
t_{PLH}	A or B	B or A	5	20	5	18	ns
t_{PHL}			3	15	3	12	
t_{PLH}	SBA or SAB† (with A or B high)	A or B	15	40	15	35	ns
t_{PHL}			6	23	6	20	
t_{PLH}	SBA or SAB† (with A or B low)	A or B	8	30	8	25	ns
t_{PHL}			5	24	5	20	
t_{PZH}	$\overline{G}$BA	A	3	20	3	17	ns
t_{PZL}			5	22	5	18	
t_{PHZ}	$\overline{G}$BA	A	1	12	1	10	ns
t_{PLZ}			2	20	2	16	
t_{PZH}	GAB	B	8	25	8	22	ns
t_{PZL}			6	21	6	18	
t_{PHZ}	GAB	B	1	12	1	10	ns
t_{PLZ}			2	21	2	16	

†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and A I/O ports . . . . . 7 V
B I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS653 . . . . . −55°C to 125°C
SN74ALS653, SN74ALS654 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

'ALS653 recommended operating conditions

			SN54ALS653			SN74ALS653			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	A ports			5.5			5.5	V
I_{OH}	High-level output current	B ports			−12			−15	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency	A ports	0		12.5	0		35	MHz
		B ports	0		25				
t_w	Pulse duration	CBA or CAB high	25			14.5			ns
		CBA or CAB low	25			14.5			
t_{su}	Setup time before CAB↑ or CBA↑	A or B	15			10			ns
t_h	Hold time after CAB↑ or CBA↑	A or B	5			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

'ALS654 recommended operating conditions

			SN74ALS654			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage	A ports			5.5	V
I_{OH}	High-level output current	B ports			−15	mA
I_{OL}	Low-level output current				24	mA
					48†	
f_{clock}	Clock frequency	A ports	0		35	MHz
		B ports				
t_w	Pulse duration	CBA or CAB high	14.5			ns
		CBA or CAB low	14.5			
t_{su}	Setup time before CAB↑ or CBA↑	A or B	10			ns
t_h	Hold time after CAB↑ or CBA↑	A or B	0			ns
T_A	Operating free-air temperature		0		70	°C

† The 48-mA limit applies for the SN74ALS653-1, only, if V_{CC} is maintained between 4.75 V and 5.25 V.

'ALS653 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS653 MIN	SN54ALS653 TYP†	SN54ALS653 MAX	SN74ALS653 MIN	SN74ALS653 TYP†	SN74ALS653 MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	B ports	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
I_{OH}	A ports	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.75 V,	I_{OL} = 24 mA					0.35	0.5	
		V_{CC} = 4.75 V, I_{OL} = 48 mA (-1 versions)								
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
	A or B ports‡					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	A or B ports‡					−0.2			−0.2	
I_O§	B ports	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS653	V_{CC} = 5.5 V	Outputs high		47	76		47	76	mA
			Outputs low		55	88		55	88	
			Outputs disabled		55	88		55	88	

'ALS654 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS654 MIN	SN74ALS654 TYP†	SN74ALS654 MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	B ports	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA				
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2			
I_{OH}	A ports	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.75 V,	I_{OL} = 24 mA		0.35	0.5	
		V_{CC} = 4.75 V, I_{OL} = 48 mA (−1 versions)					
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	A or B ports‡					20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
	A or B ports‡					−0.2	
I_O§	B ports	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	'ALS654	V_{CC} = 5.5 V	Outputs high		47	76	mA
			Outputs low		55	88	
			Outputs disabled		55	88	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 to 5.5 V, C_L = 50 pF, R_L = 680 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T_A = MIN to MAX				UNIT
			SN54ALS653		SN74ALS653		
			MIN	MAX	MIN	MAX	
f_{max}		A	12.5				MHz
		B	25				
t_{PLH}	CBA	A	16	71	16	64	ns
t_{PHL}			6	24	6	22	
t_{PLH}	CAB	B	10	35	10	30	ns
t_{PHL}			5	20	5	17	
t_{PLH}	A	B	5	20	5	18	ns
t_{PHL}			1.5	18	2	15	
t_{PLH}	B	A	8	63	12	56	ns
t_{PHL}			2	18	2	15	
t_{PLH}	SBA† (with B high)	A	19	68	19	62	ns
t_{PHL}			5	27	5	25	
t_{PLH}	SBA† (with B low)	A	19	68	19	62	ns
t_{PHL}			5	27	5	25	
t_{PLH}	SAB† (with A high)	B	8	30	15	35	ns
t_{PHL}			6	25	6	22	
t_{PLH}	SAB† (with A low)	B	12	40	8	25	ns
t_{PHL}			6	25	6	22	
t_{PLH}	$\overline{G}$BA	A	6	35	6	30	ns
t_{PHL}			6	27	6	24	
t_{PZH}	GAB	B	7	25	8	22	ns
t_{PZL}			6	25	6	22	
t_{PHZ}	GAB	B	1	16	1	14	ns
t_{PLZ}			2	21	2	16	

†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T_A = MIN to MAX		UNIT
			SN74ALS654		
			MIN	MAX	
f_{max}		A	35		MHz
		B			
t_{PLH}	CBA	A	16	64	ns
t_{PHL}			6	22	
t_{PLH}	CAB	B	10	30	ns
t_{PHL}			5	17	
t_{PLH}	A	B	5	18	ns
t_{PHL}			2	15	
t_{PLH}	B	A	12	56	ns
t_{PHL}			2	15	
t_{PLH}	SBA† (with B high)	A	19	62	ns
t_{PHL}			5	25	
t_{PLH}	SBA† (with B low)	A	19	62	ns
t_{PHL}			5	25	
t_{PLH}	SAB† (with A high)	B	15	35	ns
t_{PHL}			6	22	
t_{PLH}	SAB† (with A low)	B	8	25	ns
t_{PHL}			6	22	
t_{PLH}	$\overline{G}$BA	A	6	30	ns
t_{PHL}			6	24	
t_{PZH}	GAB	B	8	22	ns
t_{PZL}			6	22	
t_{PHZ}	GAB	B	1	14	ns
t_{PLZ}			2	16	

† These parameters are measured with the internal output state of the storage register opposite to that of the input.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS651, SN54ALS652 . . . . . −55°C to 125°C
SN74ALS651, SN74ALS652 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS651 SN54AS652			SN74AS651 SN74AS652			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency		0		75	0		90	MHz
t_w	Pulse duration	CBA or CAB high	6			5			ns
		CBA or CAB low	7			6			
t_{su}	Setup time before CAB↑ or CBA↑	A or B	7			6			ns
t_h	Hold time after CAB↑ or CBA↑	A or B	0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS651 SN54AS652			SN74AS651 SN74AS652			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.50				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.50	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.75			−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS651	V_{CC} = 5.5 V	Outputs high		110	185		110	185	mA
			Outputs low		120	195		120	195	
			Outputs disabled		130	195		130	195	
	'AS652		Outputs high		120	195		120	195	
			Outputs low		130	211		130	211	
			Outputs disabled		130	211		130	211	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS651 switching characteristics (see Figure 2)

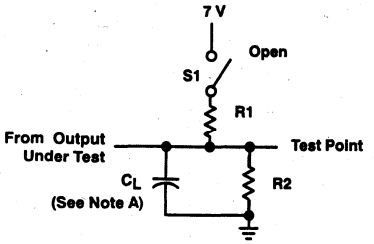
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS651		SN74AS651		
			MIN	MAX	MIN	MAX	
f_{max}			75		90		MHz
t_{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	9	2	8	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SAB†	A or B	2	12	2	11	ns
t_{PHL}			2	10	2	9	
t_{PZH}	$\overline{G}$BA	A	2	11	2	10	ns
t_{PZL}			3	18	3	16	
t_{PHZ}	$\overline{G}$BA	A	2	10	2	9	ns
t_{PLZ}			2	10	2	9	
t_{PZH}	GAB	B	3	12	3	11	ns
t_{PZL}			3	20	3	16	
t_{PHZ}	GAB	B	2	11	2	10	ns
t_{PLZ}			2	12	2	11	

'AS652 switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS652		SN74AS652		
			MIN	MAX	MIN	MAX	
f_{max}			75		90		MHz
t_{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	11	2	9	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SAB†	A or B	2	12	2	11	ns
t_{PHL}			2	10	2	9	
t_{PZH}	$\overline{G}$BA	A	2	11	2	10	ns
t_{PZL}			3	18	3	16	
t_{PHZ}	$\overline{G}$BA	A	2	10	2	9	ns
t_{PLZ}			2	10	2	9	
t_{PZH}	GAB	B	3	12	3	11	ns
t_{PZL}			3	20	3	16	
t_{PHZ}	GAB	B	2	11	2	10	ns
t_{PLZ}			2	12	2	11	

†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

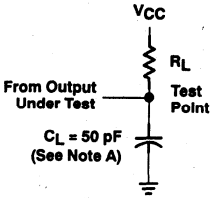
PARAMETER MEASUREMENT INFORMATION



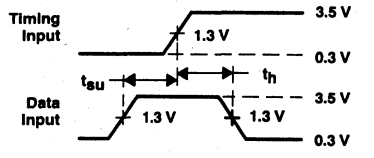
LOAD CIRCUIT FOR
3-STATE OUTPUTS

SWITCH POSITION TABLE

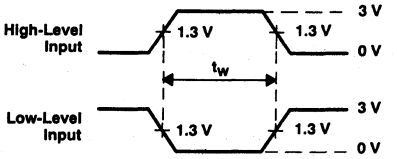
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



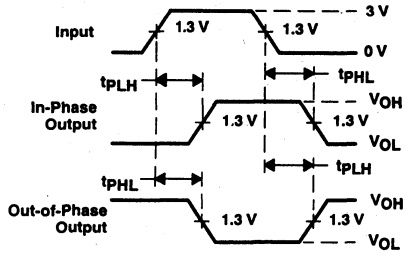
LOAD CIRCUIT FOR
OPEN-COLLECTOR OUTPUTS



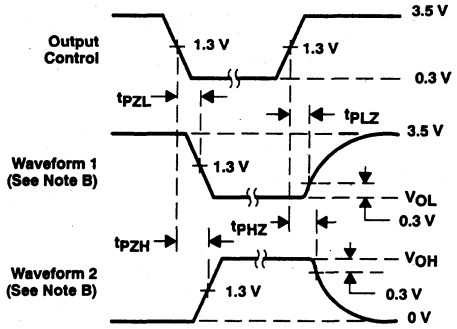
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLED TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. The outputs are measured one at a time with one transition per measurement.

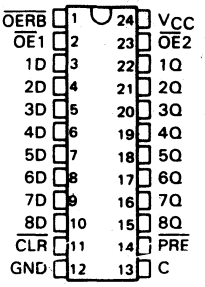
Figure 2. Load Circuits and Voltage Waveforms

SN74ALS666, SN74ALS667
8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

D2855, JUNE 1984 – REVISED MAY 1986

- **3-State I/O-Type Read-Back Inputs**
- **Bus-Structured Pinout**
- **Choice of True or Inverting Logic**
  'ALS666 . . . True Outputs
  'ALS667 . . . Inverting Outputs
- **Preset and Clear Inputs**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS666 . . . DW OR NT PACKAGE
(TOP VIEW)



description

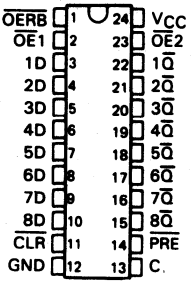
These 8-bit latches are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto the input data bus. In addition, they provide a 3-state buffer type output and are easily utilized in bus-structured applications.

The eight latches of the 'ALS666 and 'ALS667 are transparent D-type. While the enable (C) is high, the Q outputs of the 'ALS666 will follow the data (D) inputs. On the 'ALS667, the $\overline{Q}$ outputs will provide the inverse of what is applied to its data (D) inputs. On both devices, the Q or $\overline{Q}$ output will be in the high-impedance state if either output control, $\overline{OE}1$ or $\overline{OE}2$, is at a high logic level.

Read-back is provided thru the read-back control input ($\overline{OERB}$). When $\overline{OERB}$ is taken low, the data present at the output of the data latches will be allowed to pass back onto the input data bus. When it is taken high, the output of the data latches will be isolated from the data (D) inputs. The read-back control does not affect the internal operation of the latches; however, caution should be exercised not to create a bus-conflict situation.

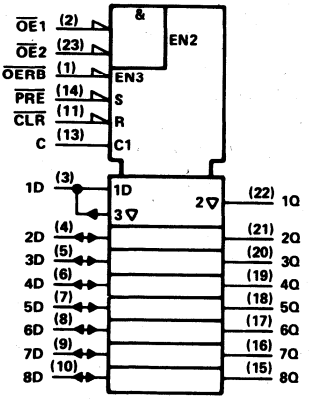
The SN74ALS666 and SN74ALS667 are characterized for operation from 0°C to 70°C.

SN74ALS667 . . . DW OR NT PACKAGE
(TOP VIEW)

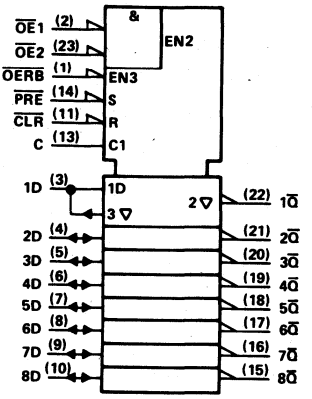


logic symbols†

'ALS666



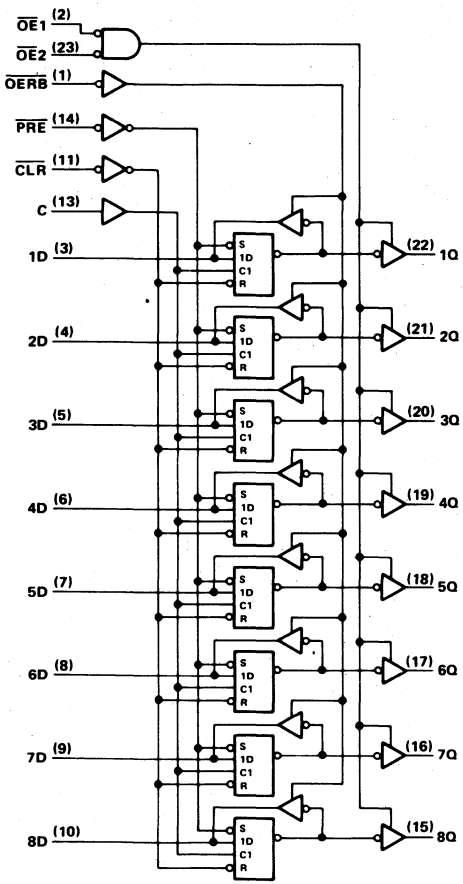
'ALS667



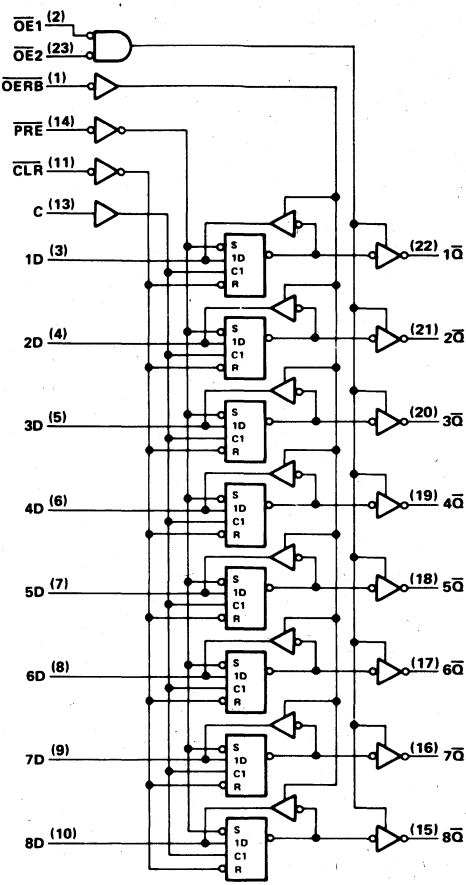
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12
Pin numbers shown are for DW and NT packages.

logic diagrams (positive logic)

'ALS666

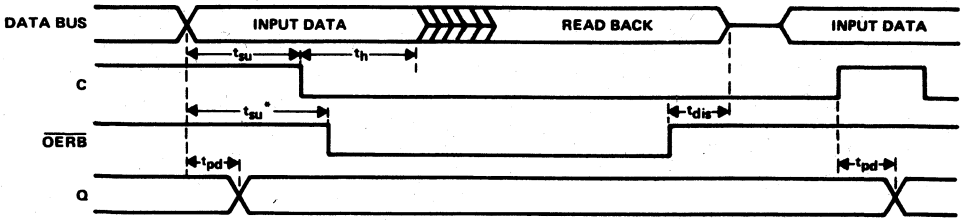


'ALS667



Pin numbers shown are for DW and NT packages.

timing diagram



$\overline{CLR}$ = H, $\overline{PRE}$ = H, $\overline{OE}1$ = L, $\overline{OE}2$ = L

*This setup time ensures the readback circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage (all inputs except D input) . . . . . 7 V
Voltage applied to D inputs and to disabled 3-state outputs . . . . . 5.5 V
Operating free-air temperature range: SN74ALS666, SN74ALS667 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN74ALS666 SN74ALS667			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q			−2.6	mA
		D			−0.4	
I_{OL}	Low-level output current	Q			24	mA
		D			8	
t_w	Pulse duration	Enable C high	10			ns
		$\overline{CLR}$ low	10			
		$\overline{PRE}$ low	10			
t_{su}	Setup time	Data before C↓	10			ns
		Data before $\overline{OERB}$↓	10			
t_h	Hold time	Data after C↓	5			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS666 SN74ALS667			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
	Q or $\overline{Q}$	V_{CC} = 4.5 V,	I_{OH} = −1 mA				
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	D	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
	Q or $\overline{Q}$	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
I_{OZH}	Q or $\overline{Q}$	V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	
I_I	D inputs	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	mA
	All others	V_{CC} = 5.5 V,	V = 7 V			0.1	
I_{IH}	D inputs‡	V_{CC} = 5.5 V,	V = 2.7 V			20	μA
	All others					20	
I_{IL}	D inputs‡	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
	All others					−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	'ALS666	V_{CC} = 5.5 V, $\overline{OERB}$ high	Q outputs high		25	50	mA
			Q outputs low		40	73	
			Q outputs disabled		30	55	
	'ALS667		$\overline{Q}$ outputs high		25	50	
			$\overline{Q}$ outputs low		45	79	
			$\overline{Q}$ outputs disabled		30	60	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS666 switching characteristics (see Figure 1)

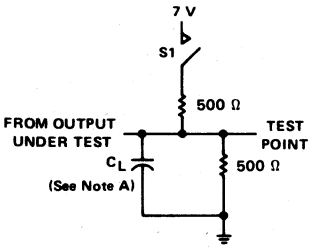
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = MIN to MAX		UNIT
			'ALS666			SN74ALS666		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	Q		7	10	3	14	ns
t_{PHL}				11	15	4	18	
t_{PLH}	C	Q		12	16	6	21	ns
t_{PHL}				16	21	8	27	
t_{PLH}	$\overline{CLR}$	Q		17	22	9	29	ns
t_{PHL}		D		17	24	11	32	
t_{PLH}	$\overline{PRE}$	Q		13	18	7	22	ns
t_{PHL}		D		17	22	9	28	
t_{en}	$\overline{OERB}$	D		11	17	4	21	ns
t_{dis}				6	11	1	14	
t_{en}	$\overline{OE1}$, $\overline{OE2}$	Q		11	17	4	21	ns
t_{dis}				6	11	1	14	

'ALS667 switching characteristics (see Figure 1)

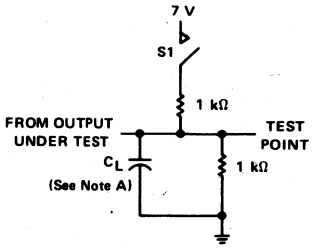
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = MIN to MAX		UNIT
			'ALS667			SN74ALS667		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$		13	17	6	20	ns
t_{PHL}				9	13	4	15	
t_{PLH}	C	$\overline{Q}$		18	23	9	28	ns
t_{PHL}				14	19	7	22	
t_{PLH}	$\overline{CLR}$	$\overline{Q}$		14	19	7	24	ns
t_{PHL}		D		17	23	8	26	
t_{PLH}	$\overline{PRE}$	$\overline{Q}$		17	23	8	25	ns
t_{PHL}		D		18	25	9	28	
t_{en}	$\overline{OERB}$	D		11	17	4	21	ns
t_{dis}				6	11	1	14	
t_{en}	$\overline{OE1}$, $\overline{OE2}$	$\overline{Q}$		11	17	4	21	ns
t_{dis}				6	11	1	14	

$t_{en} = t_{PZH}$ or t_{PZL}
$t_{dis} = t_{PHZ}$ or t_{PLZ}

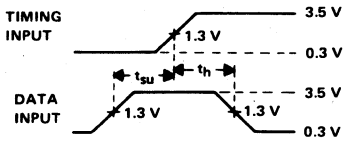
PARAMETER MEASUREMENT INFORMATION



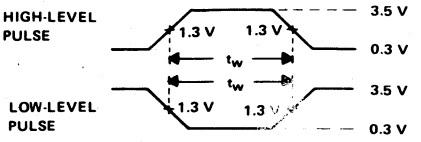
LOAD CIRCUIT FOR
Q OR $\overline{Q}$ OUTPUTS



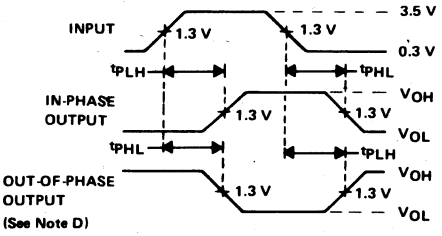
LOAD CIRCUIT FOR D OUTPUTS



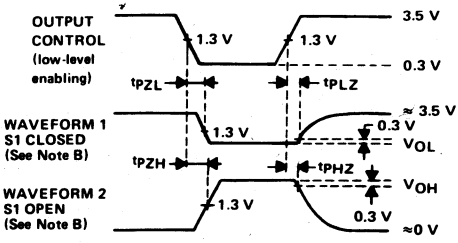
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE WIDTHS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

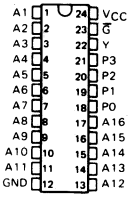
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay items of 3-state outputs, switch S1 is open.

FIGURE 1

D2661, JUNE 1982 – REVISED OCTOBER 1991

- **'ALS677A is a 16-bit Address Comparator with Enable**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS677A . . . DW OR NT PACKAGE
(TOP VIEW)



description

The 'ALS677A address comparator simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 16 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A16 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

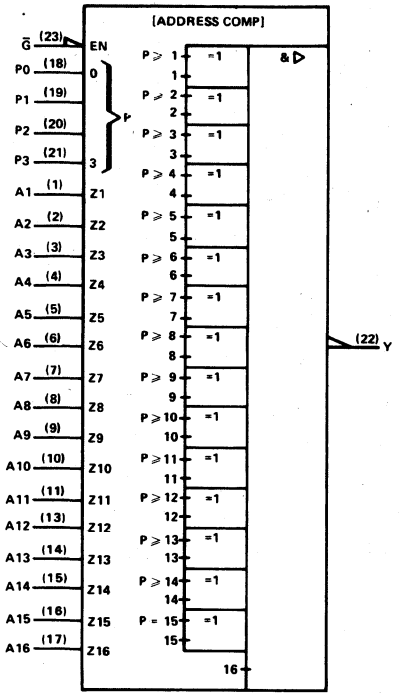
The 'ALS677A features an enable input ($\overline{G}$). When $\overline{G}$ is low, the device is enabled. When $\overline{G}$ is high, the device is disabled and the output is high regardless of the A and P inputs.

The SN74ALS677A is characterized for operation from 0°C to 70°C.

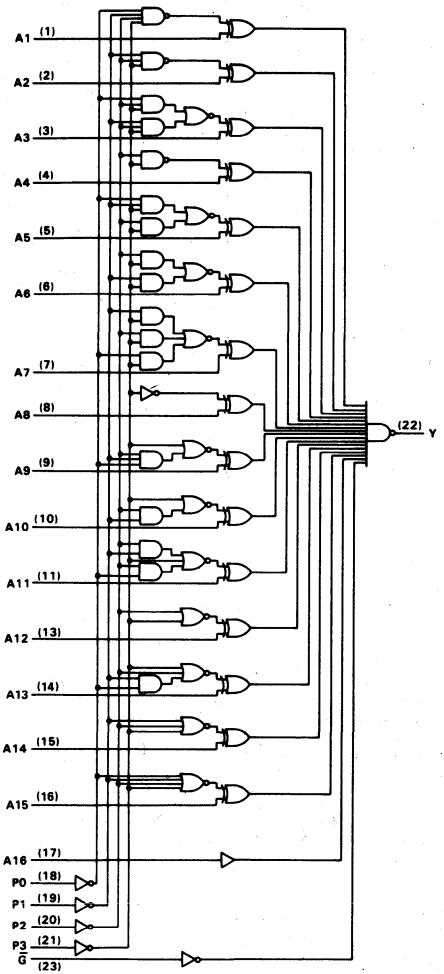
FUNCTION TABLE

'ALS677A		INPUTS COMMON TO 'ALS677A AND 'ALS678																				OUTPUT
$\overline{G}$	C	P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	Y
L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	H	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	All other combinations																				H
H		'ALS677A: Any combination																				H

'ALS677A logic symbol†



'ALS677A logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN74ALS677A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74ALS677			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−2.6	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS677A			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA				
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	'ALS677A	V_{CC} = 5.5 V			21	33	mA
					21	35	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS667A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX		UNIT
			'ALS677A			SN74ALS677A		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	Any P	Y		11	18	4	25	ns
t_{PHL}				22	32	8	38	
t_{PLH}	Any A	Y		10	17	5	35	ns
t_{PHL}				16	25	5	30	
t_{PLH}	$\overline{G}$	Y		6	10	3	13	ns
t_{PHL}				16	30	5	35	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION INFORMATION

The 'ALS677A can be wired to recognize any one of 2^{16} addresses. The number of "lows" in the address determines the input pattern for the P inputs. Then those system address lines that are low in the address to be recognized are connected to the lowest numbered A inputs of the address comparator and the system address lines that are high are connected to the highest numbered A inputs.

For example, assume the comparator is to enable a device when the 16-bit system address is:

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
H	H	L	L	H	H	L	L	H	H	L	L	H	H	H	H

Since the address contains 6 lows and 10 highs, the following connections are made:

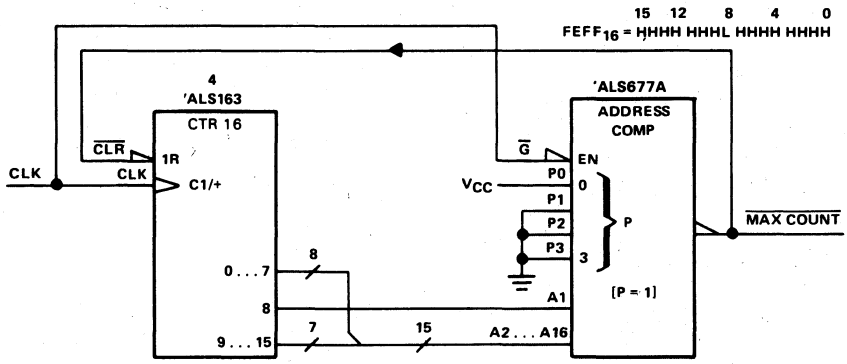
P3 to 0 V, P2 to V_{CC}, P1 to V_{CC}, and P0 to 0 V.

System address lines A13, A12, A9, A8, A5, and A4 to comparator inputs A1 through A6 in any convenient order.

The remaining ten system address lines to comparator inputs A7 through A16 in any convenient order.

The output provides an active-low enabling signal.

The following circuit is a modulo-N synchronous counter. The 'ALS163 is connected to provide a low-level clear signal when N = $FEFF_{16}$.

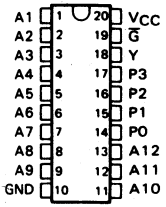


MODULO-N SYNCHRONOUS COUNTER

D2661, JUNE 1982 – REVISED MAY1986

- **Dependable Texas Instruments Quality and Reliability**

SN74ALS679 . . . DW OR N PACKAGE
(TOP VIEW)



description

The 'ALS679 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 12 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A12 must be high-to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

The 'ALS679 features an enable input ($\overline{G}$). When $\overline{G}$ is low, the device is enabled. When $\overline{G}$ is high, the device is disabled and the output is high regardless of the A and P inputs.

The SN74ALS679 is characterized for operation from 0°C to 70°C.

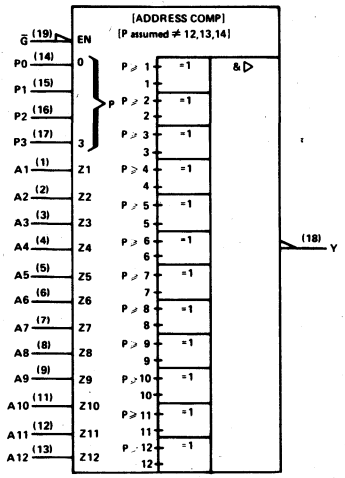
FUNCTION TABLE

'ALS679																	OUTPUT
$\overline{G}$	P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	Y
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L
L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	L
L	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	L
L	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	H	H	H	L	L†
L	H	H	L	H	L	L	L	L	L	L	L	L	L	H	H	L	L†
L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L†
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	All other combinations																H
H	Any combination																H

†The three shaded rows of the function table show combinations that would normally not be used in address comparator applications. The logic symbols above are not valid for these combinations in which P = 12, 13, and 14. If symbols valid for all combinations are required, starting with the fourth Exclusive-OR from the bottom, change P ≧ 9 to P = 9 . . . 11/13 . . . 15, P ≧ 10 to P = 10/11/14/15, and P ≧ 11 to P = 11/15.

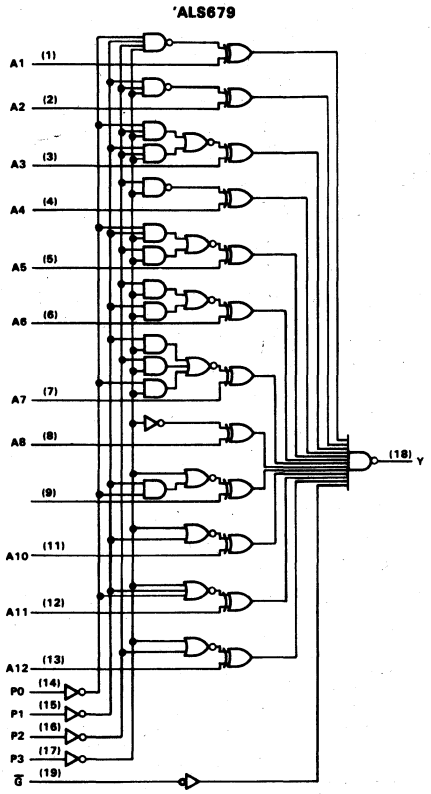
logic symbol ‡

'ALS679



‡These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positve logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN74ALS679. . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74ALS679			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−2.6	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS679			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA				
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			17	28	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS679 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX		UNIT
			SN74ALS679		
			MIN	MAX	
t_{PLH}	Any P	Y	4	25	ns
t_{PHL}			8	35	
t_{PLH}	Any A	Y	5	22	ns
t_{PHL}			5	30	
t_{PLH}	$\overline{G}$	Y	3	13	ns
t_{PHL}			5	25	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

The 'ALS679 can be wired to recognize any one of 2^{12} addresses. The number of "lows" in the address determines the input pattern for the P inputs. Then those system address lines that are low in the address to be recognized are connected to the lowest numbered A inputs of the address comparator and the system address lines that are high are connected to the highest numbered A inputs.

For example, assume the comparator is to enable a device when the 12-bit system address is:

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
H	H	L	L	H	H	L	L	H	H	H	H

Since the address contains 4 lows and 8 highs, the following connections are made:

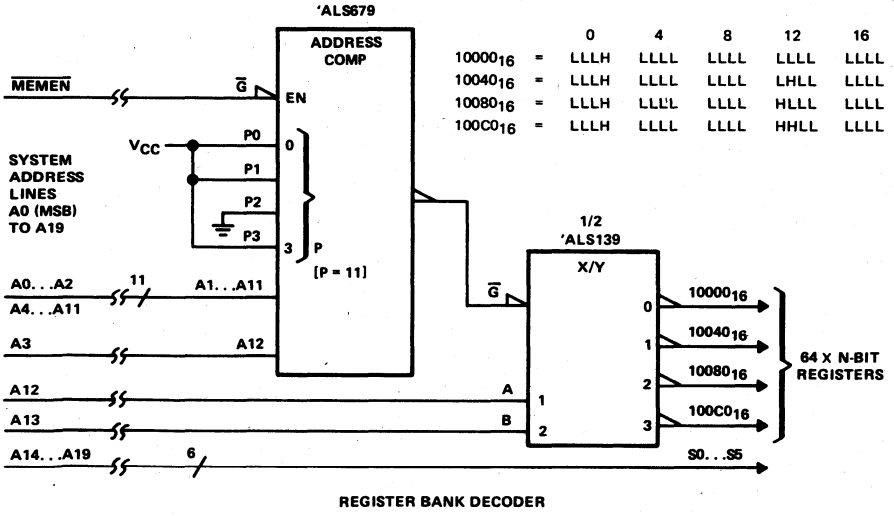
P3 to 0 V, P2 to V_{CC}, P1 to 0 V, and P0 to 0 V.

System address lines A9, A8, A5, and A4 to comparator inputs A1 through A4 in any convenient order.

The remaining eight system address lines to comparator inputs A5 through A12 in any convenient order.

The output provides an active-low enabling signal.

The following circuit is a register bank decoder that examines the 14 most significant bits (A0 through A13) of a 20-bit address to select banks corresponding to the hex addresses 10000, 10040, 10080, and 100C0.

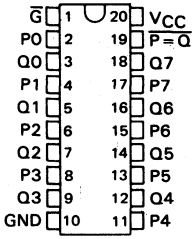


REGISTER BANK DECODER

D2661, JUNE 1982 – REVISED MAY 1986

- **Compares Two Eight-Bit Words**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS688 . . . J PACKAGE
SN74ALS688 . . . DW OR N PACKAGE
(TOP VIEW)



description

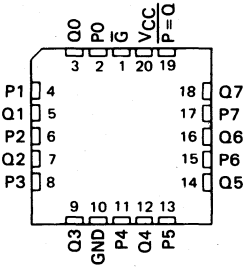
These identity comparators perform comparisons of two eight-bit binary or BCD words. The 'ALS688 provides $\overline{P = Q}$ totem-pole outputs.

The SN54ALS688 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS688 is characterized for operation from 0°C to 70°C.

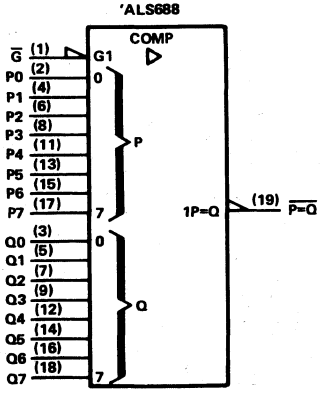
FUNCTION TABLE

INPUTS		OUTPUT
DATA P,Q	ENABLE $\overline{G}$	$\overline{P = Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

SN54ALS688 . . . FK PACKAGE
(TOP VIEW)

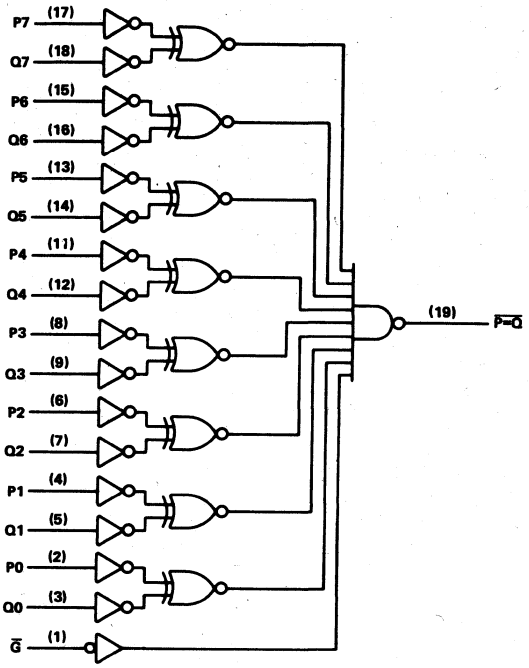


logic symbol ‡



‡These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage: 'ALS689 . . . . . 7 V
Operating free-air temperature range: SN54ALS688 . . . . . −55°C to 125°C
SN74ALS688 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS688			SN74ALS688			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS688			SN74ALS688			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} 2			V_{CC} 2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	See Note 1		12	19		12	19	mA

†All typical values are at V_{CC} 5 V, T_A 25°C

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

NOTE 1: I_{CC} is measured with G grounded, P and Q at 4.5 V.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS688		SN74ALS688		
			MIN	MAX	MIN	MAX	
t_{PLH}	P	$\overline{P=Q}$	3	16	3	12	ns
t_{PHL}			5	25	5	20	
t_{PLH}	Q	$\overline{P=Q}$	3	16	3	12	ns
t_{PHL}			5	25	5	20	
t_{PLH}	$\overline{G}$	$\overline{P=Q}$	3	15	3	12	ns
t_{PHL}			5	25	5	22	

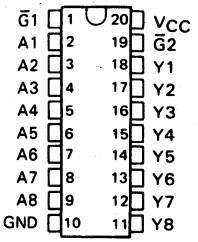
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

OCTAL BUFFERS AND LINE DRIVERS WITH INPUT PULL-UP RESISTORS

AUGUST 1984 – REVISED MAY 1986

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Input Pull-Up Resistors Added for Data Bus Termination**
- **Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS746 . . . DW OR N PACKAGE
(TOP VIEW)



description

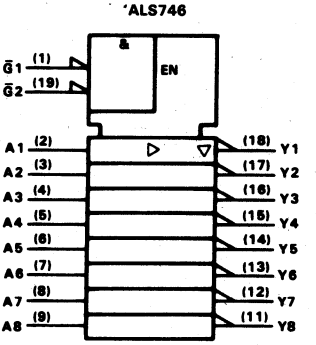
These octal buffers and line drivers are designed to have the performance of the popular SN54ALS240A/SN74ALS240A series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout. In addition, 20 kilohm resistors have been added between all inputs and V_{CC}. This eliminates adding external resistors in applications where the data bus must be at a high level whenever all other connecting devices are at a high impedance state.

The three-state control gate is a 2-input NOR such that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

The 'ALS746 provides inverted data at the outputs.

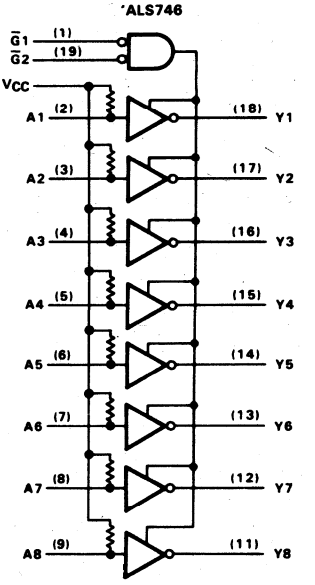
The SN74ALS746 is characterized for operation fom 0°C to 70°C.

logic symbol†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



All input pull-up resistors are 20 kΩ

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN74ALS746 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74ALS746			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS746			UNIT
				MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA				
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA†		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I	A	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	mA
	$\overline{G1}$, $\overline{G2}$	V_{CC} = 5.5 V,	V_I = 7 V			0.1	
I_{IH}	A	V_{CC} = 5.5 V,	V_I = 2.7 V			−0.2	mA
	$\overline{G1}$, $\overline{G2}$					20	μA
I_{IL}	A	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.6	mA
	$\overline{G1}$, $\overline{G2}$					−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		7	12	mA
			Outputs low		13	22	
			Outputs disabled		11	19	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
† I_{OL} = 48 mA for −1 versions.

'ALS746A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			'ALS746	SN74ALS746		
			TYP	MIN	MAX	
t_{PLH}	A	Y	7.5	3	12	ns
t_{PHL}			5.6	2	9	
t_{PZH}	$\overline{G}$	Y	9	5	15	ns
t_{PZL}			12.5	8	20	
t_{PHZ}	$\overline{G}$	Y	4	1	10	ns
t_{PLZ}			7	2	12	

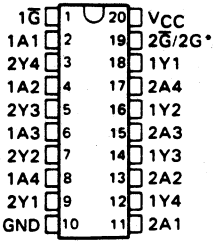
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

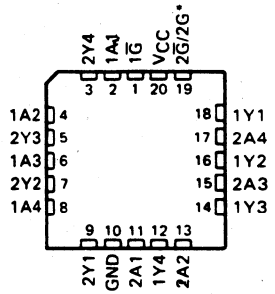
D2661, DECEMBER 1983 – REVISED FEBRUARY 1988

- **Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Register**
- **Eliminates the Need for 3-State Overlap Protection**
- **P-N-P Inputs Reduce DC Loading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Open-Collector Versions of 'AS240 and 'AS241**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS', SN54AS' ... J PACKAGE
SN74ALS', SN74AS' ... DW OR N PACKAGE
(TOP VIEW)



SN54AS756 ... FK PACKAGE
(TOP VIEW)



* $2\overline{G}$ for 'AS756 or 2G for 'AS757.

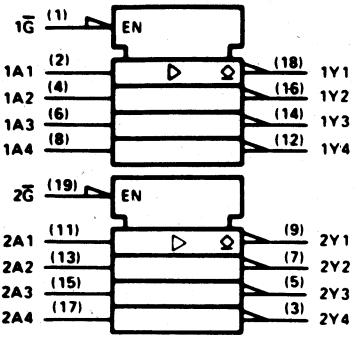
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters by eliminating the need for three-state overlap protection. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out and improved fan-in.

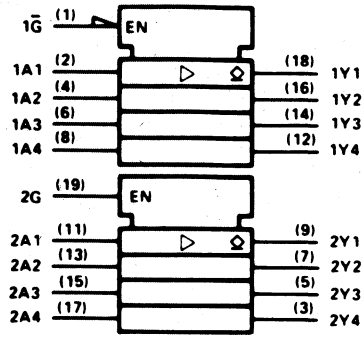
The SN54' family is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74' family is characterized for operation from 0 °C to 70 °C.

logic symbols†

'AS756



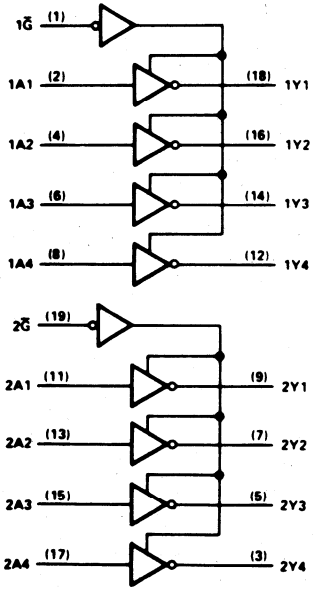
'AS757



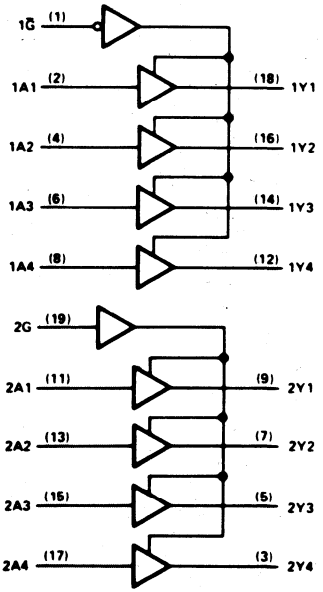
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

'AS756



'AS757



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54AS756 . . . . . −55°C to 125°C
SN74AS756, SN74AS757 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS756			SN74AS756 SN74AS757			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS756			SN74AS756 SN74AS757			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.55					V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA						0.55	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	A inputs of 'AS757 only	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All other inputs					−0.5			−0.5	
I_{CC}	'AS756	V_{CC} = 5.5 V	Output high		9	15		9	15	mA
			Output low		51	80		51	80	
	'AS757		Output high					21	33	
			Output low					61	95	

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.

'AS756 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS756		SN74AS756		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	20	3	19	ns
t_{PHL}			1	7	1	6	
t_{PLH}	$\overline{G}$	Y	3	22	3	19.5	ns
t_{PHL}			1	8.5	1	7.5	

'AS757 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX		UNIT
			SN74AS757		
			MIN	MAX	
t_{PLH}	A	Y	3	18.5	ns
t_{PHL}			1	6	
t_{PLH}	$1\overline{G}$	1Y	3	20	ns
t_{PHL}			1	7	
t_{PLH}	2G	2Y	3	21	ns
t_{PHL}			1	7.5	

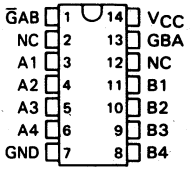
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

QUADRUPLE BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

D2910, DECEMBER 1983 – REVISED MAY 1986

- **2-Way Asynchronous Communication Between Data Buses**
- **P-N-P Inputs Reduce Loading**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74'... D OR N PACKAGE
(TOP VIEW)



description

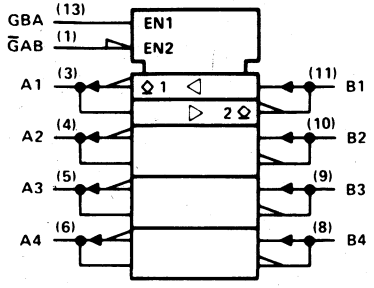
These four-data-line transceivers are designed for asynchronous two-way communications between data buses.

FUNCTION TABLE

INPUTS		'ALS758
$\overline{G}AB$	GBA	
L	L	$\overline{A}$ to B
H	H	$\overline{B}$ to A
H	L	Isolation
L	H	Latch A and B ($A = \overline{B}$)

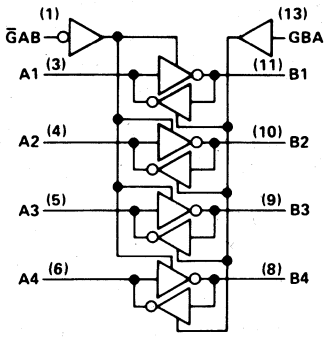
logic symbol†

'ALS758



logic diagram (positive logic)

'ALS758



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range: SN74ALS758 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74ALS758			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage			5.5	V
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS758			UNIT
				MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	A or B ports§					20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
	A or B ports§					−0.1	
I_{CC}		V_{CC} = 5.5 V	Outputs high		6	10	mA
			Outputs low		10	16	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 680 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX		UNIT
			'ALS758	SN74ALS758		
			TYP	MIN	MAX	
t_{PLH}	A or B	B or A	20	10	28	ns
t_{PHL}			5	2	12	
t_{PLH}	GBA	A	18	10	28	ns
t_{PHL}			13	6	21	
t_{PLH}	$\overline{G}AB$	B	18	10	28	ns
t_{PHL}			13	6	21	

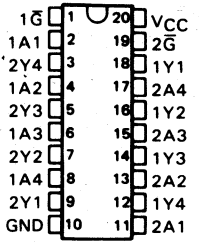
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

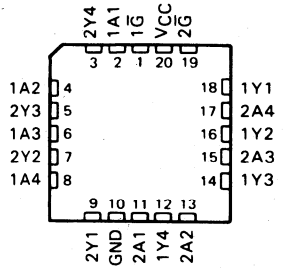
DECEMBER 1983 – REVISED FEBRUARY 1988

- **Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Eliminates the Need for 3-State Overlap Protection**
- **P-N-P Inputs Reduce DC Loading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Open-Collector Versions of 'ALS244 and 'AS244**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS760 . . . J PACKAGE
SN74ALS760, SN74AS760 . . . DW OR N PACKAGE
(TOP VIEW)



SN54AS760 . . . FK PACKAGE
(TOP VIEW)

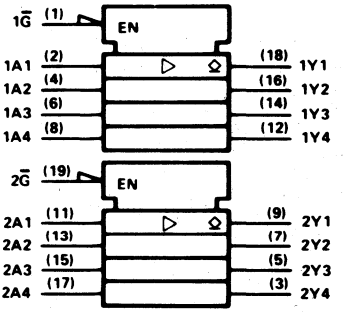


description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters by eliminating the need for 3-state overlap protection. Taken together with the 'AS756 and 'AS757, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{G}$ (active-low input control) inputs, and complimentary G and $\overline{G}$ inputs.

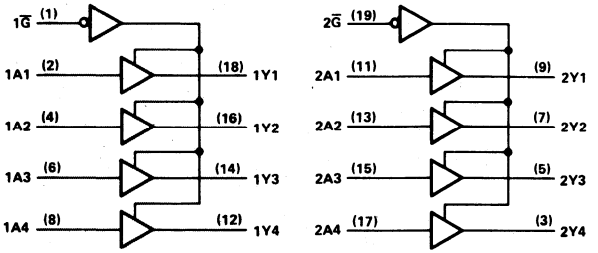
The SN54AS760 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS760 and SN74AS760 are characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage. . . . . 7 V
Operating free-air temperature range: SN74ALS760. . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74ALS760			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage			5.5	V
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS760			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		9	15	mA
		Outputs low		15	19	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX		UNIT
			SN74ALS760		
			MIN	MAX	
t_{PLH}	A	Y	5	15	ns
t_{PHL}			5	12	
t_{PLH}	$\overline{G}$	Y	5	16	ns
t_{PHL}			5	13	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54AS760 . . . . . −55°C to 125°C
SN74AS760 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS760			SN74AS760			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS760			SN74AS760			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA						0.55	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	$\overline{G}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A					−1			−1	
I_{CC}		V_{CC} = 5.5 V	Outputs high		20	32		20	32	mA
			Outputs low		60	94		60	94	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

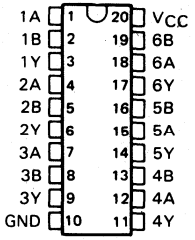
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS760		SN74AS760		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	19.5	3	18.5	ns
t_{PHL}			1	7	1	6	
t_{PLH}	$\overline{G}$	Y	3	19.5	3	18.5	ns
t_{PHL}			1	8	1	7	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

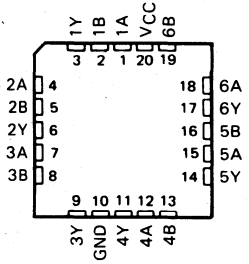
D2661, DECEMBER 1982 – REVISED MAY 1986

- **High Capacitive Drive Capability**
- **'ALS804A has Typical Delay Time of 4 ns (C_L = 50 pF) and Typical Power Dissipation of 3.4 mW per Gate**
- **'AS804B has Typical Delay Time of 2.6 ns (C_L = 50 pF) and Typical Power Dissipation of Less than 9 mW per Gate**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS804A, SN54AS804B . . . J PACKAGE
SN74ALS804A, SN74AS804B . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS804A, SN54AS804B . . . FK PACKAGE
(TOP VIEW)



description

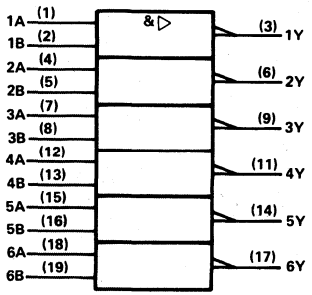
These devices contain six independent 2-input NAND drivers. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS804A and SN54AS804B are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS804A and SN74AS804B are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each driver)

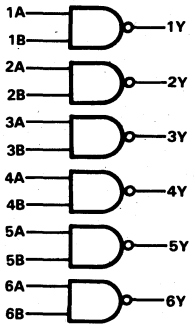
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS804A . . . . . −55°C to 125°C
SN74ALS804A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 50°C

recommended operating conditions

		SN54ALS804A			SN74ALS804A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS804A			SN74ALS804A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.9	2.5		0.9	2.5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		7	12		7	12	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS804A	SN54ALS804A		SN74ALS804A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	4	1	9	1	7	ns
t_{PHL}			4	1	9	1	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS804B . . . . . −55°C to 125°C
SN74AS804B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 50°C

recommended operating conditions

		SN54AS804B			SN74AS804B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS804B			SN74AS804B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25	−50		−200	−50		−200	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		3.5	5		3.5	5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		16	27		16	27	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS804B		SN74AS804B		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	5	1	4	ns
t_{PHL}			1	5	1	4	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, DECEMBER 1982 – REVISED MAY 1986

- **High Capacitive Drive Capability**
- **'ALS805A has Typical Delay Time of 4.2 ns (C_L = 50 pF) and Typical Power Dissipation of 4.2 mW per Gate**
- **'AS805B has Typical Delay Time of 2.6 ns (C_L = 50 pF) and Typical Power Dissipation of 12 mW per Gate**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

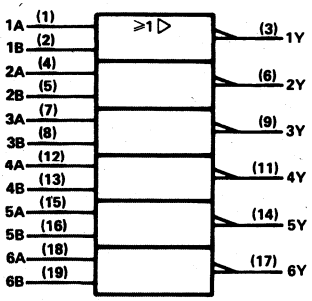
These devices contain six independent 2-input NOR drivers. They perform the Boolean functions $Y = \overline{A+B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54ALS805A and SN54AS805B are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS805A and SN74AS805B are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each driver)

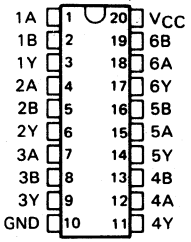
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†

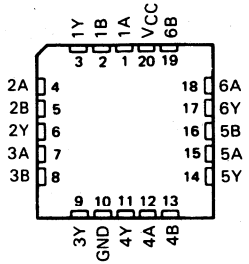


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

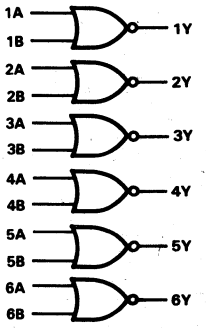
SN54ALS805A, SN54AS805B . . . J PACKAGE
SN74ALS805A, SN74AS805B . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS805A, SN54AS805B . . . FK PACKAGE
(TOP VIEW)



logic diagram (positive logic)



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS805A . . . . . −55°C to 125°C
SN74ALS805A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS805A			SN74ALS805A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS805A			SN74ALS805A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		2	4		2	4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		8	14		8	14	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS805A	SN54ALS805A		SN74ALS805A		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	4	2	9	2	7	ns
t_{PHL}			4	2	9	2	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS805B . . . . . −55°C to 125°C
SN74AS805B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS805B			SN74AS805B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS805B			SN74AS805B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−200	−50		−200	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		6.5	10		6.5	10	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		20	32		20	32	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

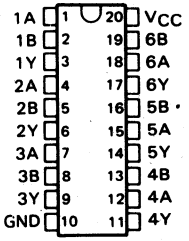
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS805B		SN74AS805B		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	4.8	1	4.3	ns
t_{PHL}			1	4.8	1	4.3	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

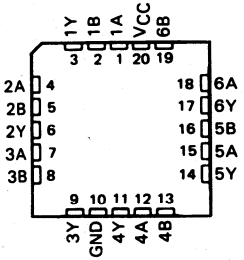
D2661, DECEMBER 1982 – REVISED MAY 1986

- **High Capacitive Drive Capability**
- **'AS808B has Typical Delay Time of 3.2 ns (C_L = 50 pF) and Typical Power Dissipation of Less than 13 mW per Gate**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS808B ... J PACKAGE
SN74AS808B ... DW OR N PACKAGE
(TOP VIEW)



SN54AS808B ... FK PACKAGE
(TOP VIEW)



description

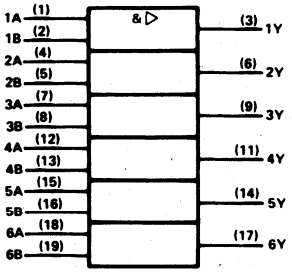
These devices contain six independent 2-input AND drivers. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The SN54AS808B is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AS808B is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each driver)

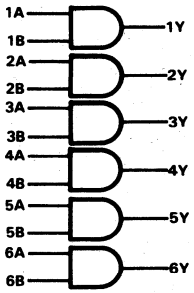
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS808B . . . . . −55°C to 125°C
SN74AS808B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS808B			SN74AS808B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS808B			SN74AS808B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−200	−50		−200	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		8	13		8	13	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		20	33		20	33	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

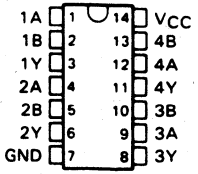
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS808B		SN74AS808B		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	6.5	1	6	ns
t_{PHL}			1	6.5	1	6	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, MARCH 1984 – REVISED OCTOBER 1988

- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS810 . . . D OR N PACKAGE
(TOP VIEW)



description

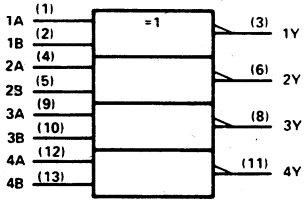
These devices contain four independent Exclusive-NOR gates. They perform the Boolean functions $Y = \overline{A + B} = (\overline{A} + B) \cdot (A + B)$ in positive logic.

A common application is a true/complement element. If one of the inputs is high, the other input will be reproduced in true form at the output. If one of the inputs is low, the signal on the other input will be reproduced inverted at the output.

FUNCTION TABLE
(EACH GATE)

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D and N packages.

exclusive-NOR logic

An Exclusive-NOR gate has many applications, some of which can be represented better by alternative logic symbols.

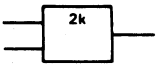
EXCLUSIVE-NOR

These are five equivalent Exclusive-NOR symbols valid for an 'ALS810 gate in positive logic; negation may be shown at any one port, or at all three of them.

LOGIC IDENTITY ELEMENT

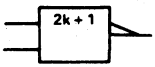
The output is active (high) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY



The output is active (high) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (low) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN74ALS810 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74ALS810			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS810			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_O*	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	A at 4.5 V, B at 0 V		5	7.5	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
* The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

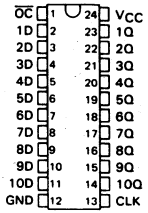
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX		UNIT
			SN74ALS810		
			MIN	MAX	
t_{PLH}	A or B (other input low)	Y	5	20	ns
t_{PHL}			3	14	
t_{PLH}	A or B (other input high)	Y	5	18	ns
t_{PHL}			3	14	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

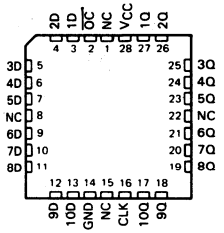
D2825, DECEMBER 1983 – REVISED JANUARY 1986

- **Functionally Equivalent to AMD's AM29821**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity**
- **Outputs Have Undershoot Protection Circuitry**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Buffered Control Inputs to Reduce DC Loading Effects**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS831 . . . JT PACKAGE
SN74AS821A . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS821 . . . FK PACKAGE
(TOP VIEW)



description

These 10-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock the Q outputs on the 'AS821A will be true to the data input.

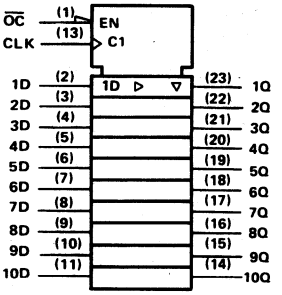
A buffered output-control input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AS' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS' family is characterized for operation from 0°C to 70°C.

'AS821A FUNCTION TABLE (EACH FLIP-FLOP)

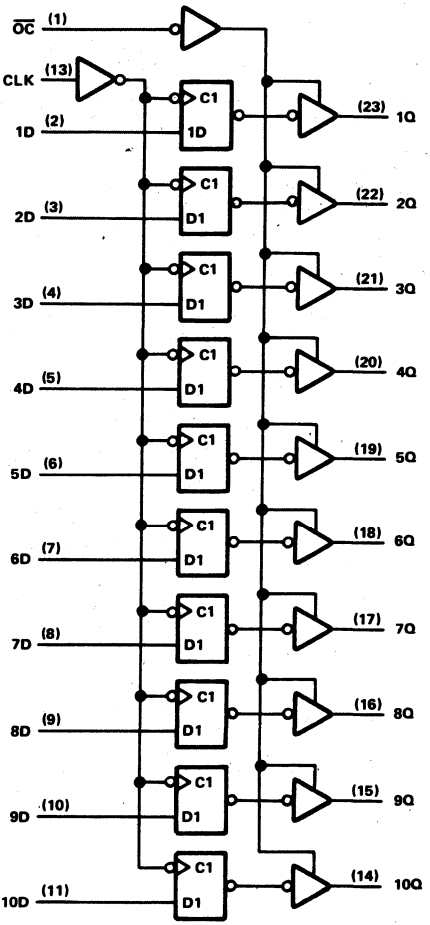
INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

'AS821A logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'AS821A logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS821 . . . . . −55°C to 125°C
SN74AS821A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operation conditions

		SN54AS821			SN74AS821A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			32			48	mA
t_w	Pulse duration, CLK high or low	9			8			ns
t_{su}	Setup time, data before CLK↑	7			6			ns
t_h	Hold time, data after CLK↑	0			0			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS821			SN74AS821A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OHZ}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	µA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		55	88		55	88	mA
		Outputs low		68	109		68	109	
		Outputs disabled		70	113		70	113	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS821		SN74AS821A		
			MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	3.5	9	3.5	7.5	ns
t_{PHL}			3.5	11.5	3.5	13	
t_{PZH}	$\overline{OC}$	Any Q	4	12	3	11	ns
t_{PZL}			4	13	4	12	
t_{PHZ}	$\overline{OC}$	Any Q	2	10	1	8	ns
t_{PLZ}			2	10	1	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

D2825, JUNE 1984 – REVISED JANUARY 1986

- **Functionally Equivalent to AMD's AM29823 and AM29824**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity**
- **Outputs Have Undershoot Protection Circuitry**
- **Power-Up High-Impedance State**
- **Buffered Control Inputs to Reduce DC Loading Effects**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

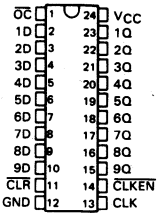
description

These 9-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

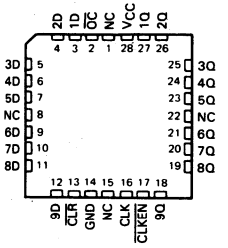
With the clock enable ($\overline{CLKEN}$) low, the nine D-type edge-triggered flip-flop enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high will disable the clock buffer, thus latching the outputs. The 'AS823A has noninverting D inputs and the 'AS824A has inverting D inputs. Taking the $\overline{CLR}$ input low causes the nine Q outputs to go low independently of the clock.

A buffered output-control input ($\overline{OC}$)can be used to place the nine outputs in either normal logic state (high or low level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

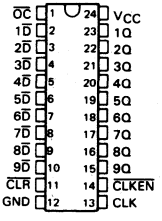
SN54AS823 . . . JT PACKAGE
SN74AS823A . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS823 . . . FK PACKAGE
(TOP VIEW)



SN74AS824A . . . DW OR NT PACKAGE
(TOP VIEW)

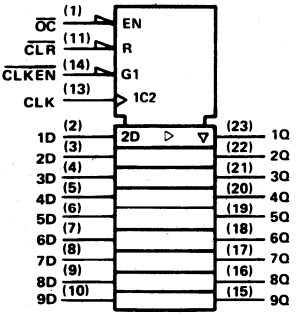


The SN54AS' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS' family is characterized for operation from 0°C to 70°C.

'AS823A FUNCTION TABLE

INPUTS					OUTPUT
$\overline{OC}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

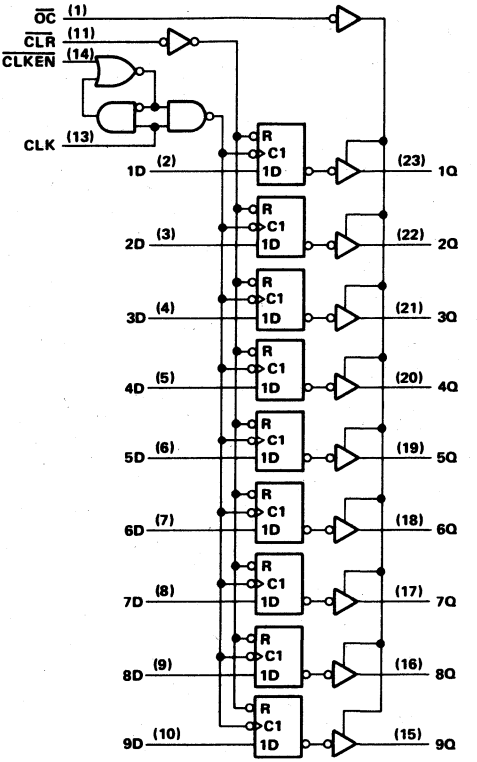
AS823A logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

Pin numbers shown are for DW, JT, and NT packages.

'AS823A logic diagram (positve logic)

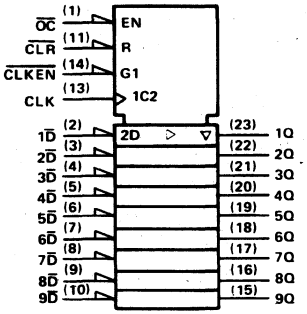


TEXAS INSTRUMENTS

'AS824A FUNCTION TABLE

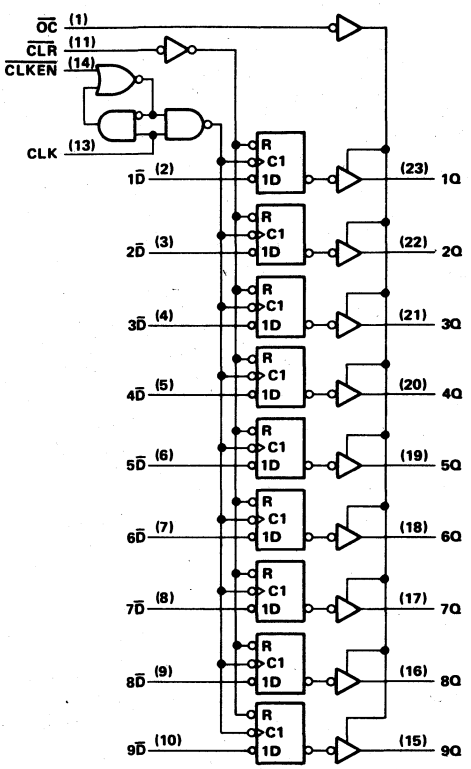
INPUTS					OUTPUT
$\overline{OC}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	$\overline{D}$	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

'AS824A logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW and NT packages.

'AS824A logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS823 . . . . . −55°C to 125°C
SN74AS823A, SN74AS824A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS823			SN74AS823A SN74AS824A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−24			−24	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration	$\overline{CLR}$ low	5			6.5			ns
		CLK high or low	9			8			
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	8			8			ns
		Data	7			6			
		$\overline{CLKEN}$ high or low	7			7.5			
t_h	Hold time, $\overline{CLKEN}$ or data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS823			SN74AS823A SN74AS824A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.3	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	µA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS823A	V_{CC} = 5.5 V	Outputs high		49	80		49	80	mA
			Outputs low		61	100		61	100	
			Outputs disabled		64	103		64	103	
	'AS824A	V_{CC} = 5.5 V	Outputs high					49	80	mA
			Outputs low					61	100	
			Outputs disabled					64	103	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS823		SN74AS823A SN74AS824A		
			MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	3.5	9	3.5	7.5	ns
t_{PHL}			3.5	12	3.5	13	
t_{PHL}	$\overline{CLR}$	Any Q	3.5	14	3.5	15.5	
t_{PZH}	$\overline{OC}$	Any Q	4	12	4	11	ns
t_{PZL}			4	13	4	12	
t_{PHZ}	$\overline{OC}$	Any Q	2	10	1	8	ns
t_{PLZ}			2	10	1.5	8	

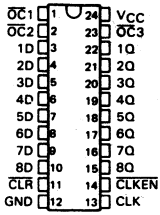
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

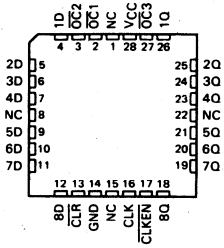
D2825, JUNE 1984 – REVISED JANUARY 1986

- **Functionally Equivalent to AMD's AM29825**
- **Improved I_{OH} Specifications**
- **Multiple Output Enables Allow Multiuser Control of the Interface**
- **Outputs Have Undershoot Protection Circuitry**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Buffered Control Inputs to Reduce DC Loading Effect**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS825 . . . JT PACKAGE
SN74AS825A . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS825 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing multiuser registers, I/O ports, bidirectional bus drivers, and working registers.

With the clock enable ($\overline{CLKEN}$) low, the eight D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high will disable the clock buffer, thus latching the outputs. The 'AS825A has noninverting D inputs. Taking the $\overline{CLR}$ input low causes the eight Q outputs to go low independently of the clock.

Multiuser buffered output-control inputs ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) can be used to place the eight outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

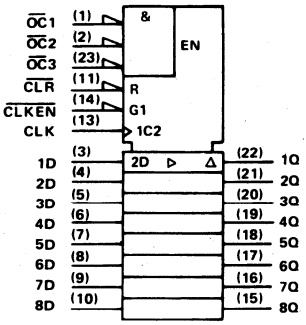
The SN54AS' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS' family is characterized for operation from 0°C to 70°C.

'AS825 FUNCTION TABLE

INPUTS					OUTPUT
$\overline{OC}$*	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

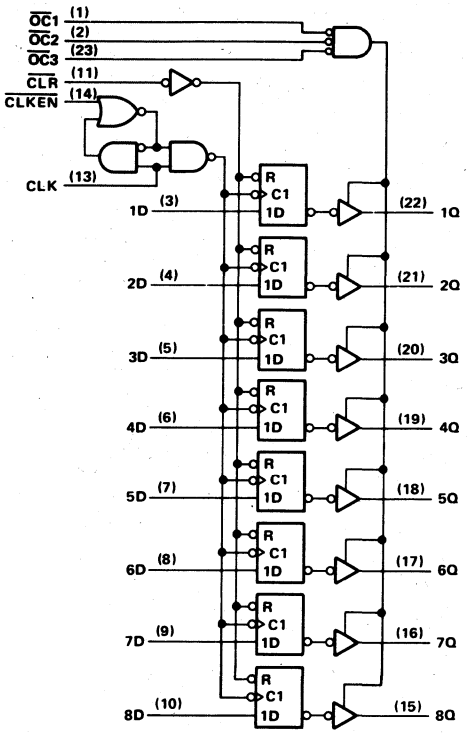
$\overline{OC}$* = H if any of $\overline{OC}$1, $\overline{OC}$2, or $\overline{OC}$3 are high.
$\overline{OC}$* = L if all of $\overline{OC}$1, $\overline{OC}$2, and $\overline{OC}$3 are low.

'AS825 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'AS825 logic diagram (positive logic)



Pin numbers are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS825 . . . . . −55°C to 125°C
SN74AS825A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operation conditions

			SN54AS825			SN74AS825A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−24			−24	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration	$\overline{CLR}$ low	5			6			ns
		CLK high or low	9			8			
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	8			8			ns
		Data	7			6			
		$\overline{CLKEN}$ high or low	7			9			
t_h	Hold time, $\overline{CLKEN}$ or data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS825			SN74AS825A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.3	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	µA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		45	73		45	73	mA
		Outputs low		56	90		56	90	
		Outputs disabled		59	95		59	95	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

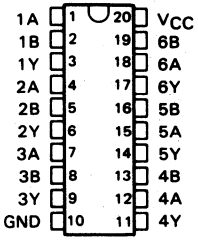
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS825		SN74AS825A		
			MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	3.5	9	3.5	7.5	ns
t_{PHL}			3.5	11.5	3.5	13	
t_{PHL}	$\overline{CLR}$	Any Q	3.5	14	3.5	15.5	
t_{PZH}	$\overline{OC}$	Any Q	4	12	4	11	ns
t_{PZL}			4	13	4	12	
t_{PHZ}	$\overline{OC}$	Any Q	2	10	1.5	8	ns
t_{PLZ}			2	10	1.5	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

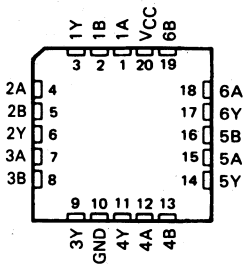
D2661, DECEMBER 1982 – REVISED SEPTEMBER 1990

- **High Capacitive Drive Capability**
- **'ALS832A Has Typical Delay Time of 4.8 ns (C_L = 50 pF) and Typical Power Dissipation of 4.5 mW per Gate**
- **'AS832B Has Typical Delay Time of 3.2 ns (C_L = 50 pF) and Typical Power Dissipation of less than 13 mW per Gate**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**

SN54ALS832A, SN54AS832B . . . J PACKAGE
SN74ALS832A, SN74AS832B . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS832A, SN54AS832B . . . FK PACKAGE
(TOP VIEW)



description

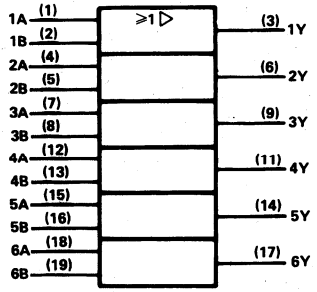
These devices contain six independent 2-input AND drivers. They perform the Boolean functions $Y = A+B$ or $Y = \overline{A \cdot B}$ in positive logic.

The SN54ALS832A and SN54AS832B are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS832A and SN74AS832B are characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each driver)

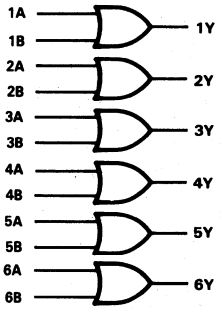
INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS832A . . . . . −55°C to 125°C
SN74ALS832A . . . . . °C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS832A			SN74ALS832A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS832A			SN74ALS832A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		6	9		6	9	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		9.5	16		9.5	16	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS832A		SN74ALS832A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	13	2	9	ns
t_{PHL}			1	11	1	8	

TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS832B . . . . . −55°C to 125°C
SN74AS832B . . . . . °C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS832B			SN74AS832B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS832B			SN74AS832B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} −2			V_{CC} −2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−200	−50		−200	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		11	17		11	17	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		22	36		22	36	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

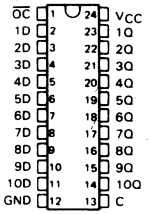
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS832B		SN74AS832B		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	7.5	1	6.3	ns
t_{PHL}			1	7	1	6.3	

D2910, DECEMBER 1983 – REVISED OCTOBER 1985

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Provide Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity**
- **Buffered Control Inputs to Reduce DC Loading**
- **Power-Up High-Impedance State**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS841, SN74AS841A . . . DW OR NT PACKAGE
(TOP VIEW)



description

These 10-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type. The 'ALS841 and 'AS841A have noninverting data (D) inputs.

A buffered output control ($\overline{OC}$) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

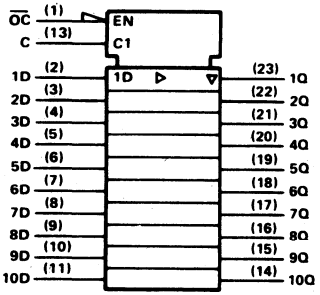
The SN74ALS841 and SN74AS841A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

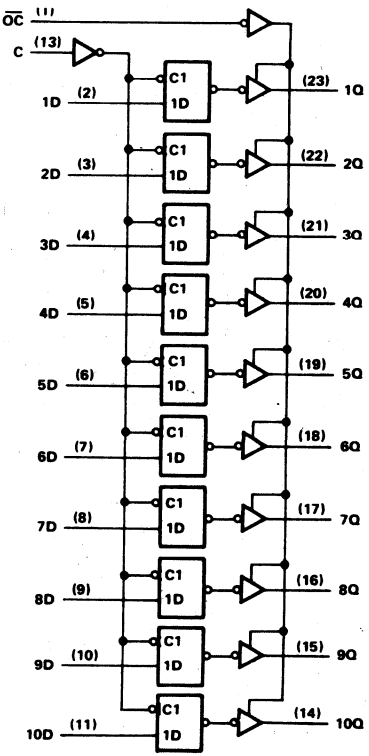
'ALS841, 'ALS841A

INPUTS			OUTPUT
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

'ALS841, 'AS841A logic symbol†



'ALS841, 'AS841A logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN74ALS841, SN74AS841A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74ALS841			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			-2.6	mA
I_{OL}	Low-level output current			24	mA
t_w	Pulse duration, enable C high	20			ns
t_{su}	Setup time, data before enable C↓	10			ns
t_h	Hold time, data after enable C↓	5			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS841			UNIT
			MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = -18 mA			-1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = -0.4 mA	V_{CC}-2			V
	V_{CC} = 4.5 V,	I_{OH} = -1 mA				
	V_{CC} = 4.5 V,	I_{OH} = -2.6 mA	2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
	V_{CC} = 4.5 V, (I_{OL} = 48 mA for -1 versions)	I_{OL} = 24 mA		0.35	0.5	
I_{OHZ}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4			-20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			-0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	-30		-112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		19	30	mA
		Outputs low		38	62	
		Outputs disabled		23	40	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS841 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX			UNIT
			'ALS841			SN74ALS841			
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	D	Q		8.5	11	2		13	ns
t_{PHL}				8.5	11	2		13	
t_{PLH}	C	Q		14	18	7		21	ns
t_{PHL}				17	23	8		26	
t_{PZH}	$\overline{OC}$	Q		7.5	10	2		12	ns
t_{PZL}				7.5	10	2		12	
t_{PHZ}	$\overline{OC}$	Q		6	8	2		10	ns
t_{PLZ}				7	9	2		12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN74ALS841A			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			-24	mA
I_{OL}	Low-level output current			48	mA
t_w	Pulse duration, enable C high	4			ns
t_{su}	Setup time, data before enable C↓	2.5			ns
t_h	Hold time, data after enable C↓	2.5			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74AS841A			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = -18 mA			-1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = -2 mA	V_{CC}-2			V
	V_{CC} = 4.5 V,	I_{OH} = -15 mA	2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = -24 mA	2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4			-50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			-0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	-30		-112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		36	60	mA
		Outputs low		58	94	
		Outputs disabled		56	93	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS841 switching characteristics

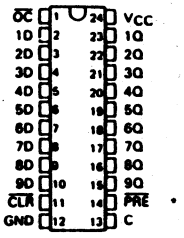
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			SN74AS841A		
			MIN	MAX	
t_{PLH}	D	Q	1	6.5	ns
t_{PHL}			1	10,5	
t_{PLH}	C	Q	2	12	ns
t_{PHL}			2	12	
t_{PZH}	$\overline{OC}$	Q	2	14	ns
t_{PZL}			2	16	
t_{PHZ}	$\overline{OC}$	Q	1	8	ns
t_{PLZ}			1	8	

9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D2910, DECEMBER 1983 – REVISED MAY 1986

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Provide Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity**
- **Buffered Control Inputs to Reduce DC Loading**
- **Power-Up High Impedance**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS843 . . . DW OR NT PACKAGE
(TOP VIEW)



description

These 9-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The nine latches are transparent D-type. The 'ALS843 have noninverting data (D) inputs.

A buffered output control ($\overline{OC}$) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

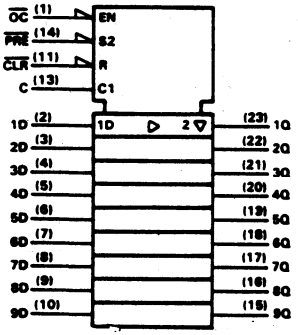
The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN74ALS843 is characterized for operation from 0°C to 70°C.

'ALS843 FUNCTION TABLE

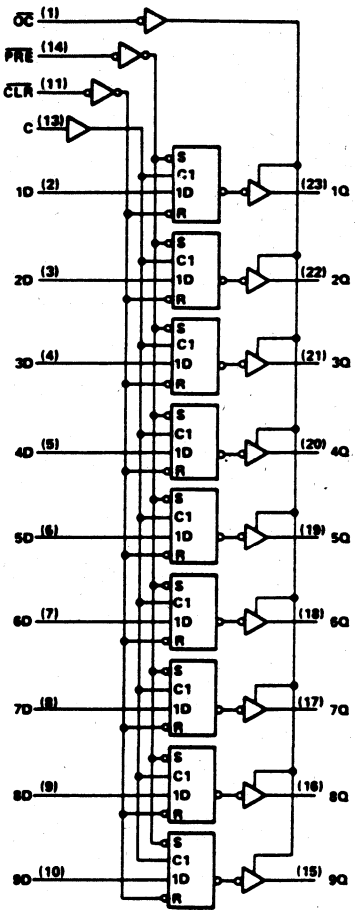
INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC}$	C	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q_0
X	X	H	X	X	Z

'ALS843 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW and NT packages.

'ALS843 logic diagram (positive logic)



TEXAS INSTRUMENTS

recommended operating conditions

			SN74ALS843			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				-2.6	mA
I_{OL}	Low-level output current				24	mA
t_w	Pulse duration	$\overline{CLR}$ or $\overline{PRE}$ low	34			ns
		C high	20			
t_{su}	Setup time, data before enable C↓		10			ns
t_h	Hold time, data after enable C↓		5			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS843			UNIT
			MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = -18 mA			-1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = -0.4 mA	V_{CC}-2			V
	V_{CC} = 4.5 V,	I_{OH} = -1 mA				
	V_{CC} = 4.5 V,	I_{OH} = -2.6 mA	2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
	V_{CC} = 4.75 V,	I_{OL} = 48 mA (-1 versions)		0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			-20	µA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			-0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	-30		-112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		21	36	mA
		Outputs low		41	67	
		Outputs disabled		25	42	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN74ALS843 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

'ALS843 switching characteristics (see Note 1)

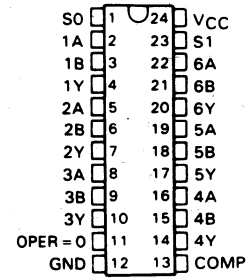
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			'ALS843			SN74ALS843		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	Q		7	11	2	13	ns
t_{PHL}				11	15	4	18	
t_{PLH}	C	Q		12	18	5	21	ns
t_{PHL}				16	23	8	26	
t_{PLH}	$\overline{PRE}$	Q		13	19	5	22	ns
t_{PHL}				19	26	6	30	
t_{PLH}	$\overline{CLR}$	Q		19	26	6	30	ns
t_{PHL}				14	21	6	23	
t_{PZH}	$\overline{OC}$	Q		7	10	2	12	ns
t_{PZL}				9	12	4	14	
t_{PHZ}	$\overline{OC}$	Q		6	9	2	10	ns
t_{PLZ}				7	10	2	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, DECEMBER 1982 – REVISED JULY 1989

- **Selects True or Complementary Data**
- **Performs AND/NAND (masking) of A or B Operand**
- **Cascadable to Expand Number of Operands**
- **Detects Zeros on A or B Operands**
- **3-State Outputs Interface Directly with System Bus**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS857 . . . JT PACKAGE
SN74ALS857 . . . DW OR NT PACKAGE
(TOP VIEW)



description

The 'ALS857 are hextuple 2-line to 1-line multiplexers with three-state outputs. The devices can provide either true (COMP low) or inverted (COMP high) data at the Y outputs. In addition, the 'ALS857 perform the logical AND function (A · B) and the clear function as well. The four modes of operation are:

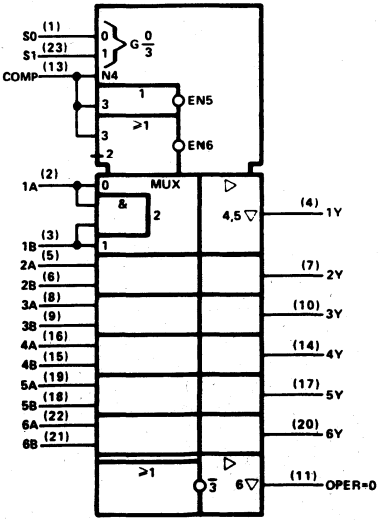
Select A data inputs,
Select B data inputs,
AND A inputs with B inputs,
Clear

In either of the first two modes, OPER = 0 is high if all the selected A or B inputs are low.

The six Y outputs and the OPER = 0 output are all three-state and rated at 12 mA and 24 mA I_{OL} for the SN54ALS857 and SN74ALS857, respectively. All outputs can be placed into the high-impedance state by applying a high level to the COMP, S0, and S1 inputs simultaneously. The complete function table is shown below.

The SN54ALS857 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS857 is characterized for operation from 0°C to 70°C.

logic symbol†

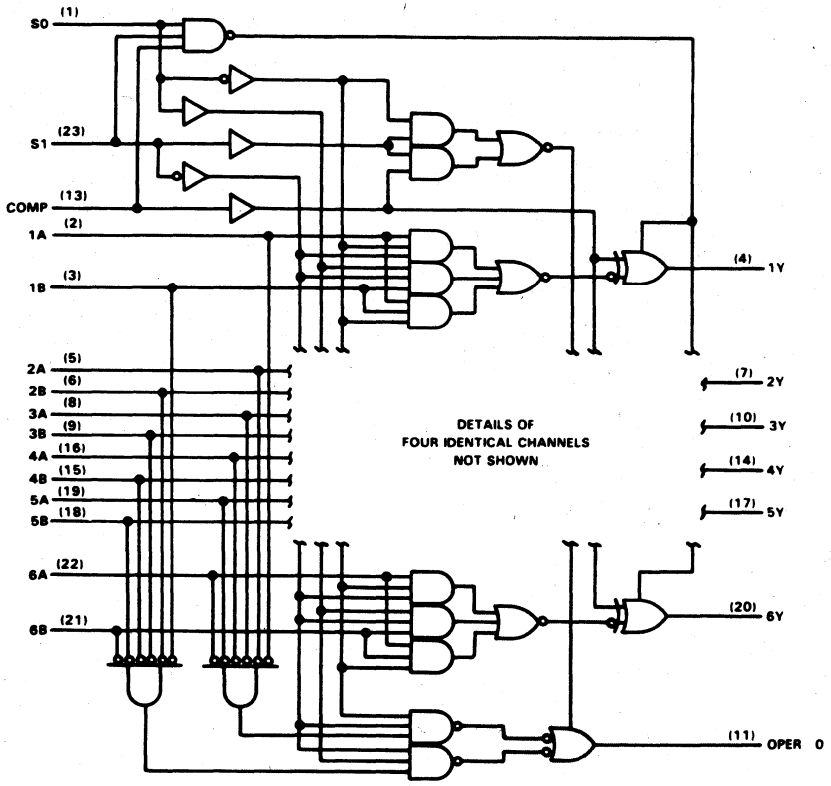


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

FUNCTION TABLE

COMP	S1	S0	Y OUTPUTS	OPER = ZERO
L	L	L	A	H = all A inputs L
L	L	H	B	H = all B inputs L
L	H	L	A•B	Z
L	H	H	L	L
H	L	L	$\overline{A}$	H = all A inputs L
H	L	H	$\overline{B}$	H = all B inputs L
H	H	L	$\overline{A \cdot B}$	Z
H	H	H	Z	Z

'ALS857 logic diagram (positive logic)



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperaure range: SN54ALS857 . . . . . −55°C to 125°C
SN74ALS857 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS857			SN74ALS857			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS857			SN74ALS857			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	V_{CC} = 5.5 V, See Note 1	Outputs high		11	24		11	24	mA
		Outputs low		16	33		16	33	
		Outputs disabled		18	36		18	36	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with all possible inputs grounded while achieving the stated output conditions.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V. to 5.5 V., C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS857		SN74ALS857		
			MIN	MAX	MIN	MAX	
t_{pd}	A or B (COMP high)	Y (Inverting)	4	28	4	25	ns
t_{pd}	A or B (COMP low)	Y (Noninverting)	4	21	4	18	ns
t_{pd}	S0 or S1	Y	7	37	7	33	ns
t_{pd}	COMP	Y	6	22	6	18	
t_{pd}	A or B	OPER = 0	5	45	5	37	
t_{pd}	S0 to S1	OPER = 0	5	30	5	23	
t_{en}	S0 to S1	Y	7	38	7	35	ns
t_{dis}			2	29	2	23	
t_{en}	COMP	Y	8	27	8	24	ns
t_{dis}			6	27	6	21	
t_{en}	S0	OPER = 0	6	24	6	20	ns
t_{dis}			11	34	11	27	
t_{en}	S1	OPER = 0	6	28	6	25	ns
t_{dis}			3	23	3	19	
t_{en}	COMP	OPER = 0	9	30	9	25	ns
t_{dis}			6	24	6	20	

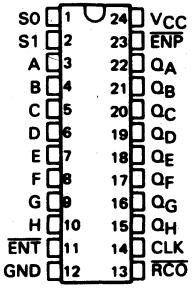
t_{pd} = t_{PLH} or t_{PHL}
t_{en} = t_{PZH} or t_{PAL}
t_{dis} = t_{PHZ} or t_{PLZ}
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

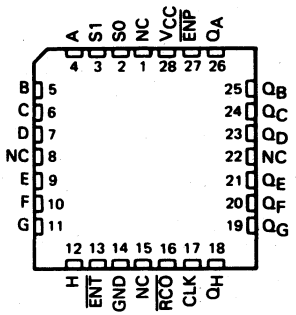
D2661, DECEMBER 1982 – REVISED JUNE 1988

- **Fully Programmable with Synchronous Counting and Loading**
- **'ALS867A and 'AS867 Have Asynchronous Clear, 'ALS869 and 'AS869 Have Synchronous Clear**
- **Fully Independent Clock Circuit Simplifies Use**
- **Ripple Carry Output for n-Bit Cascading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54' . . . JT PACKAGE
SN74' . . . DW OR NT PACKAGE
(TOP VIEW)



SN54' . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the eight flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, they may each be preset to any number between 0 and 255. The load-mode circuitry allows parallel loading of the cascaded counters. As loading is synchronous, selecting the load mode disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

FUNCTION TABLE

S1	S0	FUNCTION
L	L	Clear
L	H	Count down
H	L	Load
H	H	Count up

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{ENP}$ and $\overline{ENT}$) must be low to count. The direction of the count is determined by the levels of the select inputs (see Function Table). Input $\overline{ENT}$ is fed forward to enable the carry output. The ripple carry output thus enabled will produce a low-level pulse while the count is zero (all outputs low) counting down or 255 counting up (all outputs high). This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable $\overline{ENP}$ and $\overline{ENT}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

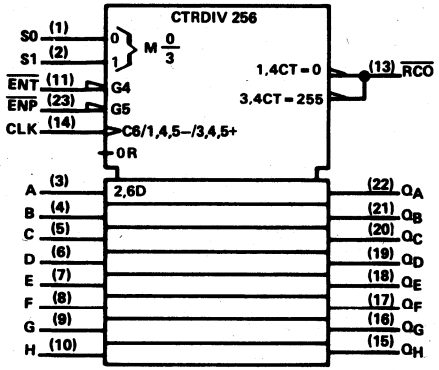
TEXAS INSTRUMENTS

These counters feature a fully independent clock circuit. With the exception of the asynchronous clear on the '867, changes at control inputs (S0, S1) that will modify the operating mode have no effect on the Q outputs until clocking occurs. For 'AS867 and 'AS869, anytime the $\overline{ENP}$ and/or $\overline{ENT}$ is taken high, $\overline{RCO}$ will either go or remain high. For 'ALS867A and 'ALS869, anytime the $\overline{ENT}$ is taken high, $\overline{RCO}$ will either go or remain high. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

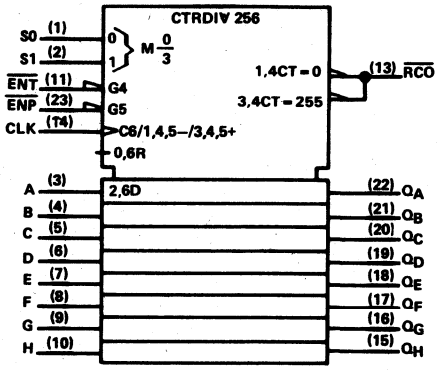
The SN54ALS' and SN54AS' are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS' and SN74AS' are characterized for operation from 0°C to 70°C.

logic symbols†

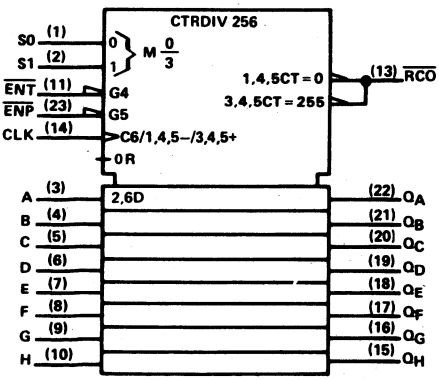
'ALS867A



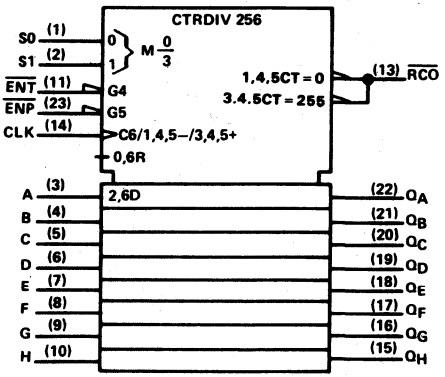
'ALS869



'AS867

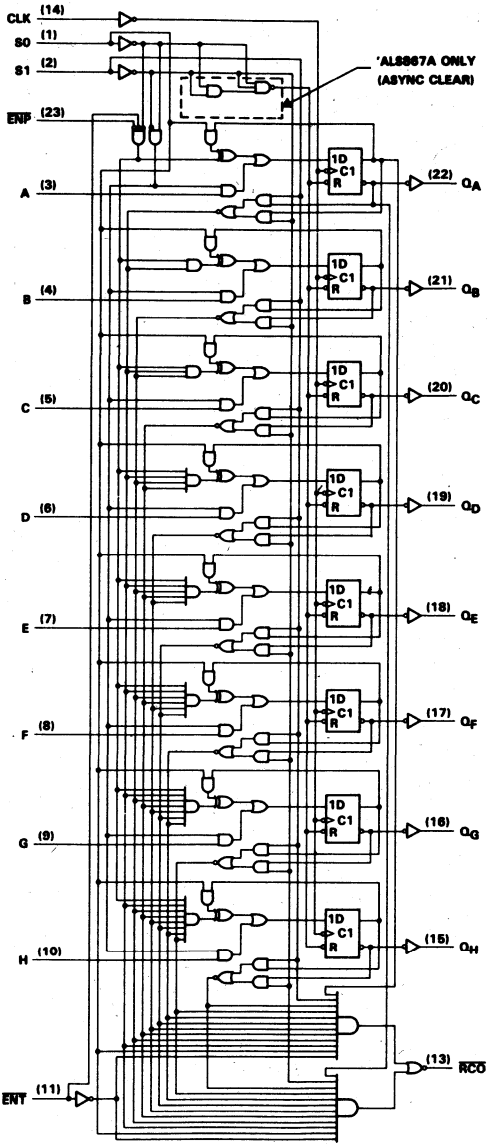


'AS869



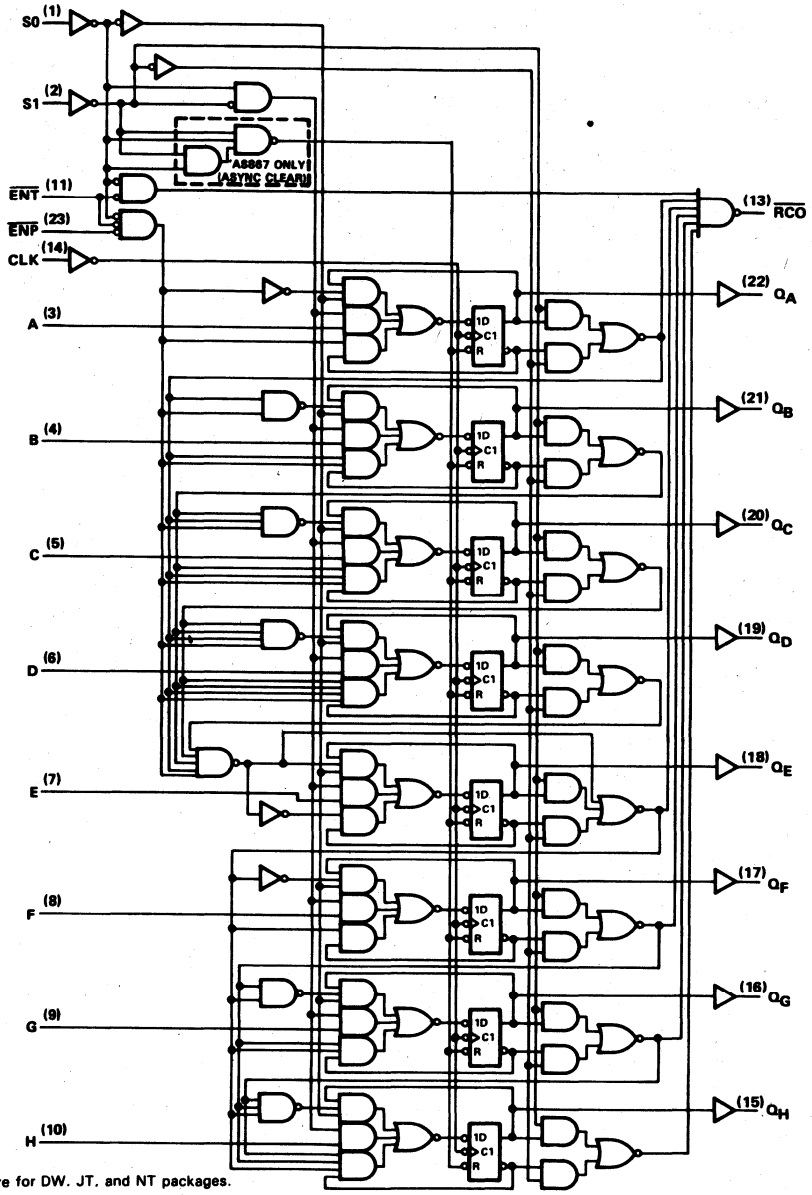
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are
for DW, JT, and NT packages.

logic diagram
(positive logic)



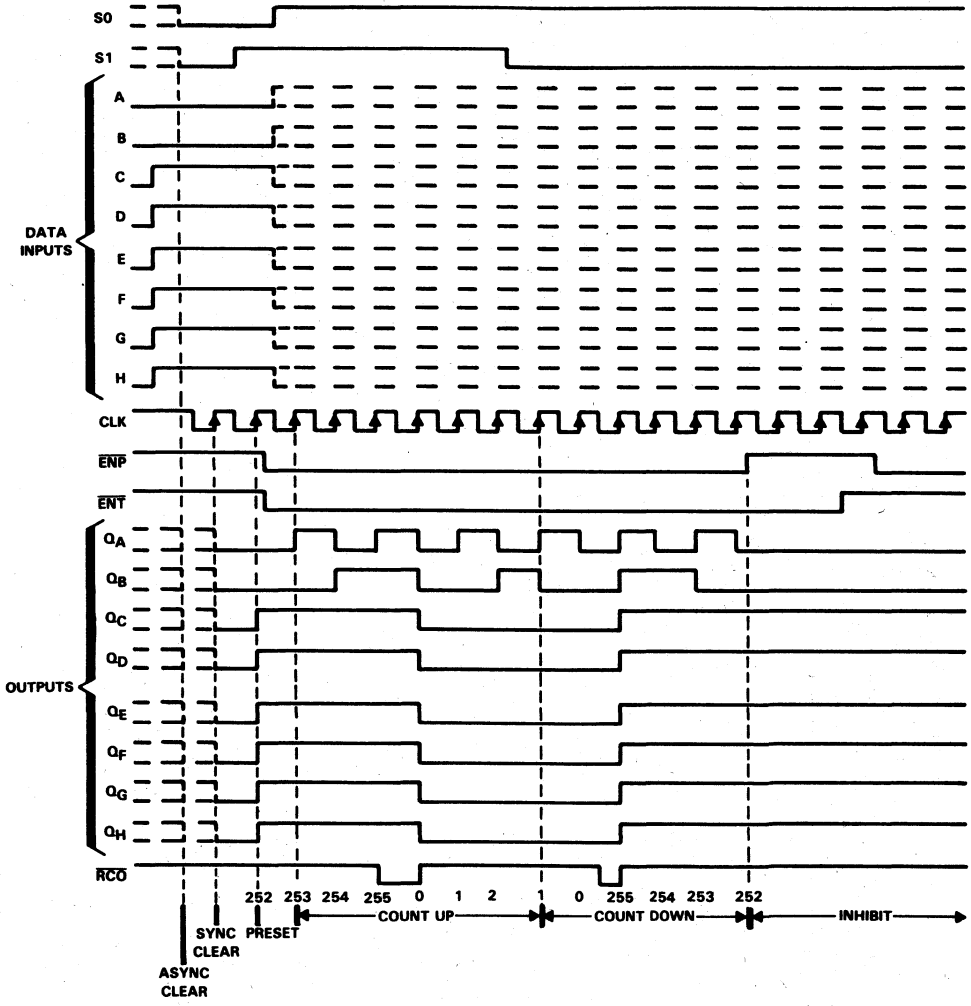
Pin numbers shown are for DW, JT, and NT packages.

TEXAS INSTRUMENTS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero ('ALS867 and 'AS867 are asynchronous; 'ALS869 and 'AS869 are synchronous)
2. Preset to binary 252
3. Count up to 253, 254, 255, 0, 1, and 2
4. Count down to 1, 0, 255, 254, 253, and 252
5. Inhibit



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−0.4	mA
I_{OL}	Low-level output current				8	mA
f_{clock}	Clock frequency		0		35	MHz
$t_{w(clock)}$	Pulse duration, clock high or low		14			ns
$t_{w(clear)}$	Duration of clear pulse (S0 and S1 low)		10			ns
t_{su}	Setup time before CLK↑	Data inputs A-H	10			ns
		$\overline{ENP}$ or $\overline{ENT}$	15			ns
		S0 low and S1 high (load)	12			ns
		S0 high and S1 low (count down)	12			ns
		S0 and S1 high (count up)	12			ns
t_h	Hold time after CLK↑	S0 high after S1↑ or S1 high after S0↑	3			ns
		Data inputs A-H	0			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			28	45	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN74ALS869 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN74ALS869			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−0.4	mA
I_{OL}	Low-level output current				8	mA
f_{clock}	Clock frequency		0		35	MHz
$t_{w\ (clock)}$	Pulse duration, clock high or low		14			ns
t_{su}	Setup time before CLK ↑	Data inputs A-H	10			ns
		$\overline{ENP}$ or $\overline{ENT}$	15			ns
		S0 ans S1 low (clear)	13			ns
		S0 low and S1 high (load)	13			ns
		S0 high and S1 low (count down)	13			ns
		S0 and S1 high (count up)	13			ns
t_h	Hold time after CLK ↑	S0 high after S1 ↑ or S1 high after S0 ↑	3			ns
		Data inputs A-H	0			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS869			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			28	45	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS867A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 0°C to 70°C		UNIT
			TYP	MAX	MIN	MAX	
f_{max}			40		35		MHz
t_{PLH}	CLK	$\overline{RCO}$	8	11	4	14	ns
t_{PHL}			8	11	4	14	
t_{PLH}	CLK	Any Q	8	13	3	16	ns
t_{PHL}			8	13	3	16	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	7	10	3	14	ns
t_{PHL}			5	7	2	9	
t_{PHL}	S0 or S1 (clear mode)	Any Q	15	20	8	26	ns
t_{PLH}	S0 or S1 (count up/down)	$\overline{RCO}$	9	12	4	16	ns
t_{PHL}			9	12	4	16	
t_{PLH}	S0 or S1 (clear mode)	$\overline{RCO}$	9	12	4	16	ns

'ALS869 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX		UNIT
			'ALS869		SN74ALS869		
			TYP	MAX	MIN	MAX	
f_{max}			40		35		MHz
t_{PLH}	CLK	$\overline{RCO}$	8	10	4	14	ns
t_{PHL}			8	10	4	14	
t_{PLH}	CLK	Any Q	8	13	3	16	ns
t_{PHL}			8	13	3	16	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	7	10	3	14	ns
t_{PHL}			5	7	2	9	
t_{PLH}	S1 (count up/down)	$\overline{RCO}$	7	11	4	15	ns
t_{PHL}			7	11	4	15	
t_{PLH}	S0 (clear/load)	$\overline{RCO}$	7	11	4	16	ns
t_{PHL}			6	9	4	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature: SN54AS867 . . . . . −55°C to 125°C
SN74AS867 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS867			SN74AS867			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		40	0		50	MHz
$t_{w(clock)}$	Pulse duration, clock high or low		12.5			10			ns
$t_{w(clear)}$	Duration of clear pulse (S0 and S1 low)		12.5			10			ns
t_{su}	Setup time before CLK↑	Data inputs A-H	5			4			ns
		$\overline{ENP}$ or $\overline{ENT}$	9			8			ns
		S0 low and S1 high (load)	11			10			ns
		S0 and S1 (clear)	11			10			ns
		S0 high and S1 low (count down)	42			40			ns
		S0 and S1 high (count up)	42			40			ns
t_h	Hold time after CLK↑	Data inputs A-H	0			0			ns
t_{skew}	Skew time between S0 and S1 (maximum to avoid inadvertent clear)				8			7	ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS867			SN74AS867			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.34	0.5		0.34	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	$\overline{ENT}$	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	Other inputs					20			20	
I_{IL}	$\overline{ENT}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−4			−4	mA
	Other inputs					−2			−2	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			134	195		134	195	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature: SN54AS869 . . . . . −55°C to 125°C
SN74AS869 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS869			SN74AS869			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency				40			45	MHz
$t_{w(clock)}$	Pulse duration, clock high or low		12.5			11			ns
t_{su}	Setup time before CLK↑	Data inputs A-H	6			5			ns
		$\overline{ENP}$ or $\overline{ENT}$	10			9			ns
		S0 low and S1 high (load)	13			11			ns
		S0 and S1 low (clear)	13			11			ns
		S0 high or S1 low (count down)	52			50			ns
		S0 or S1 high (count up)	52			50			ns
t_h	Hold time after CLK↑	Data inputs A-H	0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS869			SN74AS869			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.34	0.5		0.34	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	$\overline{ENT}$	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	µA
	Other inputs					20			20	
I_{IL}	$\overline{ENT}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−4			−4	mA
	Other inputs					−2			−2	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			134	195		134	195	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS867 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 500 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS867		SN74AS867		
			MIN	MAX	MIN	MAX	
f_{max}			40		50		MHz
t_{PLH}	CLK	$\overline{RCO}$	5	31	5	22	ns
t_{PHL}			6	19	6	16	
t_{PLH}	CLK	Any Q	3	12	3	11	ns
t_{PHL}			4	16	4	15	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	3	19	3	10	ns
t_{PHL}			5	21	5	17	
t_{PLH}	$\overline{ENP}$	$\overline{RCO}$	5	14	5	14	ns
t_{PHL}			5	21	5	17	
t_{PHL}	Clear (S0 or S1 low)	Any Q	7	23	7	21	ns

'AS869 switching characteristics (see Note 1)

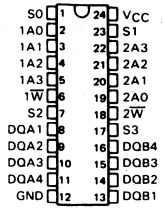
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 500 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS869		SN74AS869		
			MIN	MAX	MIN	MAX	
f_{max}			40		45		MHz
t_{PLH}	CLK	$\overline{RCO}$	6	35	6	35	ns
t_{PHL}			6	20	6	18	
t_{PLH}	CLK	Any Q	3	12	3	11	ns
t_{PHL}			4	16	4	15	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	3	25	3	15	ns
t_{PHL}			6	21	6	17	
t_{PLH}	$\overline{ENP}$	$\overline{RCO}$	5	27	5	19	ns
t_{PHL}			6	21	6	18	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, DECEMBER 1982 – REVISED OCTOBER 1991

- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Each Register File Has Individual Write Enable Controls and Address Lines**
- **Designed Specifically for Multibus Architecture and Overlapping File Operations**
- **Prioritized B Input Port Prevents Write Conflicts During Dual Input Mode**
- **Dependable Texas Instruments Quality and Reliability**

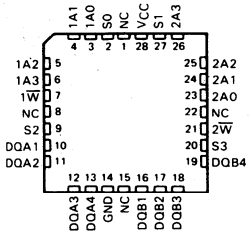
SN54ALS870 . . . JT PACKAGE
SN74ALS870 . . . DW OR NT PACKAGE
(TOP VIEW)



description

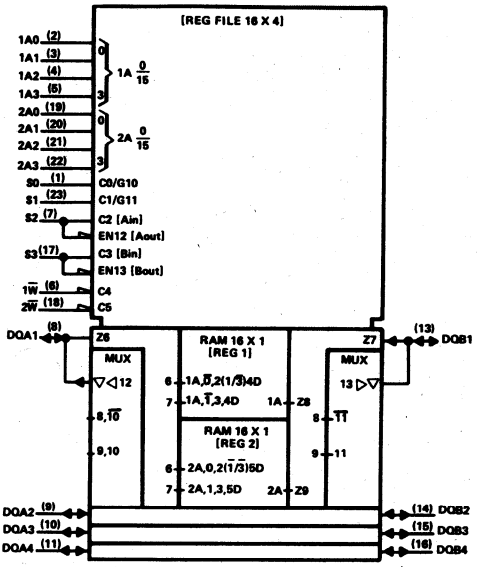
These devices features two 16-word by 4-bit register files. Each register file has individual write-enable controls and address lines. The 'ALS870 has two 4-bit data I/O ports (DQA1-DQA4 and DQB1-DQB4). The data I/O ports can output to Bus A and Bus B, receive input from Bus A and Bus B, receive input from Bus A and output to Bus B, or output to Bus A and receive input from Bus B. To prevent writing conflicts in the dual-input mode, the B input port takes priority. Two select lines, S0 and S1, control which port has access to which register. S2 determines whether the A ports are in the input or the output modes and S3 does likewise for the B ports. The address lines (1A0-1A3 or 2A0-2A3) are decoded by an internal 1-of-16 decoder to select which register word is to be accessed. All outputs are 3-state buffer-type outputs designed specifically to drive bus lines directly.

SN54ALS870 . . . FK PACKAGE
(TOP VIEW)



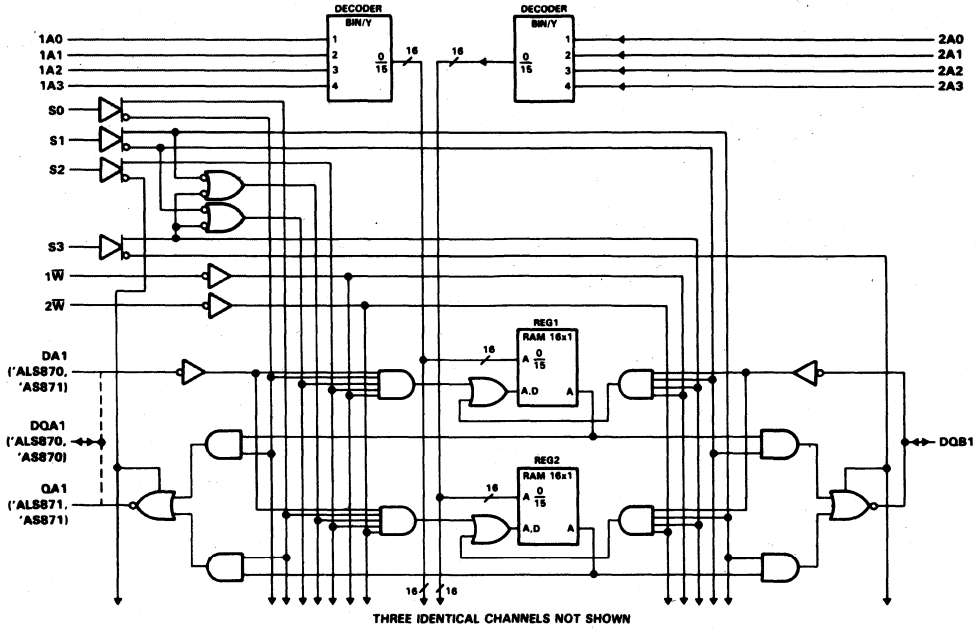
logic symbol†

'ALS870



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publications 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



FUNCTION TABLE

FILE SELECT			INPUT/OUTPUT		
S0	S1	FILE SEL	S2	S3	I/O SEL
L	L	1R TO A, 1R TO B	L	L	A OUT, B OUT
H	L	2R TO A, 1R TO B			
L	H	1R TO A, 2R TO B			
H	H	2R TO A, 2R TO B			
L	L	A TO 1R, 1R TO B	H	L	A IN, B OUT
H	L	A TO 2R, 1R TO B			
L	H	A TO 1R, 2R TO B			
H	H	A TO 2R, 2R TO B			
L	L	1R TO A, B TO 1R	L	H	A OUT, B IN
H	L	2R TO A, B TO 1R			
L	H	1R TO A, B TO 2R			
H	H	2R TO A, B TO 2R			
L	L	B TO 1R	H	H	A IN, B IN
H	L	A TO 2R, B TO 1R			
L	H	A TO 1R, B TO 2R			
H	H	B TO 2R			

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS870 . . . . . −55 °C to 125 °C
SN74ALS870 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS870			SN74ALS870			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Duration of write pulse		12			12			ns
t_{su}	Setup times	Address before write↓	5			5			ns
		Data before write↑	15			15			
		Select before write↓	12			12			
t_h	Hold times	Address after write↑	0			0			ns
		Data after write↑	0			0			
		Select after write↑	12			12			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS870			SN74ALS870			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	DQA and DQB ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.2			0.2	
I_{IH}	1$\overline{W}$ and 2$\overline{W}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	Other control inputs					40			40	
	DQA and DQB ports‡					50			50	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	DQA and DQB ports‡					−0.2			−0.2	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			80	110		80	110	mA

switching characteristics (see Note 1)

PARAMETER	FROM (INTPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS870			SN54ALS870		SN74ALS870		
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Any A	Any DQ		10	18	3	24	3	19	ns
$t_{a(S)}$	S0	Any DQA		8	14	3	18	3	15	ns
	S1	Any DQB		8	14	3	18	3	15	
t_{dis}	S2	Any DQA		6	11	3	18	3	14	ns
	S3	Any DQB		6	11	3	18	3	14	
t_{en}	S2	Any DQA		7	14	3	20	3	17	ns
	S3	Any DQB		7	14	3	20	3	17	
t_{pd}	$\overline{W}$	Any DQ		12	20	5	26	5	23	ns
	DQA	DQB		13	22	5	29	5	26	
	DQB	DQA		13	22	5	29	5	26	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN74ALS873B, SN74AS873A, SN54ALS873B, SN54AS873
DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

D2661, APRIL 1982 – REVISED MAY 1989

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **'ALS880A and 'AS880 are Alternative Versions with Inverting Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These dual 4-bit registers feature three-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

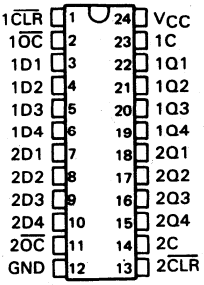
The dual 4-bit latches are transparent D-type. While the latch enable input (1C or 2C) is high, the Q outputs will follow the data (D) inputs in true form, according to the function table. When the latch enable input is taken low, the outputs will be latched. When $\overline{CLR}$ goes low, the Q outputs go low independently of enable C. The outputs are in a high-impedance state when $\overline{OC}$ (output control) is at a high logic level.

The SN54ALS873B and SN54AS873 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS873B and SN74AS873A are characterized for operation from 0°C to 70°C.

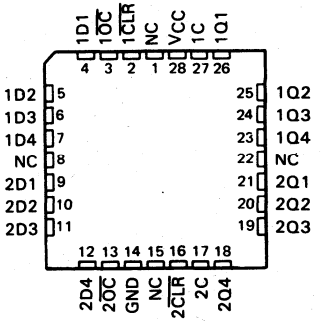
FUNCTION TABLE (EACH LATCH)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	ENABLE C	D	Q
L	L	X	X	L
L	H	H	H	H
L	H	H	L	L
L	H	L	X	Q_0
H	X	X	X	Z

SN54ALS873B, SN54AS873 . . . JT PACKAGE
SN74ALS873B, SN74AS873 . . . DW OR NT PACKAGE
(TOP VIEW)



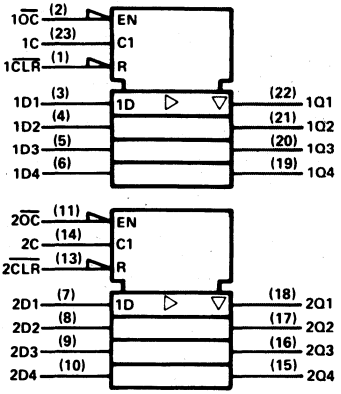
SN54ALS873B, SN54AS873 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

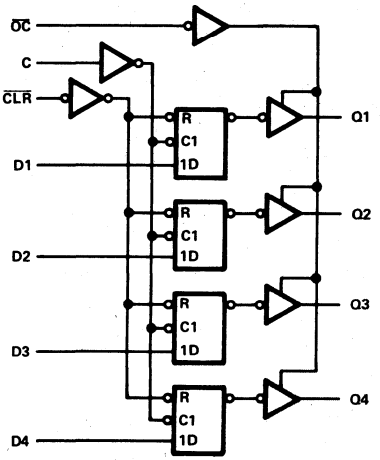
TEXAS INSTRUMENTS

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (each quad latch, positive logic)



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS873B, SN54AS873 . . . . . −55°C to 125°C
SN74ALS873B, SN74AS873A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS873B			SN74ALS873B			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration	$\overline{CLR}$ low	15			15			ns
		Enable C high	10			10			
t_{su}	Setup time, data before enable C↓		10			10			ns
t_h	Hold time, data after enable C↓		7			7			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS873B			SN74ALS873B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		11	21		11	21	mA
		Outputs low		16	29		16	29	
		Outputs disabled		20	31		20	31	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS873B			SN54ALS873B		SN74ALS873B		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q		7	11	2	17	2	14	ns
t_{PHL}				7	10	2	15	2	14	
t_{PLH}	C	Q		13	17	8	29	8	22	ns
t_{PHL}				14	18	8	26	8	21	
t_{PHL}	$\overline{CLR}$	Q		12	16	6	24	6	20	ns
t_{PZH}	$\overline{OC}$	Q		11	14	4	22	4	18	ns
t_{PZL}				11	15	4	23	4	18	
t_{PHZ}	$\overline{OC}$	Q		7	9	2	12	2	10	ns
t_{PLZ}				7	11	2	21	2	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

			SN54AS873			SN74AS873A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration	$\overline{CLR}$ low	4.5			3.5			ns
		Enable C high	5.5			4.5			
t_{su}	Setup time, data before enable C↓		2			2			ns
t_h	Hold time, data after enable C↓		3			3			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS873			SN74AS873A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		68	110		68	110	mA
		Outputs low		67	109		67	109	
		Outputs disabled		80	129		80	129	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS873		SN74AS873A		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3	9	3	9.5	ns
t_{PHL}			3	7	3	6.5	
t_{PLH}	C	Q	6	14	6	13	ns
t_{PHL}			4	9	4	7.5	
t_{PHL}	$\overline{CLR}$	Q	3	8.5	3	9	ns
t_{PZH}	$\overline{OC}$	Q	2	8	2	6.5	ns
t_{PZL}			4	11	4	9.5	
t_{PHZ}	$\overline{OC}$	Q	2	8	2	6.5	ns
t_{PLZ}			2	8.5	2	7.5	

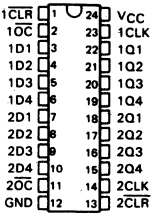
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

D2661, APRIL 1982 – REVISED MAY 1986

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Choice of True or Inverting Logic**
  'ALS874B, 'AS874 True Outputs
  'ALS876A, 'AS876 Inverting Outputs
- **Asynchronous Clear**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS874B, SN54AS874 . . . JT PACKAGE
SN74ALS874B, SN74AS874 . . . DW OR NT PACKAGE
(TOP VIEW)



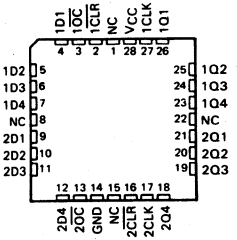
description

These dual four-bit registers feature three-state outputs designed specifically for bus driving. This makes these devices paricularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

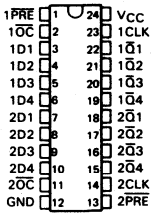
The edge-triggered flip-flops enter data on the low-to-high transition of the clock. The 'ALS874B and 'AS874 have $\overline{CLR}$ inputs and noninverting Q outputs; the 'ALS876A and 'AS876 have $\overline{PRE}$ inputs and inverting Q outputs. In each case, taking this input low causes the four Q or Q outputs to go low independently of the clock.

The SN54ALS' and SN54AS' devices are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS' and SN74AS' devices are characterized for operation from 0°C to 70°C.

SN54ALS874B, SN54AS874 . . . FK PACKAGE
(TOP VIEW)



SN74ALS876A, SN74AS876 . . . DW OR NT PACKAGE
(TOP VIEW)



FUNCTION TABLES

'ALS874B, 'AS874 (EACH FLIP-FLOP)

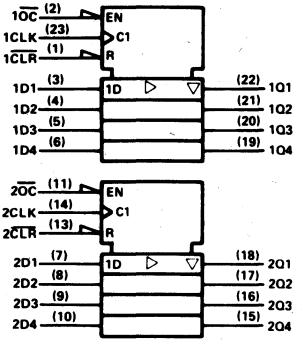
INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	Q
L	L	X	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

'ALS876A, 'AS876 (EACH FLIP-FLOP)

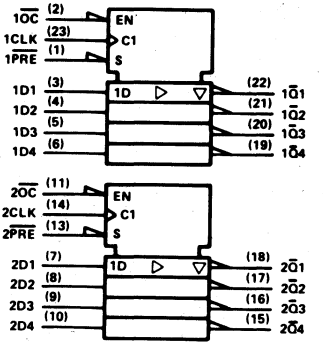
INPUTS				OUTPUT
OC	$\overline{PRE}$	CLK	D	$\overline{Q}$
L	L	X	X	L
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

logic symbols†

'ALS874B, 'AS874



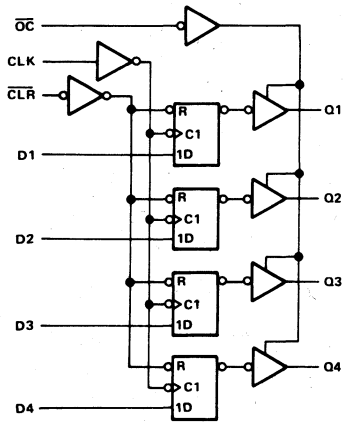
'ALS876A, 'AS876



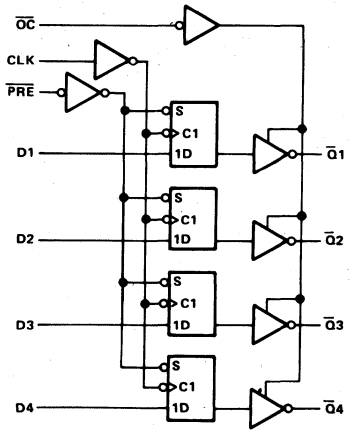
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617.12.

logic diagrams (positive logic)

'ALS874B, 'AS874 (EACH QUAD FLIP-FLOP)



'ALS876A, 'AS876 (EACH QUAD FLIP-FLOP)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54ALS874B . . . . . −55°C to 125°C
SN74ALS874B, SN74ALS876A. . . . . .0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS874B			SN74ALS874B SN74ALS876A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		25	0		30	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	10			10			ns
		CLK high	20			16.5			
		CLK low	20			16.5			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	10			10			
t_h	Hold time, data after CLK↑		4			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS874B			SN74ALS874B SN74ALS876A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS874B	V_{CC} = 5.5 V	Output high		14	21		14	21	mA
			Outputs low		19	30		19	30	
			Outputs disabled		20	32		20	32	
	'ALS876A		Outputs high					14	21	
			Outputs low					18	29	
			Outputs disabled					20	31	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS874B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS874B			SN54ALS874B		SN74ALS874B		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			40	50		25		30		MHz
t_{PLH}	CLK	Any Q		8	10	4	15	4	14	ns
t_{PHL}				8	13	4	15	4	14	
t_{PHL}	$\overline{CLR}$	Any Q		11	14	5	20	5	17	ns
t_{PZH}	$\overline{OC}$	Any Q		9	12	4	21	4	18	ns
t_{PZL}				11	15	4	21	4	18	
t_{PHZ}	$\overline{OC}$	Any Q		6	8	2	12	2	10	ns
t_{PLZ}				5.7	8	3	15	3	12	

'ALS876A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			'ALS876A			SN74ALS876A		
			MIN	TYP	MAX	MIN	MAX	
f_{max}			40	50		30		MHz
t_{PLH}	CLK	Any $\overline{Q}$		8	11	4	14	ns
t_{PHL}				9	12	4	14	
t_{PHL}	$\overline{PRE}$	Any $\overline{Q}$		10	16	6	19	ns
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$		10	13	4	18	ns
t_{PZL}				11	15	4	18	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$		6	8	2	10	ns
t_{PLZ}				7	10	3	13	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS874 . . . . . −55°C to 125°C
SN74AS874, SN74AS876 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS874			SN74AS874 SN74AS876			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency		0		100	0		125	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4			2			ns
		CLK high	4			3			
		CLK low	5			4			
t_{su}	Setup time before CLK↑	Data	2.5			2			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	5			4			
t_h	Hold time, data after CLK↑		1			1			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS874			SN74AS874 SN74AS876			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.4				V
		V_{CC} = 4.5 V	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			10	μA
I_{IL}	D	V_{CC} = 5.5 V,	V_I = 0.4 V			−3			−2	mA
	All other					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS874	V_{CC} = 5.5 V	Output high		82	133		82	133	mA
			Outputs low		92	149		92	149	
			Outputs disabled		100	160		100	160	
	'AS876		Outputs high					88	142	
			Outputs low					94	150	
			Outputs disabled					100	160	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS874 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS874		SN74AS874		
			MIN	MAX	MIN	MAX	
f_{max}			100		125		MHz
t_{PLH}	CLK	Any Q	3	11.5	3	8.5	ns
t_{PHL}			4	12.5	4	10.5	
t_{PHL}	$\overline{CLR}$	Any Q	4	11	4	9.5	ns
t_{PZH}	$\overline{OC}$	Any Q	2	8	2	7	ns
t_{PZL}			3	11.5	3	10.5	
t_{PHZ}	$\overline{OC}$	Any Q	2	7	2	6	ns
t_{PLZ}			2	8.5	2	7.5	

'AS876 switching characteristics (see Note 1)

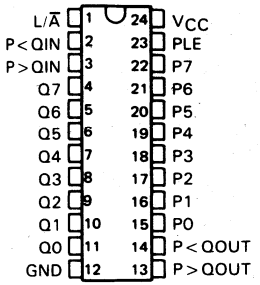
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			SN74AS876		
			MIN	MAX	
f_{max}			125		MHz
t_{PLH}	CLK	Any $\overline{Q}$	3	8.5	ns
t_{PHL}			4	10.5	
t_{PHL}	$\overline{PRE}$	Any $\overline{Q}$	4	9.5	ns
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	2	7	ns
t_{PZL}			3	10.5	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	2	6	ns
t_{PLZ}			2	6	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

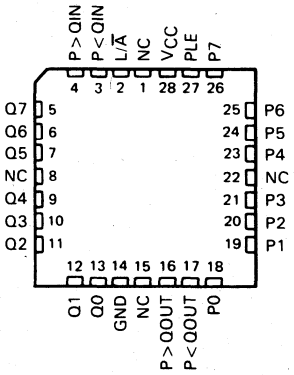
D2661, DECEMBER 1982 – REVISED MARCH 1985

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Latchable P Input Ports with Power-Up Clear**
- **Choice of Logical or Arithmetic (2's Complement) Comparison**
- **Data and PLE Inputs Utilize P-N-P Input Transistors to Reduce DC Loading Effects**
- **Approximately 35% Improvement in AC Performance Over Schottky TTL while Performing More Functions**
- **Cascadable to n-Bits while Maintaining High Performance**
- **10% Less Power than STTL for an 8-Bit Comparison**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS885 . . . . JT PACKAGE
SN74AS885 . . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS885 . . . FK PACKAGE
(TOP VIEW)



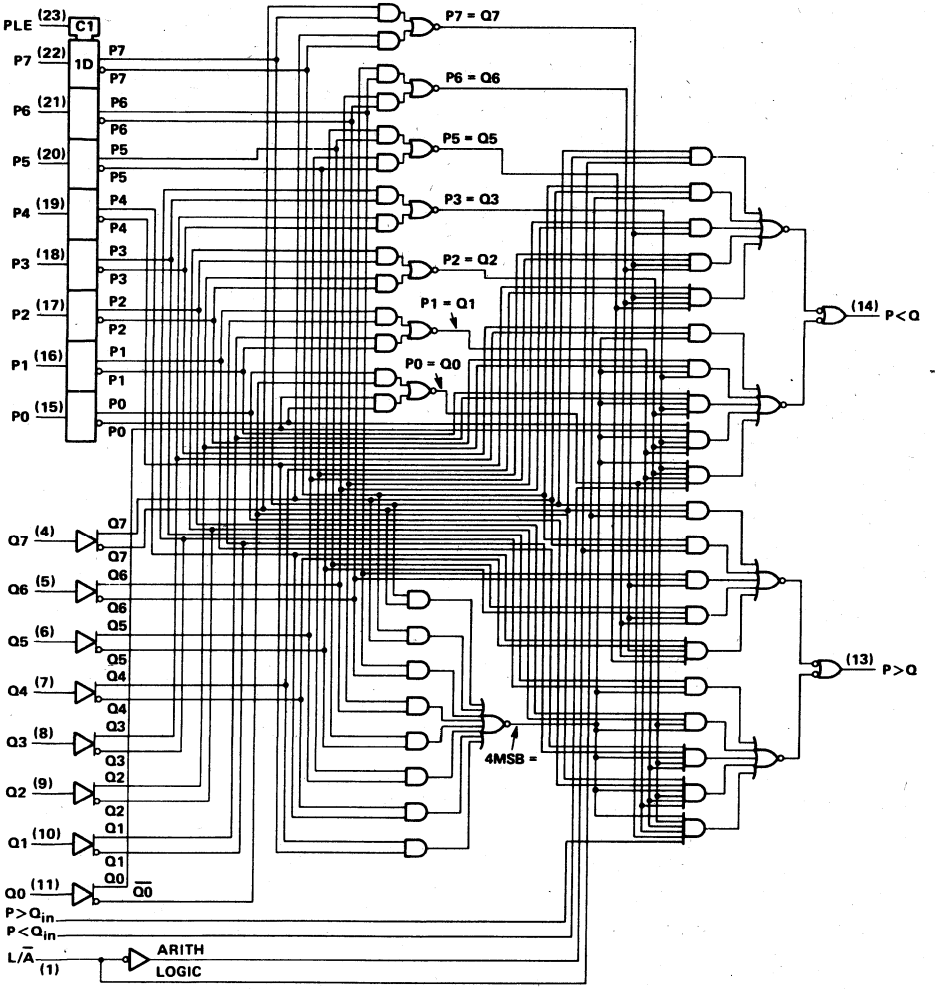
description

These advanced Schottky devices are capable of performing high-speed arithmetic or logic comparisons on two 8-bit binary or two's complement words. Two fully decoded decisions about words P and Q are externally available at two outputs. These devices are fully expandable to any number of bits without external gates. The P > Q and P < Q outputs of a stage handling less-significant bits may be connected to the P > Q and P < Q inputs of the next stage handling more-significant bits to obtain comparisons of words of longer lengths. The cascading paths are implemented with only a two-gate-level delay to reduce overall comparison times for long words. Two alternative methods of cascading are shown in the typical application data.

The latch is transparent when P Latch Enable (PLE) is high; the P input port is latched when PLE is low. This provides the designer with temporary storage for the P data word. The enable circuitry is implemented with minimal delay times to enhance performance when cascaded for longer words. The PLE and P and Q data inputs utilize p-n-p input transistors to reduce the low-level current input requirement to typically −0.25 mA, which minimizes dc loading effects.

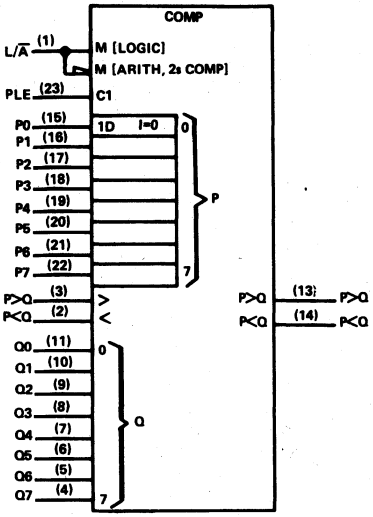
The SN54AS885 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS885 is characterized for operation from 0°C to 70°C.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

FUNCTION TABLE

COMPARISON	L/Ā	DATA INPUTS P0-P7, Q0-Q7	INPUT P>Q	INPUT P<Q	OUTPUTS P>Q	OUTPUTS P<Q
LOGICAL	H	P>Q	X	X	H	L
LOGICAL	H	P<Q	X	X	L	H
LOGICAL‡	H	P=Q	H OR L	H OR L	H OR L	H OR L
ARITHMETIC	L	P AG Q	X	X	H	L
ARITHMETIC	L	Q AG P	X	X	L	H
ARITHMETIC‡	L	P=Q	H OR L	H OR L	H OR L	H OR L

‡In these cases the P>Q output will follow the P>Q input, and the P<Q output will follow the P<Q input.
AG — arithmetically greater than

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS885 . . . . . −55°C to 125°C
SN74AS885 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

PARAMETER		SN54AS885			SN74AS885			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
t_{su}	Setup time to PLE↓	2			2			ns
t_h	Hold time after PLE↓	4			4			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS885			SN74AS885			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	μA
I_{IH}	L/$\overline{A}$	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	Others					20			20	
I_{IL}	L/$\overline{A}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−4			−4	mA
	P > Q_{in} P < Q_{in}					−2			−2	
	P, Q, PLE					−1			−1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−112	−20		−112	mA
I_{CC}		V_{CC} = 5.5 V	See Note 1		130	210		130	210	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current, I_{OS}.
NOTE 1: I_{CC} is measured with all inputs high except L/$\overline{A}$, which is low.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS885			SN74AS885			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	L A	P < Q P > Q		8.5	14		8.5	13	ns
t_{PHL}				7.5	14		7.5	13	
t_{PLH}	P < Q_{in}			5	10		5	8	ns
t_{PHL}	P > Q_{in}			5.5	10		5.5	8	
t_{PLH}	Any P or Q			13.5	21		13.5	17.5	ns
t_{PHL}	Data Input			10	17		10	15	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

The 'AS885 can be cascaded to compare words longer than 8-bits. Figure 1 shows the comparison of two 32-bit words; however, the design is expandable to n-bits. Figure 1 shows the optimum cascading arrangement for comparing words of 32 bits or greater. Typical delay times shown are at V_{CC} = 5 V, T_A = 25°C, and use the standard Advanced Schottky load of R_L = 500 Ω, C_L = 50 pF.

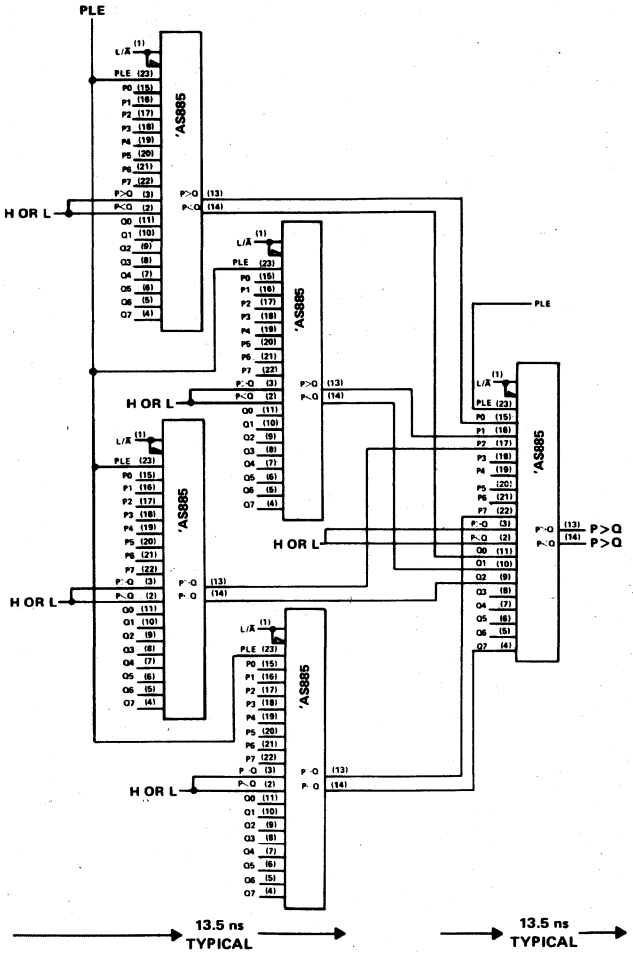


FIGURE 1. 32-BIT TO 72 (N)-BIT MAGNITUDE COMPARATOR

TYPICAL APPLICATION DATA

The method shown in Figure 2 is the fastest cascading arrangement for comparing 16-bit or 24-bit words. Typical delay times shown are at V_{CC} = 5 V, T_A = 25°C, and use the standard Advanced Schottky load of R_L = 500 Ω, C_L = 50 pF.

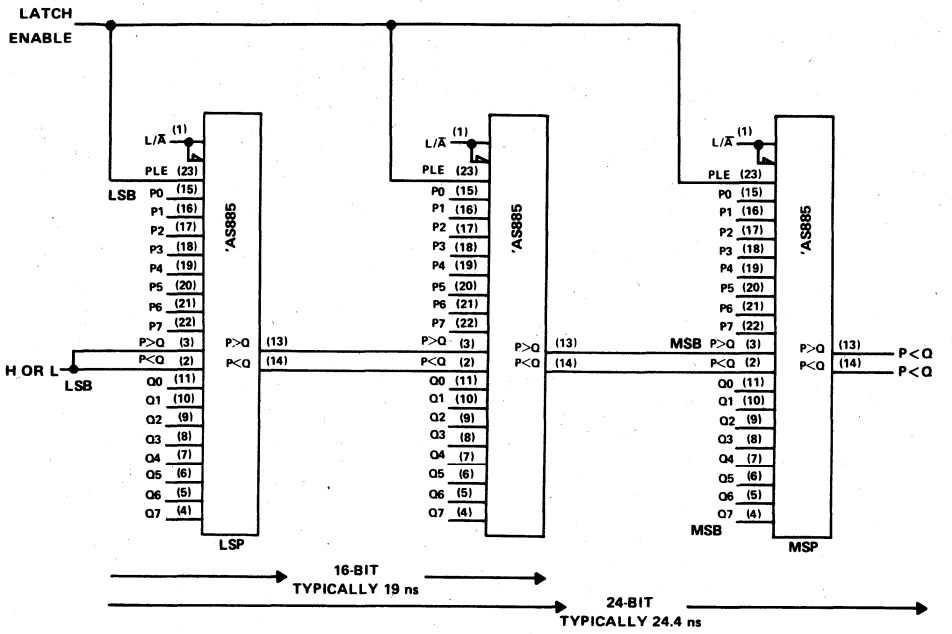


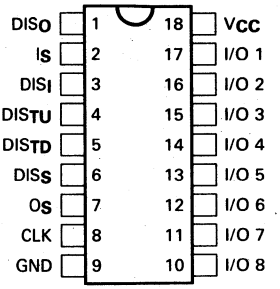
FIGURE 2

SN74ALS962
DUAL RANK 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

APRIL 1989

- **Serial-to-Parallel and Parallel-to Serial Conversion**
- **Data Exchangeable between I/O-Register and Shift Register**
- **Registers are edge-triggered by the positive transition of the clock**
- **All inputs are PNP transistors**
- **Input disable dominates over output disable**
- **3-state I/O buffers are designed for high speed bus-oriented systems**
- **24 mA output low current at I/O ports**
- **16 mA output low current at serial output**
- **Designed in ALS technology for low power consumption**
- **All control inputs are active low**
- **Device can be cascaded to N-bit word**

N PACKAGE
(TOP VIEW)



description

These circuits are 3-state, edge-triggered, 8-bit I/O registers in parallel with 8-bit serial shift registers which are capable of operating in any of the following modes:

parallel load from I/O pins to register 'A',

parallel transfer down from register 'A' to serial shift register 'B',

parallel transfer up from shift register 'B' to register 'A',

serial shift of register 'B' or exchange data between register 'A' and shift register 'B'.

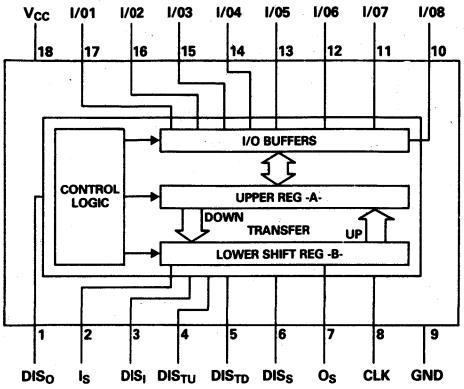
Since the register are edge-triggered by the positive transition of the clock, the control lines which determine the mode or operation are completely independent of the logic level applied to the clock.

Designed for bus-oriented systems, these circuits have their 3-state inputs and outputs on the same pins.

TEXAS INSTRUMENTS

logic symbol

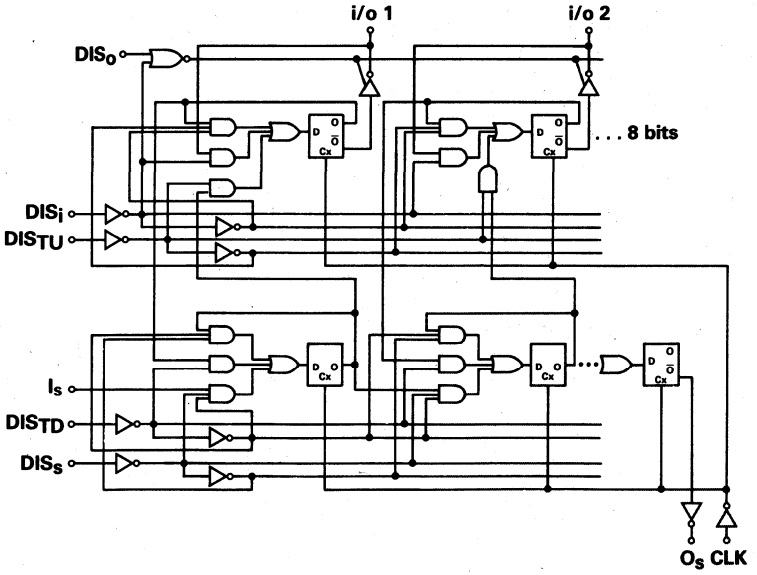
Dual-In-Line Package



Pin Description

DIS_O — Output disable
I_S — Serial input
DIS_I — Input disable
DIS_{TU} — Transfer up disable
DIS_{TD} — Transfer down disable
DIS_S — Shift disable
O_S — Serial output
CLK — Clock
GND — Ground
I/O 1 ... I/O 8 — 8-bit I/O pins
V_{CC} — Supply Voltage

logic diagram



TEXAS INSTRUMENTS

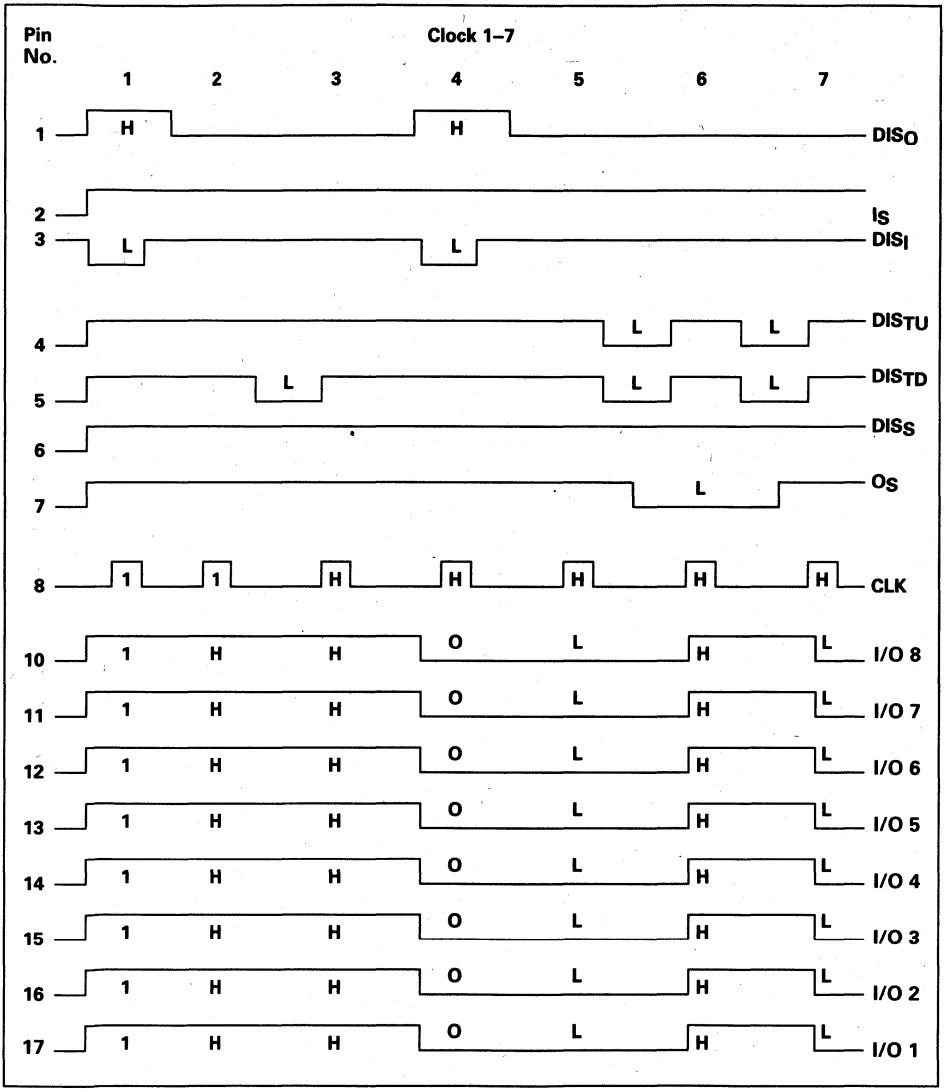
truth tables

TABLE I

	DIS O	DIS I	DIS TU	DIS TD	DIS S	CLK	IS	8-BIT I/O PINS	CONTENT OF UPPER REG. "A" A1 A2 A3 A4 A5 A6 A7 A8	CONTENT OF LOWER SERIAL SHIFT REG. "B" B1 B2 B3 B4 B5 B6 B7 B8	OS	COMMENTS
1	H	H	H	H	H	X	X	Hi-Z	a1 a2 a3 a4 a5 a6 a7 a8	b1 b2 b3 b4 b5 b6 b7 b8	b8	Stable state
2	L	H	H	H	H	X	X	Output	a1 a2 a3 a4 a5 a6 a7 a8	b1 b2 b3 b4 b5 b6 b7 b8	b8	Entering data from I/O
3	X	L	H	H	H	↑	X	Input	I1 I2 I3 I4 I5 I6 I7 I8	b1 b2 b3 b4 b5 b6 b7 b8	b8	to reg. "A"
4	H	H	L	H	H	↑	X	Hi-Z	b1 b2 b3 b4 b5 b6 b7 b8	b1 b2 b3 b4 b5 b6 b7 b8	b8	Transfer data up from
5	L	H	L	H	H	↑	X	Output	b1 b2 b3 b4 b5 b6 b7 b8	b1 b2 b3 b4 b5 b6 b7 b8	b8	reg. "B" to reg."A"
6	X	L	L	H	H	↑	X	Input	◄—— DOR ——►	b1 b2 b3 b4 b5 b6 b7 b8	b8	Reg. "A" will OR data from I/O and reg. "B"
7	H	H	H	L	X	↑	X	Hi-Z	a1 a2 a3 a4 a5 a6 a7 a8	a1 a2 a3 a4 a5 a6 a7 a8	a8	Transfer data down
8	L	H	H	L	X	↑	X	Output	a1 a2 a3 a4 a5 a6 a7 a8	a1 a2 a3 a4 a5 a6 a7 a8	a8	from reg. "A" to reg. "B"
9	X	L	H	L	X	↑	X	Input	I1 I2 I3 I4 I5 I6 I7 I8	a1 a2 a3 a4 a5 a6 a7 a8	a8	Entering data and transfer down
10	H	H	L	L	X	↑	X	Hi-Z	b1 b2 b3 b4 b5 b6 b7 b8	a1 a2 a3 a4 a5 a6 a7 a8	a8	(1) Exchange data between registers
11	L	H	L	L	X	↑	X	Output	b1 b2 b3 b4 b5 b6 b7 b8	a1 a2 a3 a4 a5 a6 a7 a8	a8	(2)
12	X	L	L	L	X	↑	X	Input	◄—— DOR ——►	a1 a2 a3 a4 a5 a6 a7 a8	a8	(3) Beside data exchanging, reg. "A" will "OR" data from I/O and reg. "B"
13	H	H	H	H	L	↑	d	Hi-Z	a1 a2 a3 a4 a5 a6 a7 a8	d b1 b2 b3 b4 b5 b6 b7	b7	Serial shifting in the
14	L	H	H	H	L	↑	d	Output	a1 a2 a3 a4 a5 a6 a7 a8	d b1 b2 b3 b4 b5 b6 b7	b7	lower reg. "B"
15	X	L	H	H	L	↑	d	Input	I1 I2 I3 I4 I5 I6 I7 I8	d b1 b2 b3 b4 b5 b6 b7	b7	Entering data and serial shifting
16	H	H	L	H	L	↑	d	Hi-Z	b1 b2 b3 b4 b5 b6 b7 b8	d b1 b2 b3 b4 b5 b6 b7	b7	Transfer up and serial
17	L	H	L	H	L	↑	d	Output	b1 b2 b3 b4 b5 b6 b7 b8	d b1 b2 b3 b4 b5 b6 b7	b7	shifting
18	X	L	L	H	L	↑	d	Input	◄—— DOR ——►	d b1 b2 b3 b4 b5 b6 b7	b7	DOR function and serial shifting

X = Don't care
Hi-Z/Output/Input = High impedance state/Output state/Input state
a1 ... a8/b1 ... b8 = The content of the upper register "A"/the lower shift register "B" before the most recent ↑ transition of the clock
I1 ... I8 = The level of steady state inputs of the I/O pins
DOR = "Data ORing function" ORing data from both I/O pins and register "B", i.e. I1+b1, I2+b2, I3+b3, ... I8+b8
d = Data of the serial input

timing diagram (example clock No. 1–7)



H/L = I/O Pins are outputs
1/O = I/O Pins are inputs

TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN74ALS962 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN74ALS962			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	all outputs			−2.6	mA
I_{OL}	Low-level output current	O_S			16	mA
		I/O1 thru I/O8			24	
f_{clock}	Clock frequency		0		25	MHz
Clock Pulse	High pulse width		25	17		ns
	Low pulse width		15	7		
t_{SET-UP}	Data set-up time	CLK↑ → I/O	10			ns
		CLK↑ → I_S	10			
t_{HOLD}	Data hold time		0			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

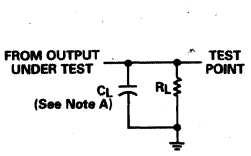
PARAMETER		TEST CONDITIONS		SN74ALS962 MIN	SN74ALS962 TYP†	SN74ALS962 MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
V_{OH}	all outputs	V_{CC} = 4.5 V	I_{OH} = −2.6 mA	2.4	3.0		V
V_{OL}	OS	V_{CC} = 4.5 V	I_{OL} = 8 mA		0.25	0.4	V
			I_{OL} = 16 mA		0.35	0.5	
	I/O1 thru I/O8	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4	
			I_{OL} = 24 mA		0.35	0.5	
I_I	I/O1 thru I/O8	V_{CC} = 5.5 V	V_I = 5.5 V			0.1	mA
	Any other		V_I = 7 V			0.1	
I_{IH}*		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}*		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_{IL} CLK		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
I_O§	all outputs	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		28	50	mA
			Outputs low		40	63	
			Outputs disabled		30	54	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
* For I/O ports (I/O1 through I/O8), the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}. Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

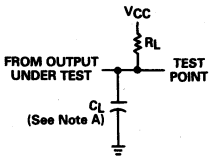
switching characteristics (V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX, C_L = 50 pF, R_L = 500 Ω)

PARAMETER			MIN	TYP	MAX	UNIT
f_{max}	Maximum Clock Frequency		25	30		MHz
t_{PLH}	Propagation Delay Time. Low-to-High-Level from Clock to Any Outputs		2	10	25	ns
t_{PHL}	Propagation Delay Time. High-to-Low-Level from Clock to Any Outputs		5	14	26	ns
t_{ENABLE}	Enable Time from Any Control Inputs		3	10	30	ns
$t_{DISABLE}$	Disable Time from Any Control Inputs		3	10	30	ns
t_{ZH}	Output Enable Time to High-Level			12	30	ns
t_{ZL}	Output Enable to Low-Level			12	30	ns
t_{HZ}	Output Disable Time from High-Level			15	20	ns
t_{LZ}	Output Disable Time from Low-Level			16	20	ns

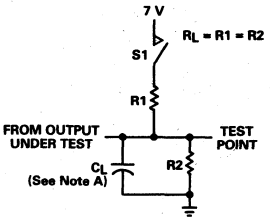
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR
STATE
TOTEM-POLE OUTPUTS

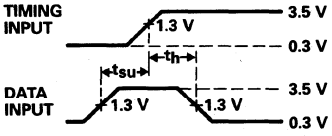


LOAD CIRCUIT FOR
OPEN-COLLECTOR OUTPUTS

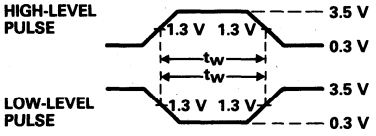


LOAD CIRCUIT FOR
THREE-STATE OUTPUTS

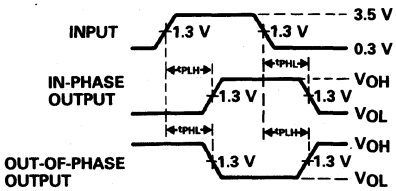
NOTE A: C_L includes probe and jig capacitance.



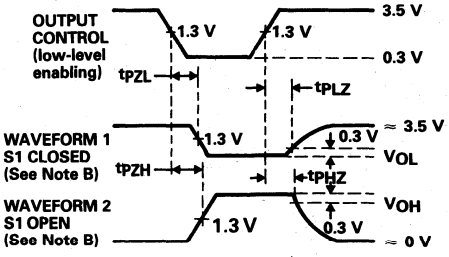
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



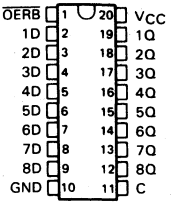
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. When measuring propagation delay items of 3-state outputs, switch S1 is open.
E. The outputs are measured one at a time with one input transition per measurement.

D2835, APRIL 1984 – REVISED MAY 1986

- **3-State I/O-Type Read-Back Inputs**
- **Bus-Structured Pinout**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS990 . . . DW OR N PACKAGE
(TOP VIEW)



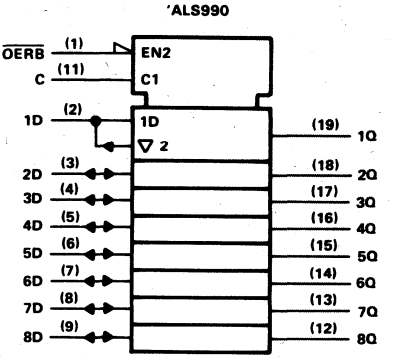
description

These 8-bit latches are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto the input data bus.

The eight latches of the 'ALS990 are transparent D-type. While the enable (C) is high, the Q outputs of the 'ALS990 will follow the data (D) inputs.

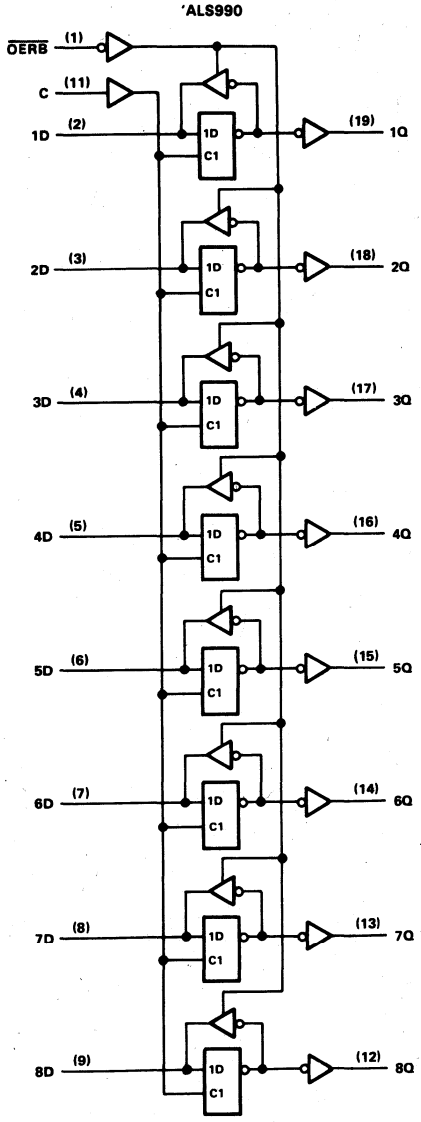
Read-back is provided through the read-back control input ($\overline{OERB}$). When the control is taken low, the data present at the output of the data latches will be allowed to pas back onto the input data bus. When it is taken high, the output of the data latches will be isolated from the data (D) inputs. The read-back control does not affect the internal operation of the latches; however, precautions should be taken not to create a bus-conflict situation.

logic symbol †

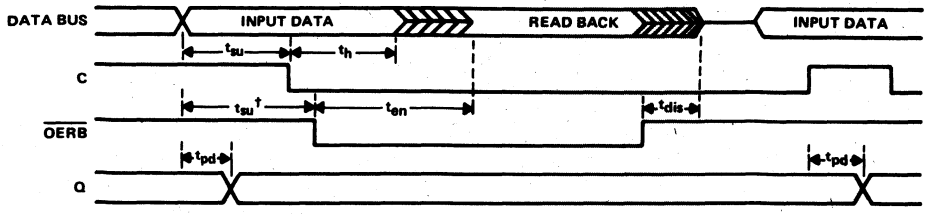


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



timing diagram



† This setup time ensures the readback circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage ($\overline{OERB}$ and C inputs) . . . . . 7 V
Voltage applied to D inputs . . . . . 5.5 V
Operating free-air temperature range: SN74ALS990 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	V
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
I_{OH}	High-level output current		Q			−2.6	mA
			D			−0.4	
I_{OL}	Low-level output current		Q			24	mA
			D			8	
t_w	Pulse duration, enable C high			10			ns
t_{su}	Setup time	Data before C↓		10			ns
		Data before $\overline{OERB}$↓		10			
t_h	Hold time	Data after C↓		5			ns
T_A	Operating free-air temperature			0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
	Q or $\overline{Q}$	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	D	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
	Q or $\overline{Q}$	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
I_I	$\overline{OERB}$, C	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
	D inputs	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	
I_{IH}	$\overline{OERB}$, C	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
	D inputs‡					20	
I_{IL}	$\overline{OERB}$, C	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
	D inputs‡					−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V, $\overline{OERB}$ high	Outputs high		27	50	mA
			Outputs low		40	70	

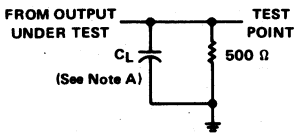
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS990 switching characteristics (see Figure 1)

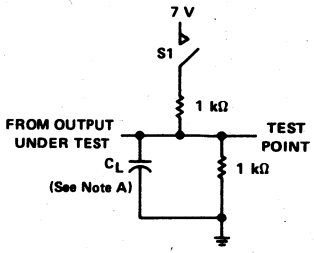
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C, See Figures 1 and 2			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = 0°C to 70°C, See Figures 1 and 2		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	Q		8	14	4	17	ns
t_{PHL}				11	22	5	24	
t_{PLH}	C	Q		13	22	6	26	ns
t_{PHL}				16	23	8	26	
t_{en}	$\overline{OERB}$	D		12	18	4	21	ns
t_{dis}				10	18	4	19	

t_{en} = t_{PZL} or t_{PZH}
t_{dis} = t_{PLZ} or t_{PHZ}

PARAMETER MEASUREMENT INFORMATION

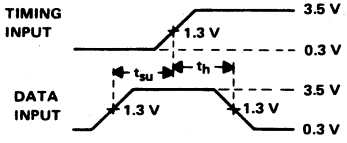


LOAD CIRCUIT FOR
Q OR $\overline{Q}$ OUTPUTS

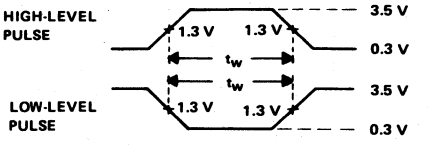


LOAD CIRCUIT FOR D OUTPUTS

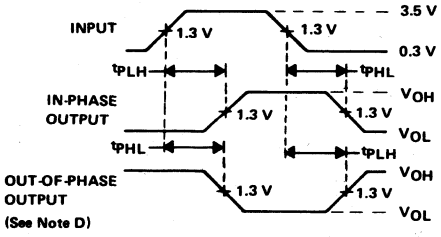
NOTE A: C_L includes probe and jig capacitance.



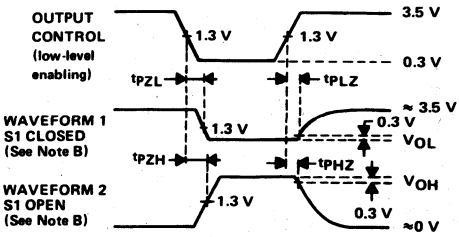
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE WIDTHS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



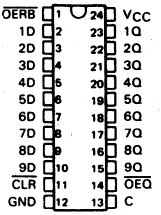
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay items of 3-state outputs, switch S1 is open.

FIGURE 1

- **3-State I/O-Type Read-Back Inputs**
- **Bus-Structured Pinout**
- **Designed with 9 Bits for Parity Applications**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS992 . . . DW OR NT PACKAGE
(TOP VIEW)



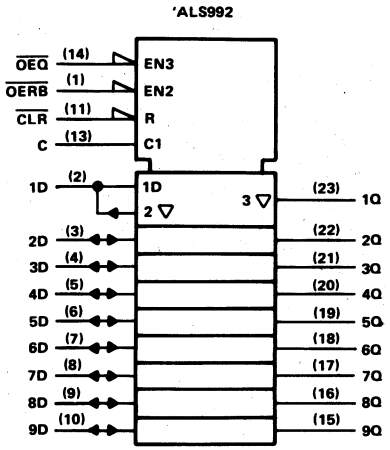
description

These 9-bit latches are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto the input data bus. In addition, they provide a 3-state buffer-type output and are easily implemented in parity applications.

The nine latches of the 'ALS992 are transparent D-type. While the enable (C) is high, the Q outputs of the 'ALS992 will follow the data (D) inputs. The Q outputs will be in the 3-state condition when output enable $\overline{OEQ}$ is high.

Read-back is provided through the read-back control input ($\overline{OERB}$). When the control is taken low, the data present at the output of the data latches will be allowed to pass back onto the input data bus. When it is taken high, the output of the data latches will be isolated from the data (D) inputs. The read-back control does not affect the internal operation of the latches; however, precautions should be taken not to create a bus-conflict situation.

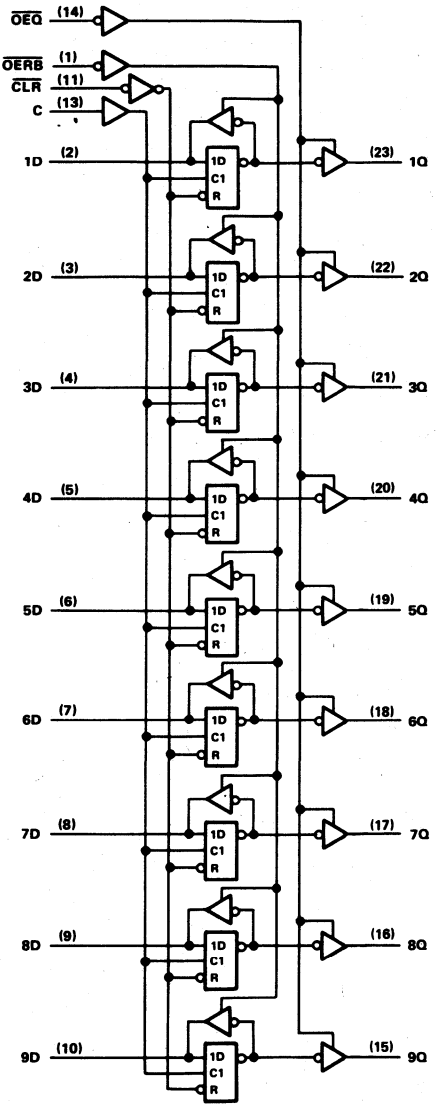
logic symbol†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for DW and NT packages.

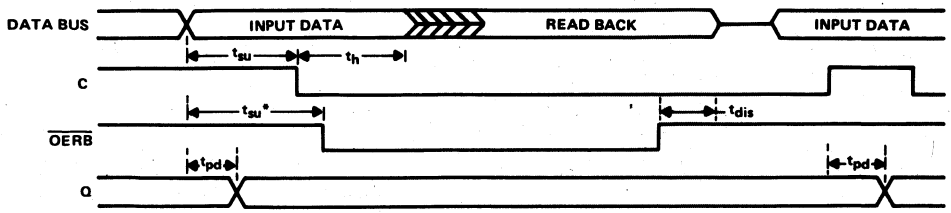
logic diagram (positive logic)

'ALS992



Pin numbers are for DW and NT packages.

timing diagram



$\overline{CLR}$ = H, $\overline{OEQ}$ = L
*This setup time ensures the readback circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, ($\overline{OERB}$, $\overline{OE}$, $\overline{CLR}$, and C inputs) . . . . . 7 V
Voltage applied to D inputs and to disabled 3-state outputs . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q or $\overline{Q}$			−2.6	mA
		D			−0.4	
I_{OL}	Low-level output current	Q or $\overline{Q}$			24	mA
		D			8	
t_w	Pulse duration	Enable C high	10			ns
		$\overline{CLR}$ low	10			
t_{su}	Setup time	Data before C↓	10			ns
		Data before $\overline{OERB}$↓	10			
t_h	Hold time	Data after C↓	5			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
	Q or $\overline{Q}$	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	D	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
	Q or $\overline{Q}$	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
I_{OZH}	Q or $\overline{Q}$	V_{CC} = 5.5 V,	V_O = 2.7 V			20	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	
I_I	D inputs	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	mA
	All other	V_{CC} = 5.5 V,	V_I = 7 V			0.1	
I_{IH}	D inputs‡	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	All other					20	
I_{IL}	D inputs‡	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
	All other					−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V, $\overline{OERB}$ high	Q outputs high		30	50	mA
			Q outputs low		50	80	
			Q outputs disabled		35	55	

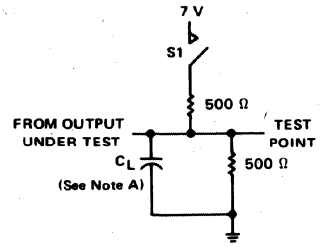
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS992 switching characteristics (see Figure 1)

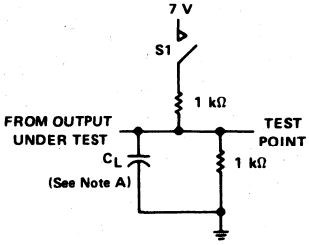
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	Q		7	10	3	14	ns
t_{PHL}				9	13	4	16	
t_{PLH}	C	Q		12	15	6	20	ns
t_{PHL}				15	19	8	25	
t_{PHL}	$\overline{CLR}$	Q		12	16	6	20	ns
t_{PHL}		D		15	22	8	26	
t_{en}	$\overline{OERB}$	D		11	17	4	21	ns
t_{dis}				6	11	2	14	
t_{en}	$\overline{OEQ}$	Q		11	16	4	18	ns
t_{dis}				6	10	1	14	

t_{en} = t_{PZH} or t_{PZL}
t_{dis} = t_{PHZ} or t_{PLZ}

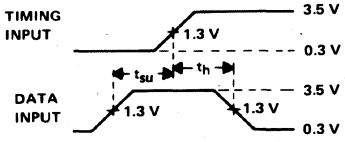
PARAMETER MEASUREMENT INFORMATION



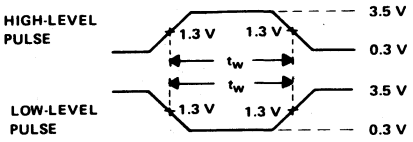
LOAD CIRCUIT FOR
Q OR $\overline{Q}$ OUTPUTS



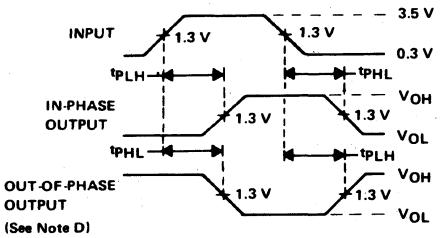
LOAD CIRCUIT FOR D OUTPUTS



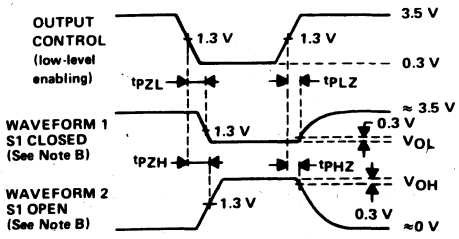
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE WIDTHS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

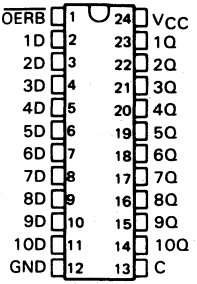
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay items of 3-state outputs, switch S1 is open.

FIGURE 1

D2856, OCTOBER 1984 – REVISED OCTOBER 1991

- **3-State I/O-Type Read-Back Inputs**
- **Bus-Structured Pinout**
- **Choice of True or Inverting Logic**
  'ALS994 . . . True Outputs
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS994 . . . DW OR NT PACKAGE
(TOP VIEW)



description

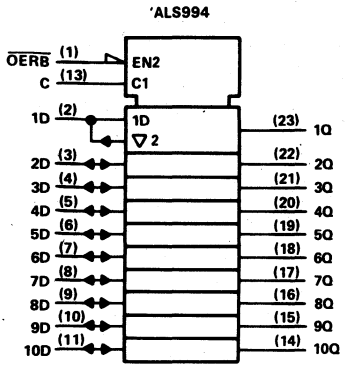
These 10-bit latches are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto the input data bus.

The ten latches of the 'ALS994 are transparent D-type. While the enable (C) is high, the Q outputs of the 'ALS994 will follow the data (D) inputs.

Read-back is provided through the read-back control input ($\overline{OERB}$). When the control is taken low, the data present at the output of the data latches will be allowed to pass back onto the input data bus. When it is taken high, the output of the data latches will be isolated from the data (D) inputs. The read-back control does not affect the internal operation of the latches; however, precautions should be taken not to create a bus-conflict situation.

The SN74ALS994 is characterized for operation from 0 °C to 70 °C.

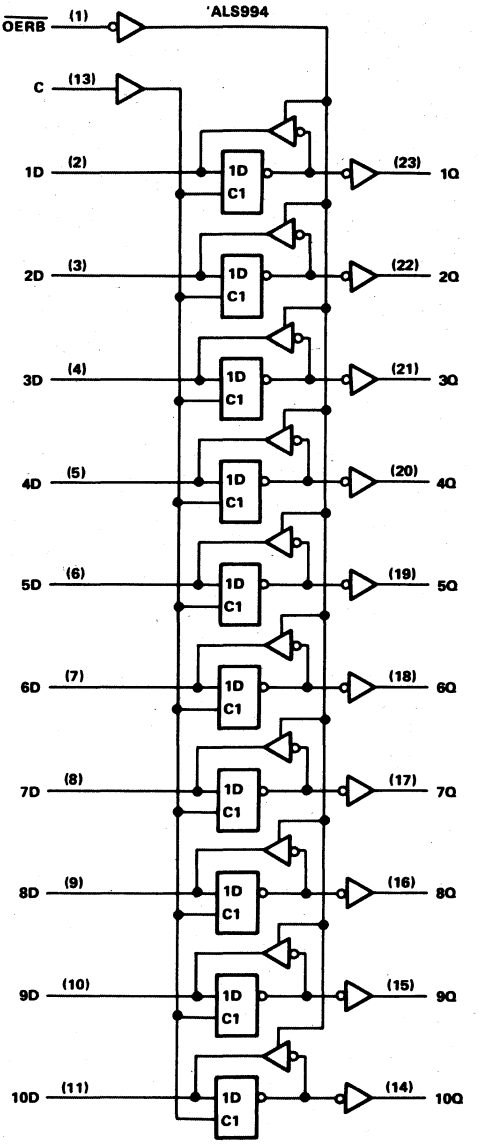
logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW and NT packages.

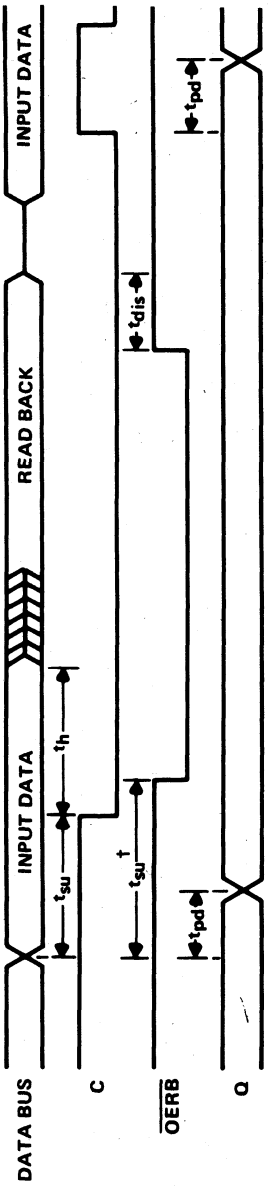
logic diagrams (positive logic)



Pin numbers shown are for DW and NT packages.

TEXAS INSTRUMENTS

timing diagram



†This setup time ensures the readback circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage ($\overline{OERB}$ and C) . . . . . 7 V
Voltage applied to D inputs . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q or $\overline{Q}$			−2.6	mA
		D			−0.4	
I_{OL}	Low-level output current	Q or $\overline{Q}$			24	mA
		D			8	
t_w	Pulse duration, enable C high		10			ns
t_{su}	Setup time	Data before C↓	10			ns
		Data before $\overline{OERB}$↓†	10			
t_h	Hold time	Input data after C↓	5			ns
T_A	Operating free-air temperature		0		70	°C

† This setup time ensures the readback circuit will not create a conflict on the input data bus.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
	Q or $\overline{Q}$	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	D	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
	Q or $\overline{Q}$	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
I_I	$\overline{OERB}$, C	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
	D inputs	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	
I_{IH}	$\overline{OERB}$, C	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
	D inputs‡					20	
I_{IL}	$\overline{OERB}$, C	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
	D inputs‡					−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	'ALS994	V_{CC} = 5.5 V, $\overline{OERB}$ high	Q outputs high		30	50	mA
			Q outputs low		52	82	
	'ALS995		$\overline{Q}$ outputs high		30	50	
			$\overline{Q}$ outputs low		55	85	

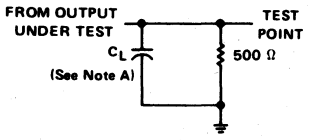
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one-half the true short-circuit output current, I_{OS}.

'ALS994 switching characteristics (see Figure 1)

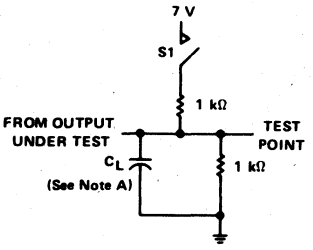
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	Q		7	10	3	14	ns
t_{PHL}				11	15	4	18	
t_{PLH}	C	Q		12	16	6	21	ns
t_{PHL}				16	21	8	27	
t_{en}	$\overline{OERB}$	D		11	17	4	21	ns
t_{dis}				9	13	2	16	

t_{en} = t_{PZH} or t_{PZL}
t_{dis} = t_{PHZ} or t_{PLZ}

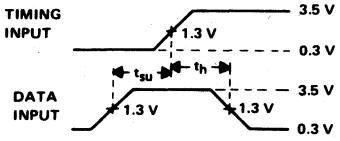
PARAMETER MEASUREMENT INFORMATION



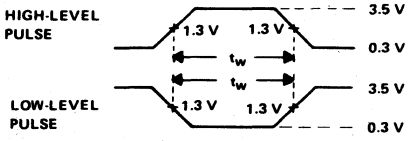
LOAD CIRCUIT FOR
Q OR $\overline{Q}$ OUTPUTS



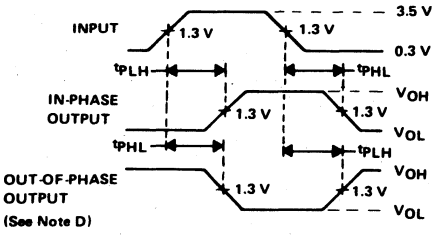
LOAD CIRCUIT FOR D OUTPUTS



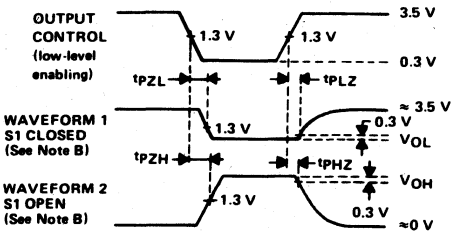
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE WIDTHS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

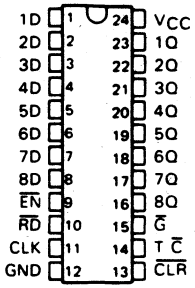
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, t_r = t_f = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

FIGURE 1

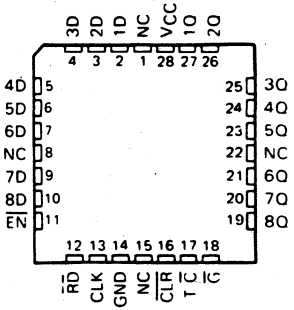
D2854, OCTOBER 1984 – REVISED AUGUST 1989

- **3-State I/O-Type Read-Back Inputs**
- **Bus-Structured Pinout**
- **T/$\overline{C}$ Determines True or Complementary Data at Q Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS996 . . . JT PACKAGE
SN74ALS996 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS996 . . . FK PACKAGE
(TOP VIEW)



NC No internal connection

description

These 8-bit latches are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto that bus. The Q outputs are designed with bus-driving capability.

The edge-triggered flip-flops enter the data on the low-to-high transition of the clock (CLK) when enable ($\overline{EN}$) is low. Data can be read-back onto the data inputs by taking the read input ($\overline{RD}$) low, in addition to having $\overline{EN}$ low. Whenever $\overline{EN}$ is high, both the read-back and write modes are disabled. Transitions on $\overline{EN}$ should only be made with CLK high in order to prevent false clocking.

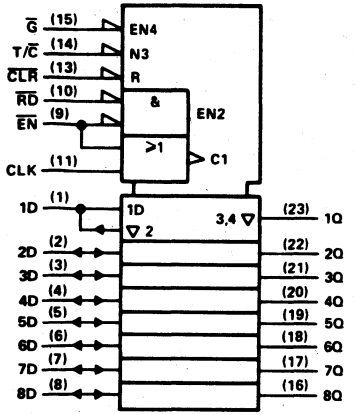
The polarity of the Q outputs can be controlled by the polarity input T/$\overline{C}$. When T/$\overline{C}$ is high, Q will be the same as is stored in the flip-flops. When T/$\overline{C}$ is low, the output data will be inverted. The Q outputs can be placed in a high-impedance state by taking the output control ($\overline{G}$) high. The output control $\overline{G}$ does not affect the internal operations of the register. Old data can be retained or new data can be entered while the outputs are off.

A low level at the clear input ($\overline{CLR}$) resets the internal registers low. The clear function is asynchronous and overrides all other register functions.

The -1 version of the SN74ALS996 is identical to the standard version except that the recommended maximum I_{OL} is increased to 48 milliamperes. There is no -1 version of the SN54ALS996.

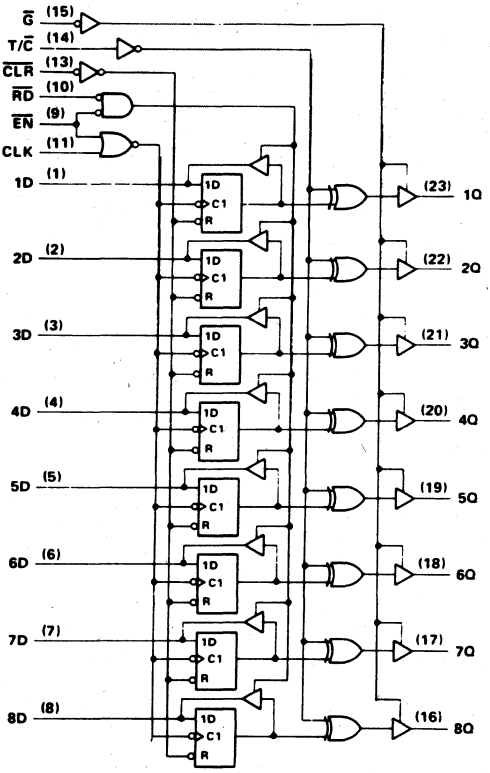
The SN54ALS996 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS996 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

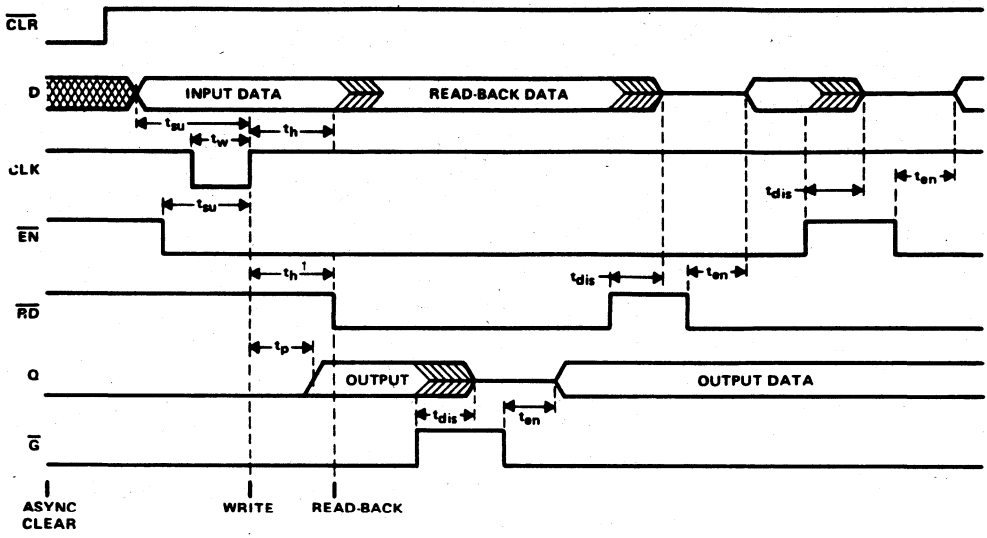


Pin numbers shown are for DW, JT, and NT packages.

TEXAS INSTRUMENTS

timing diagram

($T/\overline{C}$ = H)



†This hold time ensures the readback circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage ($\overline{G}$, $\overline{RD}$, $\overline{EN}$, CLK, $\overline{CLR}$, and T/$\overline{C}$) . . . . . 7 V
Voltage applied to D inputs and to disabled 3-state outputs . . . . . 5.5 V
Operating free-air temperature range: SN54ALS996 . . . . . −55°C to 125°C
SN74ALS996 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS996			SN74ALS996			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	(Commercial) All (Military) All except $\overline{G}$, $\overline{RD}$	2			2			V
		(Military) $\overline{G}$, $\overline{RD}$	2.2						
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	Q			−1			−2.6	mA
		D			−0.4			−0.4	
I_{OL}	Low-level output current	Q			12			24	mA
								48†	
		D			4			8	
f_{clock}	Clock frequency		0		35	0		35	MHz
t_w	Pulse duration	$\overline{CLR}$ low	10			10			ns
		CLK low	14.5			14.5			
		CLK high	14.5			14.5			
t_{su}	Setup time	Data before CLK↑	15			15			ns
		$\overline{EN}$ low before CLK↑	10			10			
		CLK high before $\overline{EN}$↑‡	15			15			
		$\overline{CLR}$ high (inactive) before CLK↑	10			10			
t_h	Hold time	Data after CLK↑	0			0			ns
		$\overline{EN}$ low after CLK↑	5			5			
		$\overline{RD}$ high after CLK↑§	5			5			
T_A	Operating free-air temperature		−55		125	0		70	°C

†The 48-mA limit applies only to the -1 versions and only if V_{CC} is maintained between 4.75 V and 5.25 V.
‡This setup time guarantees that $\overline{EN}$ will not false clock the data register.
§This hold time ensures there will be no conflict on the input data bus.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS996			SN74ALS996			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} −2			V_{CC} −2			V
	Q	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	D	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4				V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
	Q	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
		V_{CC} = 4.5 V,	I_{OL} = 48 mA (-1 versions)					0.35	0.5	
I_{OZH}	Q	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	
I_I	D outputs‡	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	All others	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	
I_{IH}	D inputs‡	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	All others					20			20	
I_{IL}	D inputs‡	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	All others					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V, $\overline{CLR}$ = 2.5 V	V_O = 2.25 V,	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V, $\overline{EN}$, $\overline{RD}$ low	Q outputs high		35	55		35	55	mA
			Q outputs low		55	85		55	85	
			Q outputs disabled		42	65		42	65	

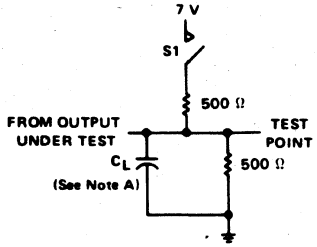
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

switching characteristics (see Figure 1)

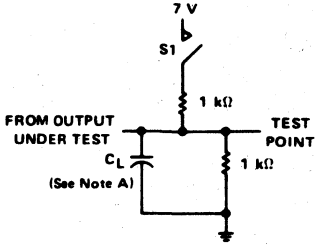
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = MIN to MAX				UNIT
			SN54ALS996		SN74ALS996		
			MIN	MAX	MIN	MAX	
f_{max}			35		35		MHz
t_{PLH}	CLK (T/$\overline{C}$ = H or L)	Q	5	30	5	28	ns
t_{PHL}			5	24	5	28	
t_{PLH}	$\overline{CLR}$ (T/$\overline{C}$ = L)	Q	5	27	7	27	ns
t_{PHL}	$\overline{CLR}$ (T/$\overline{C}$ = H)		5	23	7	23	
t_{PLH}	T/$\overline{C}$	Q	5	23	5	23	ns
t_{PHL}			5	23	5	23	
t_{PHL}	$\overline{CLR}$	D	5	30	8	30	ns
t_{en}	$\overline{RD}$	D	2	17	3	16	ns
t_{dis}			2	19	3	19	
t_{en}	$\overline{EN}$	D	2	16	3	16	ns
t_{dis}			2	19	3	19	
t_{en}	$\overline{G}$	Q	2	15	4	15	ns
t_{dis}			1	11	1	10	

t_{en} = t_{PZH} or t_{PZL}
t_{dis} = t_{PHZ} or t_{PLZ}

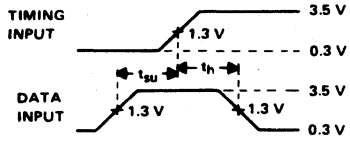
PARAMETER MEASUREMENT INFORMATION



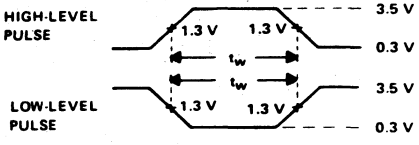
LOAD CIRCUIT FOR Q OUTPUTS



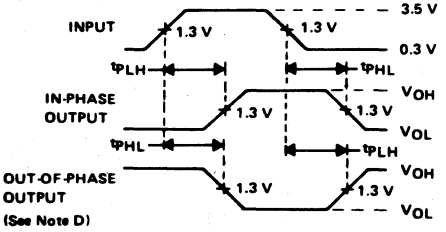
LOAD CIRCUIT FOR D OUTPUTS



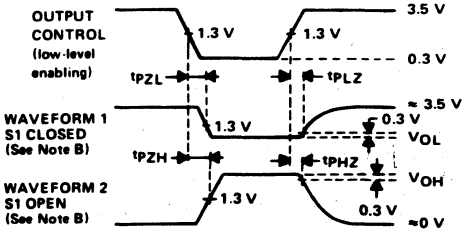
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

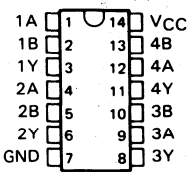
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

FIGURE 1

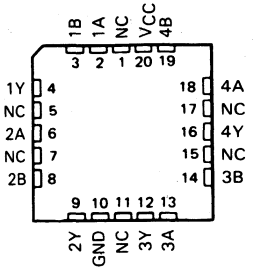
D2661, APRIL 1984 – REVISED MAY 1986

- 'AS1000A is a Driver Version of 'AS00
- 'AS1000A Offers High Capacitive-Driver Capability
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54AS1000A . . . J PACKAGE
SN74AS1000A . . . D OR N PACKAGE
(TOP VIEW)



SN54AS1000A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

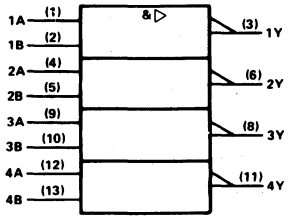
These devices contain four independent 2-input NAND buffers/drivers. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54AS1000A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS1000A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

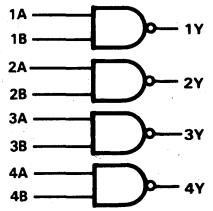
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1000A . . . . . −55°C to 125°C
SN74AS1000A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS1000A			SN74AS1000A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1000A			SN74AS1000A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OL} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−200	−50		−200	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		2.2	3.5		2.2	3.5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		12	19		12	19	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L1 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS1000A		SN74AS1000A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	5	1	4	ns
t_{PHL}	A or B	Y	1	5	1	4	ns

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982 – REVISED MAY 1986

- **'AS1004A Offers High Capacitive-Drive Capability**
- **Driver Version of 'ALS04 and 'AS04**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

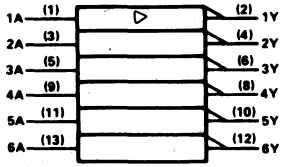
These devices contain six independent inverting drivers. They perform the Boolean function $Y = \overline{A}$.

The SN54AS1004A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1004 and SN74AS1004A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each inverter)

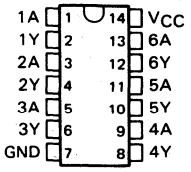
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†

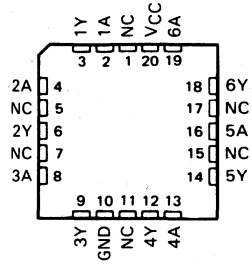


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54AS1004A . . . J PACKAGE
SN74ALS1004, SN74AS1004A . . . D OR N PACKAGE
(TOP VIEW)

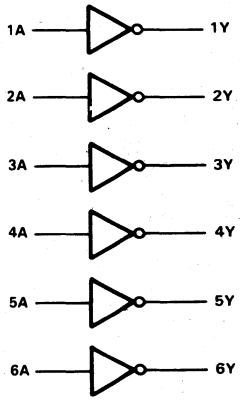


SN54AS1004A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN74ALS1004 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74ALS1004			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS1004			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA				
	V_{CC} = 4.5 V,	I_{OH} = −15 mA	2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V	V_I = 0 V		0.84	3	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		7	12	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX		UNIT
			SN74ALS1004		
			MIN	MAX	
t_{PLH}	A	Y	1	7	ns
t_{PHL}			1	6	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1004A . . . . . −55°C to 125°C
SN74AS1004A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS1004A			SN74AS1004A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1004A			SN74AS1004A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = 40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−200	−50		−200	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		3.5	5		3.5	5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		16	27		16	27	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS1004A		SN74AS1004A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	5	1	4	ns
t_{PHL}			1	5	1	4	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982 – REVISED MAY 1986

- **Buffer Version of 'ALS05**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

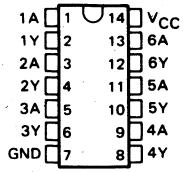
These devices contain six independent inverting buffers. They perform the Boolean function $Y = \overline{A}$. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS1005 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS1005 is characterized for operation from 0 °C to 70 °C.

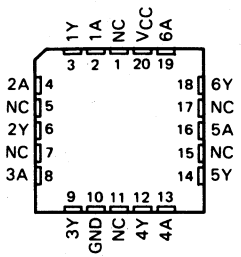
FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
H	L
L	H

SN54ALS1005 . . . J PACKAGE
SN74ALS1005 . . . D OR N PACKAGE
(TOP VIEW)

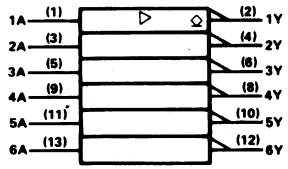


SN54ALS1005 . . . FK PACKAGE
(TOP VIEW)



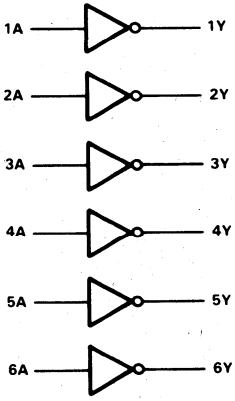
NC – No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1005 . . . . . −55°C to 125°C
SN74ALS1005 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1005			SN74ALS1005			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1005			SN74ALS1005			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.9	3		0.9	3	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		7	12		7	12	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C

switching characteristics (see Note 1)

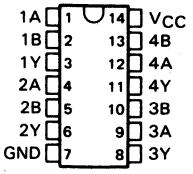
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1005		SN74ALS1005		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	5	35	5	30	ns
t_{PHL}			2	12	2	10	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, DECEMBER 1982 – REVISED MAY 1986

- **'AS1008A is a Driver Version of 'AS08**
- **'AS1008A Offers High Capacitive Drive Capability**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74AS1008A . . . D OR N PACKAGE
(TOP VIEW)



description

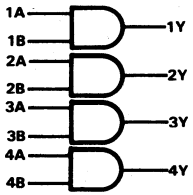
These devices contain four independent 2-input AND buffers/drivers. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A}+\overline{B}}$ in positive logic.

The SN74AS1008A is characterized for operation from 0°C to 70°C.

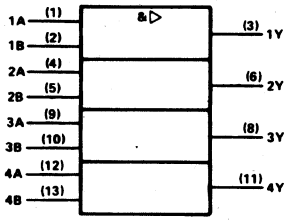
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic diagram (positive logic)



logic symbol†



Pin numbers shown are for D and N packages.

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN74AS1008A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74AS1008A			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−48	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74AS1008A			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA				
	V_{CC} = 4.5 V,	I_{OH} = −48 mA	2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−200	mA
I_{CCH}	V_{CC} = 5.5 V	V_I = 4.5 V		5.6	9.5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		13.5	22	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

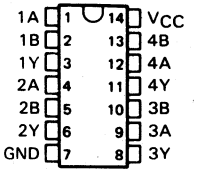
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX		UNIT
			SN74AS1008A		
			MIN	MAX	
t_{PLH}	A or B	Y	1	6	ns
t_{PHL}			1	6	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

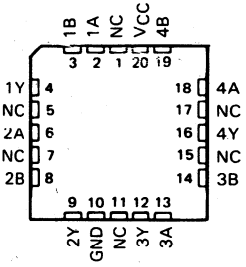
D2661, DECEMBER 1982 – REVISED MAY 1986

- **'AS1032A is a Driver Version of 'AS32**
- **'AS1032A Offers High Capacitive Drive Capability**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS1032A . . . J PACKAGE
SN74AS1032A . . . D OR N PACKAGE
(TOP VIEW)



SN54AS1032A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

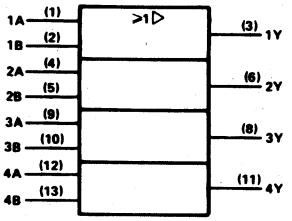
These devices contain four independent 2-input NAND buffers/drivers. They perform the Boolean functions $Y = A + B$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54AS1032A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS1032A is characterized for operation from 0°C to 70°C.

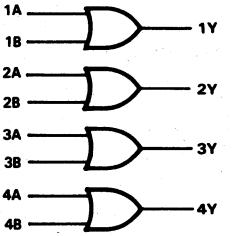
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†



logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1032A . . . . . −55°C to 125°C
SN74AS1032A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS1032A			SN74AS1032A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1032A			SN74AS1032A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−200	−50		−200	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		7.7	11.5		7.7	11.5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		14.7	24		14.7	24	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS1032A		SN74AS1032A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	7	1	6.3	ns
t_{PHL}			1	7	1	6.3	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, APRIL 1982 – REVISED MAY 1986

- **'AS1034A Offers High Capacitive-Drive Capability**
- **Noninverting Drivers**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

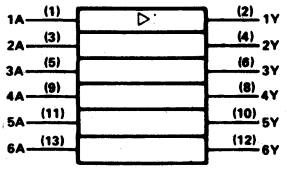
These devices contain six independent noninverting drivers. They perform the Boolean functions Y = A.

The SN54ALS1034 and SN54AS1034A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1034 and SN74AS1034A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each buffer)

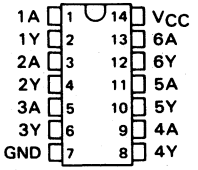
INPUT A	OUTPUT Y
H	H
L	L

logic symbol†

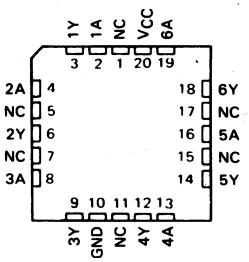


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54ALS1034, SN54AS1034A . . . J PACKAGE
SN74ALS1034, SN74AS1034A . . . D OR N PACKAGE
(TOP VIEW)

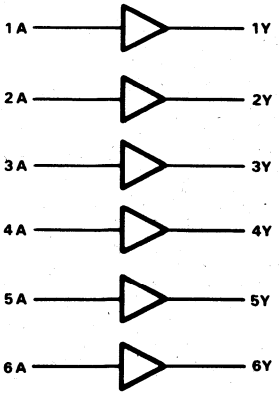


SN54ALS1034, SN54AS1034A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1034 . . . . . −55°C to 125°C
SN74ALS1034 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1034			SN74ALS1034			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output curent			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1034			SN74ALS1034			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4				V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		3	6		3	6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		8	14		8	14	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1034		SN74ALS1034		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	11	1	8	ns
t_{PHL}			1	13	1	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS1034A . . . . . −55°C to 125°C
SN74AS1034A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS1034A			SN74AS1034A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−40			−48	mA
I_{OL}	Low-level output current			40			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1034A			SN74AS1034A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −40 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −48 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 40 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−200	−50		−200	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		9	15		9	15	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		21	35		21	35	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS1034A		SN74AS1034A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	6.5	1	6	ns
t_{PHL}			1	6.5	1	6	

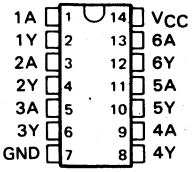
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

HEX NONINVERTING BUFFERS WITH OPEN-COLLECTOR OUTPUTS

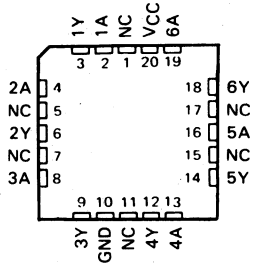
D2661, APRIL 1982 – REVISED MAY 1986

- **Noninverting Buffers with Open-Collector Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS1035 . . . J PACKAGE
SN74ALS1035 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS1035 . . . FK PACKAGE
(TOP VIEW)



NC–No internal connection

description

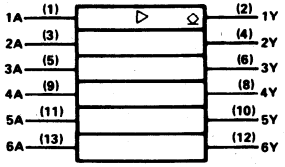
These devices contain six independent noninverting buffers. They perform the boolean functions Y = A. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS1035 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1035 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each buffer)

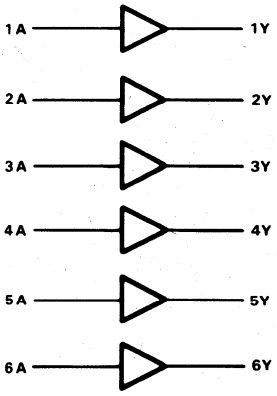
INPUT A	OUTPUT Y
H	H
L	L

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS1035 . . . . . −55°C to 125°C
SN74ALS1035 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1035			SN74ALS1035			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1035			SN74ALS1035			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		3	6		3	6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		8	14		8	14	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1035		SN74ALS1035		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	5	35	5	30	ns
t_{PHL}			2	14	2	12	

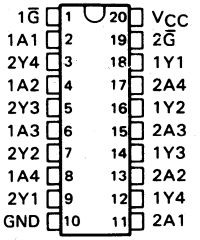
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982 – REVISED MAY 1986

- **Low-Power Version of 'ALS240A**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce DC Loading**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS1240 . . . DW OR N PACKAGE
(TOP VIEW)

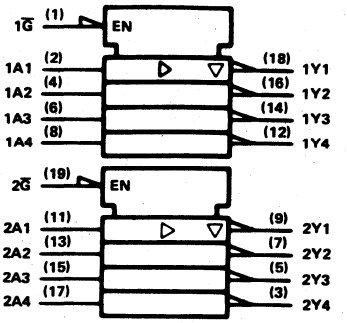


description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out and improved fan-in.

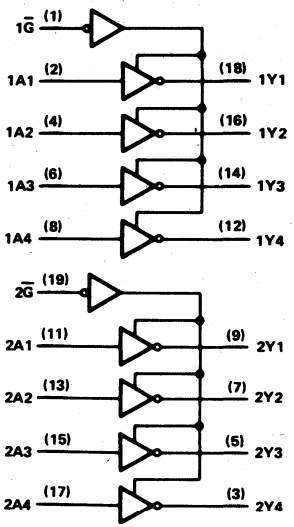
The SN74ALS1240 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN74ALS1240 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74ALS1240			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			16	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS1240			UNIT
			MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA				
	V_{CC} = 4.5 V,	I_{OH} = −15 mA	2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4	V
	V_{CC} = 4.5 V, (I_{OL} = 24 mA for −1 versions)	I_{OL} = 16 mA		0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	µA
I_{OZL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−20	µA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}§	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}§	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_O†	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		5	8	mA
		Outputs low		8.5	14	
		Outputs disabled		8.1	13	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
† The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

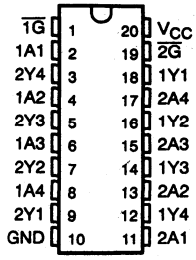
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			'ALS1240	SN74ALS1240		
			TYP	MIN	MAX	
t_{PLH}	A	Y	7.5	2	13	ns
t_{PHL}			6.5	2	13	
t_{PZH}	$\overline{G}$	Y	11.5	4	20	ns
t_{PZL}			14	6	22	
t_{PHZ}	$\overline{G}$	Y	7.5	2	10	ns
t_{PLZ}			8	3	13	

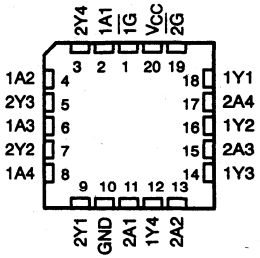
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Low-Power Version of SN74ALS244A-1 and SN54ALS244A**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce DC Loading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54ALS1244A . . . J PACKAGE
SN74ALS1244A . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS1244A . . . FK PACKAGE
(TOP VIEW)



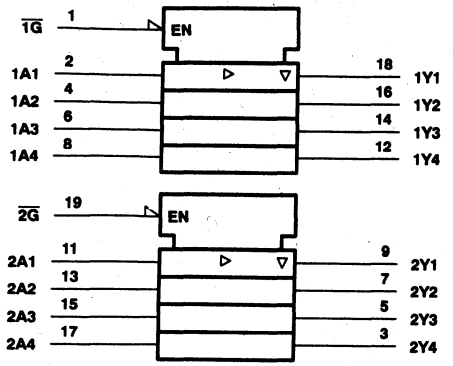
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory drivers, clock drivers, and bus-oriented receivers and transmitters.

Taken together with the 'ALS1240, these devices provide the choice of inverting and noninverting outputs.

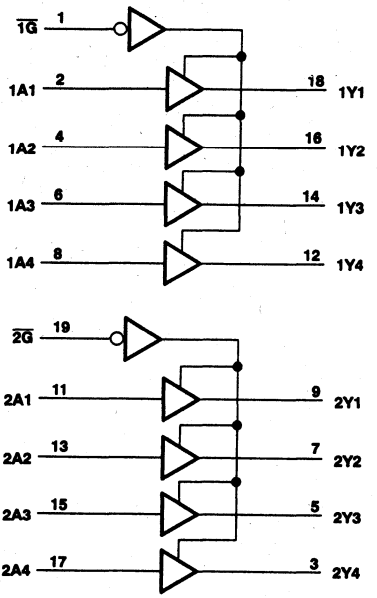
The SN54ALS1244A is characterized over the full military temperature range of −55°C to 125°C. The SN74ALS1244A is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage, V_I ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range: SN54ALS1244A ..... −55°C to 125°C
SN74ALS1244A ..... 0°C to 70°C
Storage temperature range ..... −55°C to 150°C

recommended operation conditions

		SN54ALS1244A			SN74ALS1244A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			8			16	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1244A			SN74ALS1244A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V, (I_{OL} = 24 mA for −1 version)	I_{OL} = 16 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		6	15		6	11	mA
		Outputs low		10	20		10	17	
		Outputs disabled		11	25		11	20	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			SN54ALS1244A		SN74ALS1244B		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	21	3	14	ns
t_{PHL}			3	16	3	14	
t_{PZH}	$\overline{G}$	Y	6	28	6	22	ns
t_{PZL}			6	26	6	22	
t_{PHZ}	$\overline{G}$	Y	2	15	2	13	ns
t_{PLZ}			3	25	3	16	

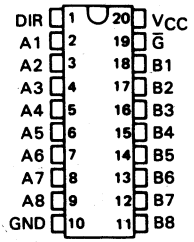
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN74ALS1245A, SN54ALS1245A
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

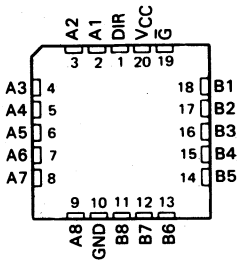
D2661, DECEMBER 1982 – REVISED MAY 1986

- **'Bidirectional Bus Transceivers in High-Density 20-Pin Packages**
- **Lower-Power Version of 'ALS245A**
- **'ALS1245A is Identical to 'ALS1645A**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS1245A . . . J PACKAGE
SN74ALS1245A . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS1245A . . . FK PACKAGE
(TOP VIEW)



description

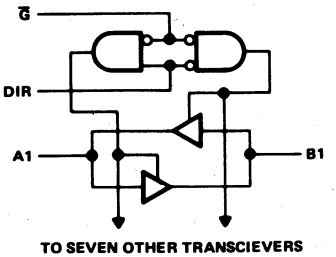
This octal bus transceiver is designed for asynchronous two-way communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G) can be used to disable the device so the buses are effectively isolated.

The SN54ALS1245A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1245A is characterized for operation from 0°C to 70°C.

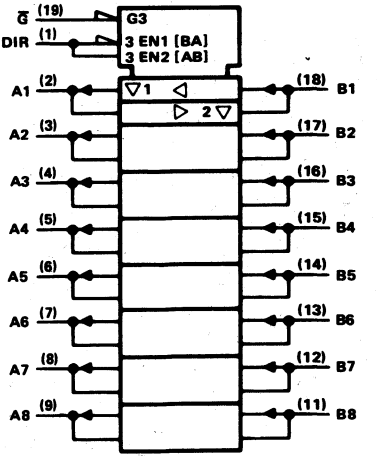
FUNCTION TABLE

CONTROL INPUTS		OPERATION
G	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS1245A . . . . . −55°C to 125°C
SN74ALS1245A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operation conditions

		SN54ALS1245A			SN74ALS1245A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			8			16	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS1245A			SN74ALS1245A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 24 mA for −1 version)	I_{OL} = 16 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A, B ports§	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A, B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A, B ports§					−0.1			−0.1	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Output high		21	33		21	30	mA
			Output low		23	36		23	33	
			Output disabled		25	40		25	36	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

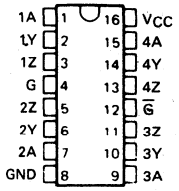
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1245A		SN74ALS1245A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	19	2	13	ns
t_{PHL}			2	15	2	13	
t_{PZH}	$\overline{G}$	A or B	8	30	8	25	ns
t_{PZL}			8	29	8	25	
t_{PHZ}	$\overline{G}$	A or B	2	14	2	12	ns
t_{PLZ}			3	30	3	18	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Equivalent to AM26LS31M**
- **Meets EIA Standard RS-422A**
- **TTL-, DTL-Compatible**
- **Complementary Outputs**
- **High Output Impedance in Power-Off Conditions**
- **Complementary Output Enable Inputs**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS1631 . . . N PACKAGE
(TOP VIEW)



description

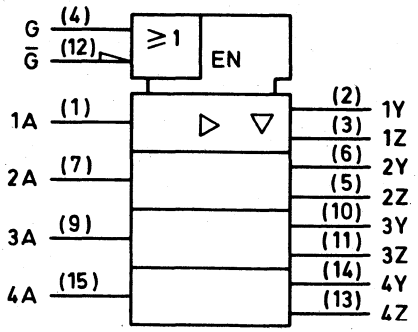
The SN74ALS1631 is quadruple complementary-output line drivers designed to meet the requirements of EIA Standard RS-422 and Federal Standard 1020. The three-stage outputs have high-current capability for driving balanced lines such as twisted-pair or parallel-wire transmission lines, and they provide a high-impedance state in the power-off condition. The enable function in common to all four drivers and offers a choice of active-high of active-low inputs.

FUNCTION TABLE
(EACH DRIVER)

INPUT	ENABLES		OUTPUTS	
A	G	G̅	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level
L = low level
X = irrelevant
Z = high impedance (off)

logic symbol



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Output off-state voltage . . . . . 5.5 V
Operating free-air temperature range: SN74ALS1631 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: All voltage values, except differential output voltage V_O, are with respect to network ground terminal.

recommended operating conditions

		SN74ALS1631			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−33	mA
I_{OL}	Low-level output current			33	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

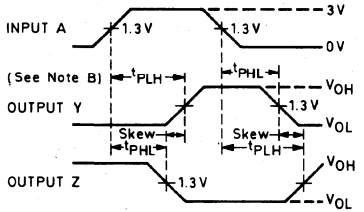
PARAMETER	TEST CONDITIONS		SN74ALS1631			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.7	3.2		V
	V_{CC} = 4.5 V,	I_{OH} = −20 mA				
	V_{CC} = 4.5 V,	I_{OH} = −33 mA	2.4			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 33 mA		0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
I_O*	V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	mA
I_{CC}	V_{CC} = 5.5 V	Outputs disabled		31	45	mA
		Outputs enabled		22	35	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
* The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

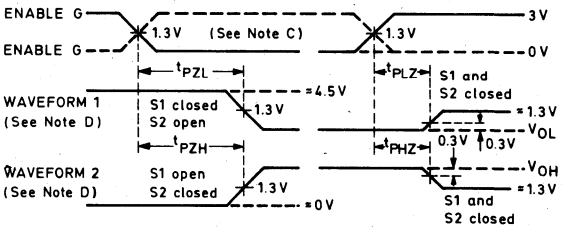
switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_1 = 180 Ω, R_2 = 75 Ω				UNIT
				SN54ALS1631		SN74ALS1631		
				MIN	MAX	MIN	MAX	
tPLH	A	Y/Z	C_L = 30 pF, see Figure 1 S1 and S2 open	2	15	2	12	ns
tPHL	A	Y/Z		4	20	4	16	ns
skew	Y	Z			8		6	ns
tPZH	G/$\overline{G}$	Y/Z	C_L = 30 pF, R_L = 75 Ω, see Figure 1	8	25	8	22	ns
tPZL	G/$\overline{G}$	Y/Z	C_L = 30 pF, R_L = 180 Ω, see Figure 1	8	28	8	25	ns
tPHZ	G/$\overline{G}$	Y/Z	C_L = 10 pF, see Figure 1, S1 and S2 open	2	16	2	14	ns
tPLZ	G/$\overline{G}$	Y/Z		3	27	3	23	ns

PARAMETER MEASUREMENT INFORMATION



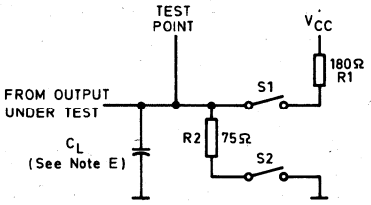
PROPAGATION TIMES AND SKEW



ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS

PROPAGATION DELAY TIMES AND SKEW



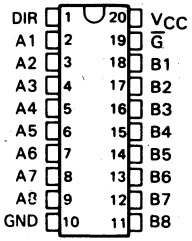
NOTES:
A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} = 50 Ω, t_r and t_f ≤ 2 ns.
B. When measuring propagation delay times and skew, switches S1 and S2 are open.
C. Each enable is tested separately.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES

D2661, DECEMBER 1982 – REVISED MAY 1986

- **Bidirectional Bus Transceivers in High-Density 20-Pin Packages**
- **Lower-Power Versions of 'ALS640 Series**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS' . . . DW OR N PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are effectively isolated. The 'ALS1640A features inverting logic, while the 'ALS1645A features noninverting logic.

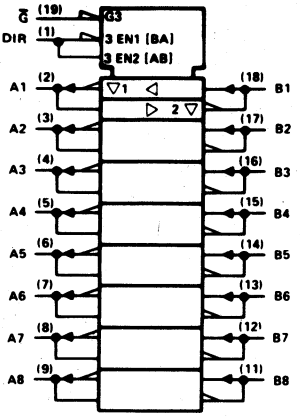
The SN74ALS' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

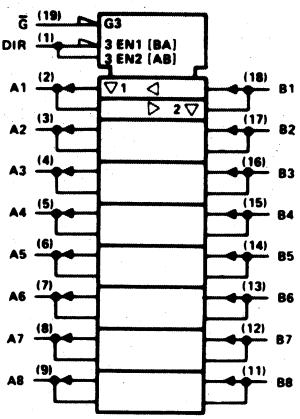
CONTROL INPUTS		OPERATION	
$\overline{G}$	DIR	'ALS1640A	'ALS1645A
L	L	$\overline{B}$ data to A bus	B data to A Bus
L	H	$\overline{A}$ data to B bus	A data to Bus
H	X	Isolation	Isolation

logic symbols†

'ALS1640A



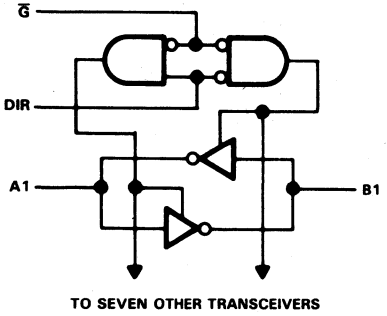
'ALS1645A



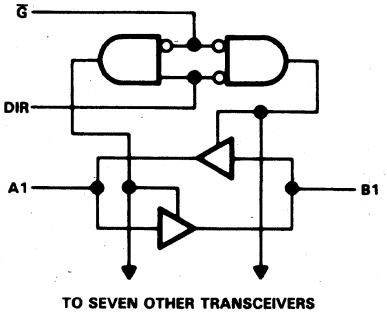
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

'ALS1640A



'ALS1645A



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN74ALS1640A, SN74ALS1645A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74ALS1640A SN74ALS1645A			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			16	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS1640A SN74ALS1645A			UNIT
				MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA				
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 16 mA		0.35	0.5	
		V_{CC} = 4.75 V,	I_{OL} = 24 mA (−1 versions)		0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	A or B ports §					20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
	A or B ports §					−0.1	
I_O†		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	'ALS1640A	V_{CC} = 5.5 V			18	32	mA
	'ALS1645A				25	36	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
† The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS1640A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			SN74ALS1640A		
			MIN	MAX	
t_{PLH}	A or B	B or A	5	15	ns
t_{PHL}			2	10	
t_{PZH}	$\overline{G}$	A or B	5	20	ns
t_{PZL}			5	22	
t_{PHZ}	$\overline{G}$	A or B	2	10	ns
t_{PLZ}			5	13	

'ALS1645A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			SN74ALS1645A		
			MIN	MAX	
t_{PLH}	A or B	B or A	2	13	ns
t_{PHL}			2	13	
t_{PZH}	$\overline{G}$	A or B	8	25	ns
t_{PZL}			8	25	
t_{PHZ}	$\overline{G}$	A or B	2	12	ns
t_{PLZ}			3	18	

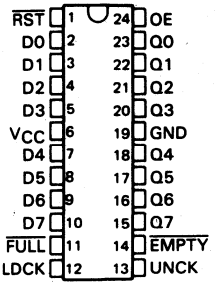
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

64 x 8 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORY

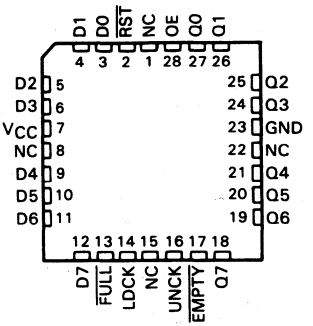
D3091, FEBRUARY 1988 – REVISED MARCH 1990

- **Independent Asynchronous Inputs and Outputs**
- **64 Words by 8 Bits**
- **Data Rates from 0 to 40 MHz**
- **Fall-Through Time . . . 20 ns Typical**
- **3-State Outputs**

NT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

This 512-bit memory uses Advanced Low-Power Schottky IMPACT-X™ technology and features high speed and fast fall-through times. It is organized as 64 words by 8 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The function is used as a buffer to couple two buses operating at different clock rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition of the load clock input (LDCK) and is read out on a low-to-high transition of the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 64 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

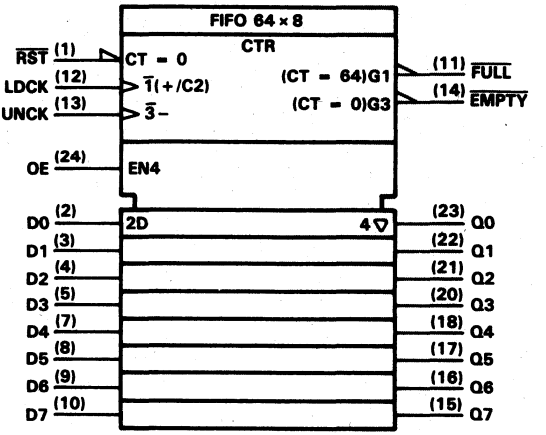
Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ output flags. The $\overline{\text{FULL}}$ output will be low when the memory is full, and high when the memory is not full. The $\overline{\text{EMPTY}}$ output will be low when the memory is empty, and high when it is not empty.

A low level on the reset input ($\overline{\text{RST}}$) resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and $\overline{\text{FULL}}$ high. The outputs are not reset to any specific logic levels. The first low-to-high transition on LDCK, either after a $\overline{\text{RST}}$ pulse or from an empty condition, causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. The first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at a high-impedance state when the output-enable input (OE) is low. The OE input does not effect either the $\overline{\text{FULL}}$ or $\overline{\text{EMPTY}}$ output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

The SN74ALS2232A is characterized for operation from 0°C to 70°C.

IMPACT–X is a trademark of Texas Instruments Incorporated.

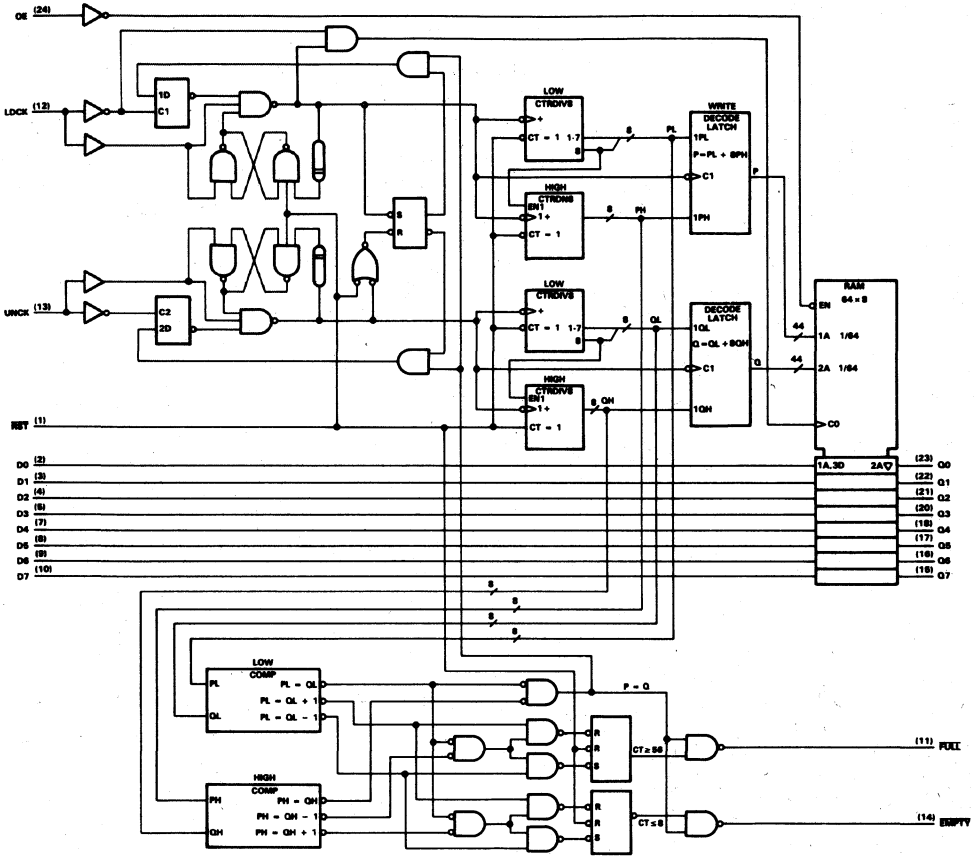
logic symbol†



†This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

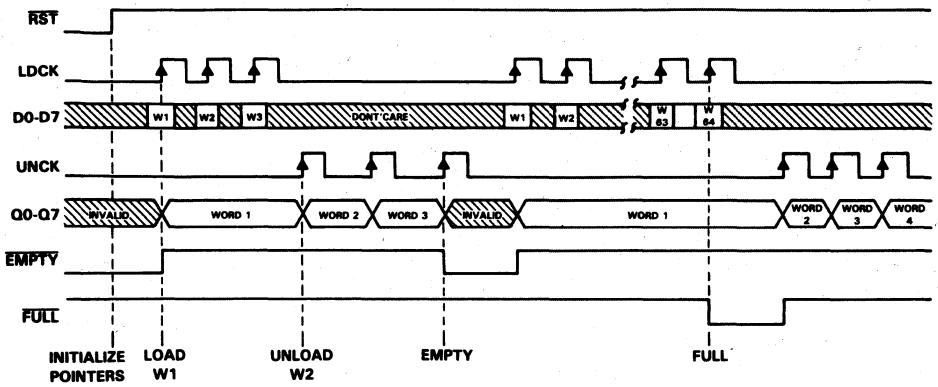
Pin numbers shown are for the NT package.

logic diagram (positive logic)



Pin numbers shown are for the NT package.

timing diagram



absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			−2.6	mA
		$\overline{FULL}$, $\overline{EMPTY}$			−0.4	
I_{OL}	Low-level output current	Q outputs			24	mA
		$\overline{FULL}$, $\overline{EMPTY}$			8	
f_{clock}	Clock frequency	LDCK, UNCK	0		40	MHz
t_w	Pulse duration	$\overline{RST}$ low	25			ns
		LDCK low	13			
		LDCK high	12			
		UNCK low	13			
		UNCK high	12			
t_{su1}	Setup time, data before LDCK↑		5			ns
t_{su2}	Setup time, $\overline{RST}$ high (inactive) before LDCK↑		5			ns
t_h	Hold time, data after LDCK↑		5			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			1.2	V
V_{OH}	$\overline{FULL}$, $\overline{EMPTY}$	V_{CC} = MIN TO MAX,	I_{OH} = 0.4 mA	V_{CC}−2			V
	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	Q outputs	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4	V
			I_{OL} = 24 mA		0.35	0.5	
	$\overline{FULL}$, $\overline{EMPTY}$		I_{OL} = 4 mA		0.25	0.4	
			I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	CLKS	V_{CC} = 5.5 V,	V_{IN} = 0.4 V			−0.2	mA
	Others					−0.1	
I_O‡	Q outputs	V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−130	mA
	$\overline{FULL}$, $\overline{EMPTY}$			−20		−112	
I_{CC}		V_{CC} = 5.5 V			175	270	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

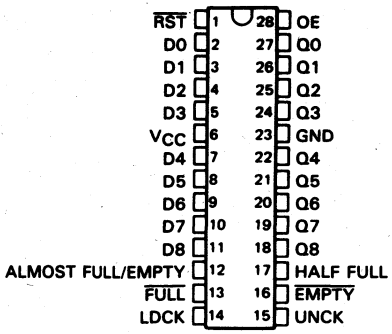
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}	LDCK					40		MHz
	UNCK					40		
t_{pd}	LDCK↑	Any Q		18	26		30	ns
t_{pd}	UNCK↑	Any Q		18	24		27	ns
t_{PLH}	LDCK↑	$\overline{EMPTY}$		12	16		18	ns
t_{PHL}	UNCK↑	$\overline{EMPTY}$		12	17		20	ns
t_{PHL}	$\overline{RST}$↓	$\overline{EMPTY}$		12	17		20	ns
t_{PHL}	LDCK↑	$\overline{FULL}$		16	21		22	ns
t_{PLH}	UNCK↑	$\overline{FULL}$		10	15		18	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL}$		13	19		23	ns
t_{en}	$\overline{OE}$↑	Q		11	15		17	ns
t_{dis}	$\overline{OE}$↓	Q		11	17		19	ns

Note 1: Load circuit and voltage waveforms are shown in Section 1.

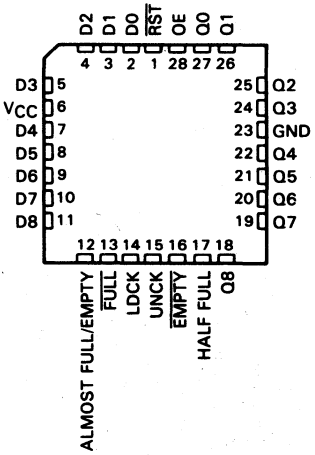
D3092, FEBRUARY 1988 – REVISED MARCH 1990

- **Independent Asynchronous Inputs and Outputs**
- **64 Words by 9 Bits**
- **Data Rates from 0 to 40 MHz**
- **Fall-Through Time . . . 20 ns Typical**
- **3-State Outputs**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

This 576-bit memory uses Advanced Low-Power Schottky IMPACT–X™ technology and features high speed and fast fall-through times. It is organized as 64 words by 9 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The function is used as a buffer to couple two buses operating at different clock rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition of the load clock input (LDCK) and is read out on a low-to-high transition of the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 64 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$, ALMOST FULL/EMPTY, and HALF FULL output flags. The $\overline{\text{FULL}}$ output will be low when the memory is full and high when the memory is not full. The $\overline{\text{EMPTY}}$ output will be low when the memory is empty and high when it is not empty. The ALMOST FULL/EMPTY flag is high when the FIFO contains eight or less words or fifty-six or more words. The ALMOST FULL/EMPTY flag is low when the FIFO contains between nine and fifty-five words. The HALF FULL flag is high when the FIFO contains thirty-two or more words, and is low when the FIFO contains thirty-one words or less.

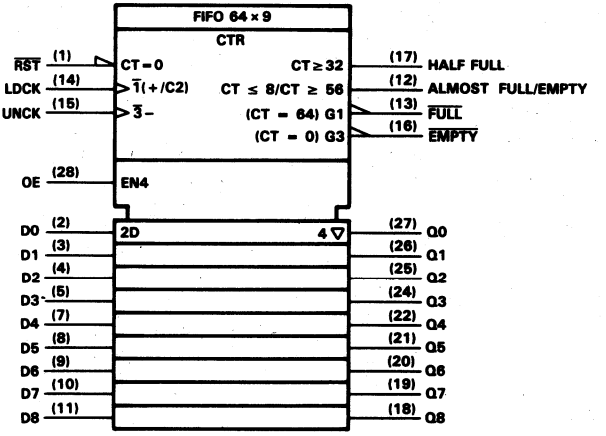
IMPACT–X is a trademark of Texas Instruments Incorporated.

description (continued)

A low level on the reset input ($\overline{RST}$) resets the internal stack control pointers and also sets EMPTY low and $\overline{FULL}$ high. The outputs are not reset to any specific logic levels. The first low-to-high transition on LDCK, either after a $\overline{RST}$ pulse or from an empty condition, causes $\overline{EMPTY}$ to go high and the data to appear on the Q outputs. The first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at a high-impedance state when the output-enable input (OE) is low. The OE input does not affect either the $\overline{FULL}$ or $\overline{EMPTY}$ output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

The SN74ALS2233A is characterized for operation from 0°C to 70°C.

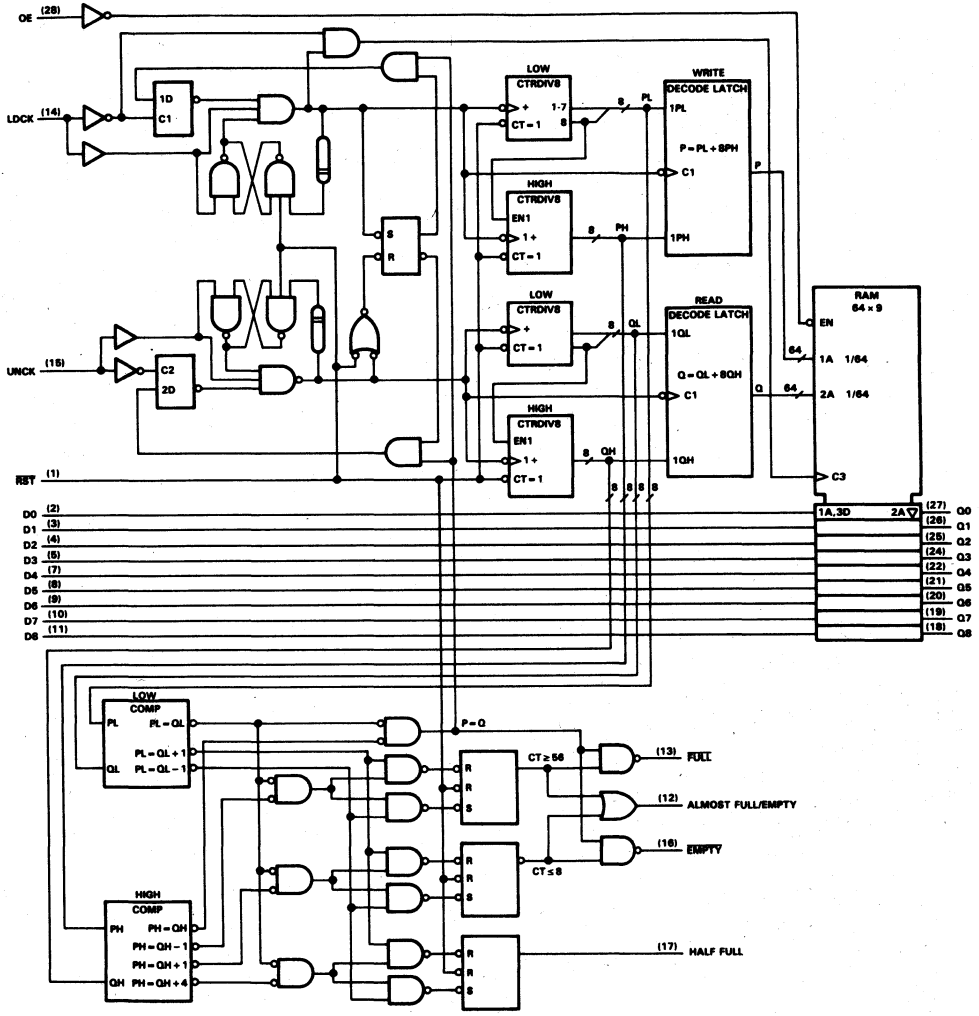
logic symbol†



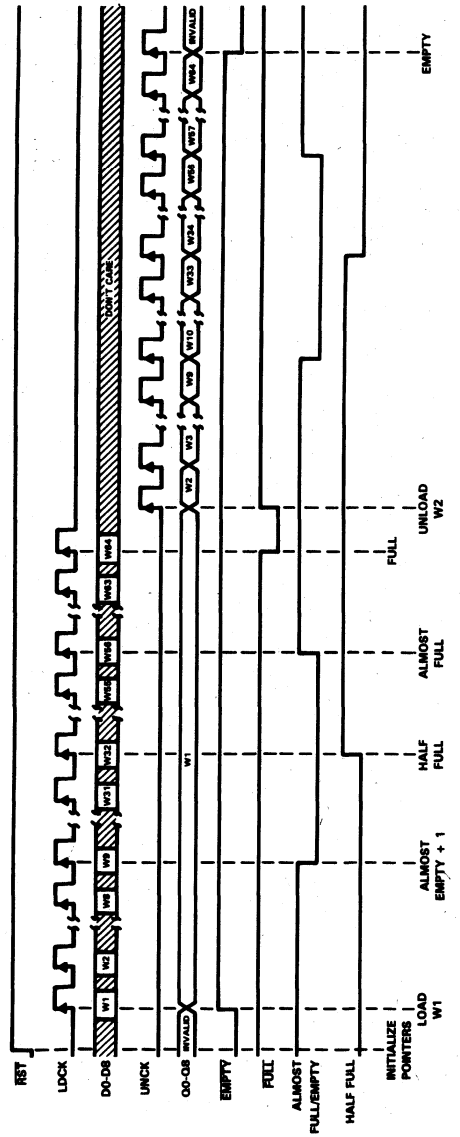
†This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

Pin numbers shown are for the N package.

logic diagram (positive logic)



timing diagram



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			−2.6	mA
		Flag outputs			−0.4	
I_{OL}	Low-level output current	Q outputs			24	mA
		Flag outputs			8	
f_{clock}	Clock frequency	LDCK, UNCK	0		40	MHz
t_w	Pusle duration	$\overline{RST}$ low	25			ns
		LDCK low	13			
		LDCK high	12			
		UNCK low	13			
		UNCK high	12			
t_{su1}	Setup time, data before LDCK↑		5			ns
t_{su2}	Setup time, $\overline{RST}$ high (inactive) before LDCK↑		5			ns
t_h	Hold time, data after LDCK↑		5			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			1.2	V
V_{OH}	Flag outputs	V_{CC} = MIN TO MAX,	I_{OH} = 0.4 mA	V_{CC}−2			V
	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	Q Outputs	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4	V
			I_{OL} = 24 mA		0.35	0.5	
	Flag outputs		I_{OL} = 4 mA		0.25	0.4	
			I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	CLKs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
	Others					−0.1	
I_O‡	Q outputs	V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−130	mA
	Flag outputs			−20		−112	
I_{CC}		V_{CC} = 5.5 V			175	290	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

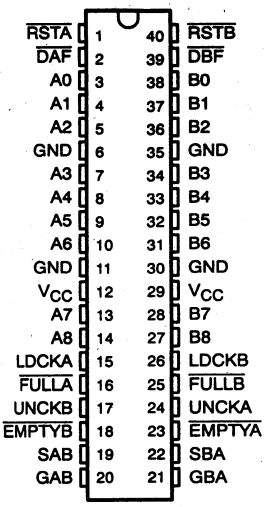
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}	LDCK					40		MHz
	UNCK					40		
t_{pd}	LDCK↑	Any Q		18	26		30	ns
t_{pd}	UNCK↑	Any Q		18	24		27	ns
t_{PLH}	LDCK↑	$\overline{EMPTY}$		12	16		18	ns
t_{PHL}	UNCK↑	$\overline{EMPTY}$		12	17		20	ns
t_{PHL}	RST↓	$\overline{EMPTY}$		12	17		20	ns
t_{PHL}	LDCK↑	$\overline{FULL}$		16	21		22	ns
t_{PLH}	UNCK↑	$\overline{FULL}$		10	15		18	ns
t_{PLH}	$\overline{RST}$↓	$\overline{FULL}$		13	19		23	ns
t_{PLH}	LDCK↑	ALMOST FULL/EMPTY		22	27		30	ns
t_{PHL}				19	25		28	
t_{PLH}	UNCK↑	ALMOST FULL/EMPTY		22	27		30	ns
t_{PHL}				17	23		26	
t_{PLH}	$\overline{RST}$↓	ALMOST FULL/EMPTY		12	16		18	
t_{PLH}	LDCK↑	HALF FULL		22	27		30	ns
t_{PHL}	$\overline{RST}$↓	HALF FULL		28	32		35	ns
t_{PHL}	UNCK↑	HALF FULL		16	22		25	ns
t_{en}	OE↑	Q		11	15		17	ns
t_{dis}	OE↓	Q		11	17		19	ns

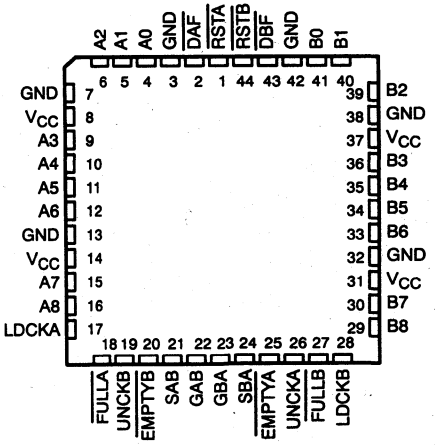
Note 1: Load circuits and voltage waveforms are shown in Section 1.

- **Independent Asychronous Inputs and Outputs**
- **Bidirectional**
- **32 Words by 9 Bits Each**
- **Programmable Depth**
- **Data Rates from 0 to 40 MHz**
- **Fall-Through Time . . . 22 ns Typ**
- **3-State Outputs**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

This 576-bit memory uses Advanced Low-Power Schottky IMPACT-X™ technology and features high speed and fast fall-through times. It consists of two FIFOs organized as 32 words by 9 bits each.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

The 'ALS2238 consists of bus transceiver circuits, two 32 X 9 FIFOs, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal FIFO memories. Enable GAB and GBA are provided to control the transceiver functions. The SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low level selects real-time data and a high selects stored data. Eight fundamental bus-management functions can be performed as shown on the Operating Modes page.

Data on the A or B data bus, or both, is written into the FIFOs on a low-to-high transition at the load clock input (LDCKA or LDCKB) and is read out on a low-to-high transition at the unload clock input (UNCKA or UNCKB). The memory is full when the number of words clocked in exceeds, by the defined depth, the number of words clocked out.

IMPACT-X is a trademark of Texas Instruments Incorporated.

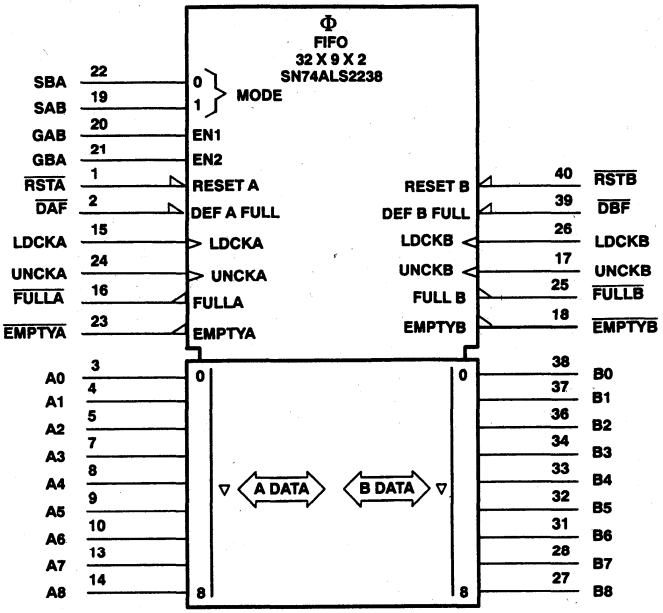
When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memories is monitored by the $\overline{\text{FULLA}}$, $\overline{\text{FULLB}}$, $\overline{\text{EMPTYA}}$, and $\overline{\text{EMPTYB}}$ output flags. The $\overline{\text{FULLA}}$ and $\overline{\text{FULLB}}$ are definable full flags. A high-to-low transition on $\overline{\text{DAF}}$ stores the binary value of A0 through A4 into a register for use as the value of X. A high-to-low transition on $\overline{\text{DBF}}$ stores the binary value of B0 through B4 into a register for use as the value of Y. In this way, the depth of either FIFO can be defined to be one to thirty-two words deep. The value of X and Y must be defined after power-up or the stored value of X and Y will be ambiguous. The $\overline{\text{FULLA}}$ and $\overline{\text{FULLB}}$ outputs will be low when their corresponding memories are full and high when the memories are not full.

The $\overline{\text{EMPTYA}}$ and $\overline{\text{EMPTYB}}$ outputs will be low when their corresponding memories are empty and high when they are not empty. The status flag outputs are always active.

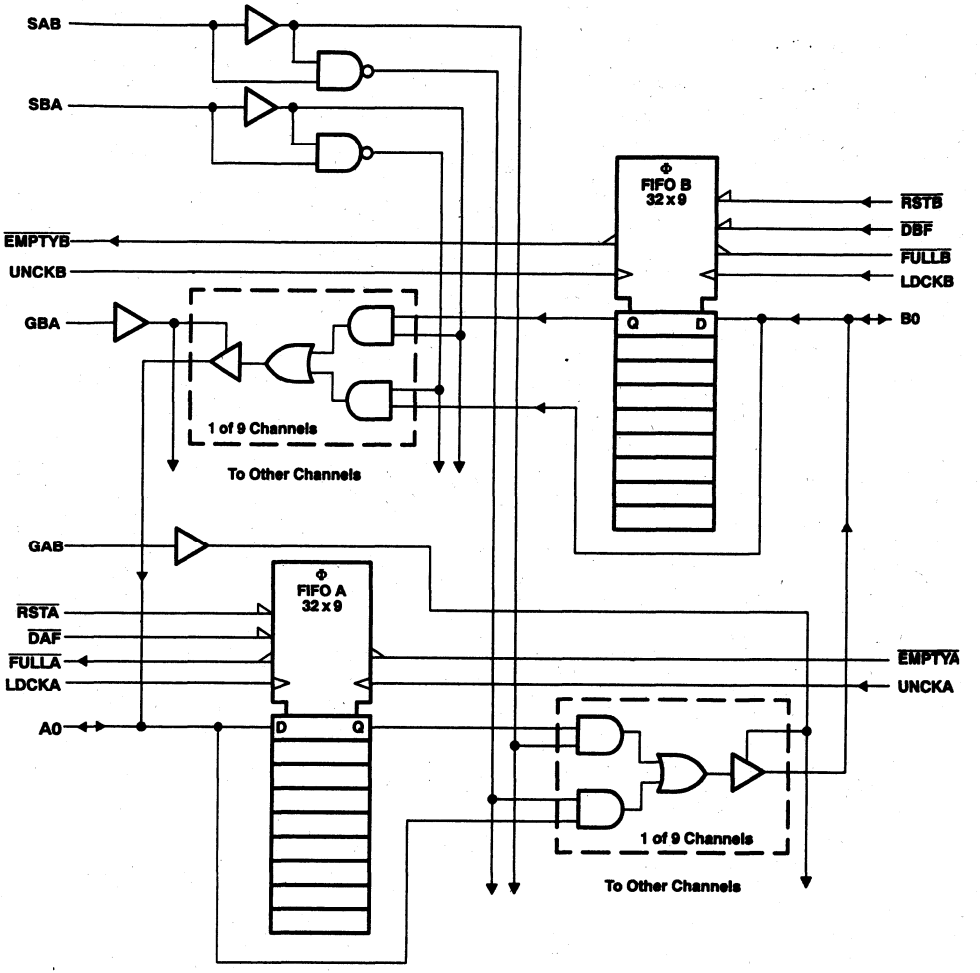
A low-level pulse on the $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$ inputs resets the control pointers on FIFO A or FIFO B and also sets $\overline{\text{EMPTYA}}$ low and $\overline{\text{FULLA}}$ high, or $\overline{\text{EMPTYB}}$ low and $\overline{\text{FULLB}}$ high. The outputs are not reset to any specific logic levels. With $\overline{\text{DAF}}$ at a low level, a low-level pulse on $\overline{\text{RSTA}}$ sets FIFO A to a depth of 32 minus X, where X is the value stored above. With $\overline{\text{DAF}}$ at a high level, a low level pulse on $\overline{\text{RSTA}}$ sets FIFO A to a depth of 32 words. The depth of FIFO B is set in a similar manner. The first low-to-high transition on LDCKA or LDCKB, either after a reset pulse or from an empty condition, will cause $\overline{\text{EMPTYA}}$ or $\overline{\text{EMPTYB}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

logic symbol†



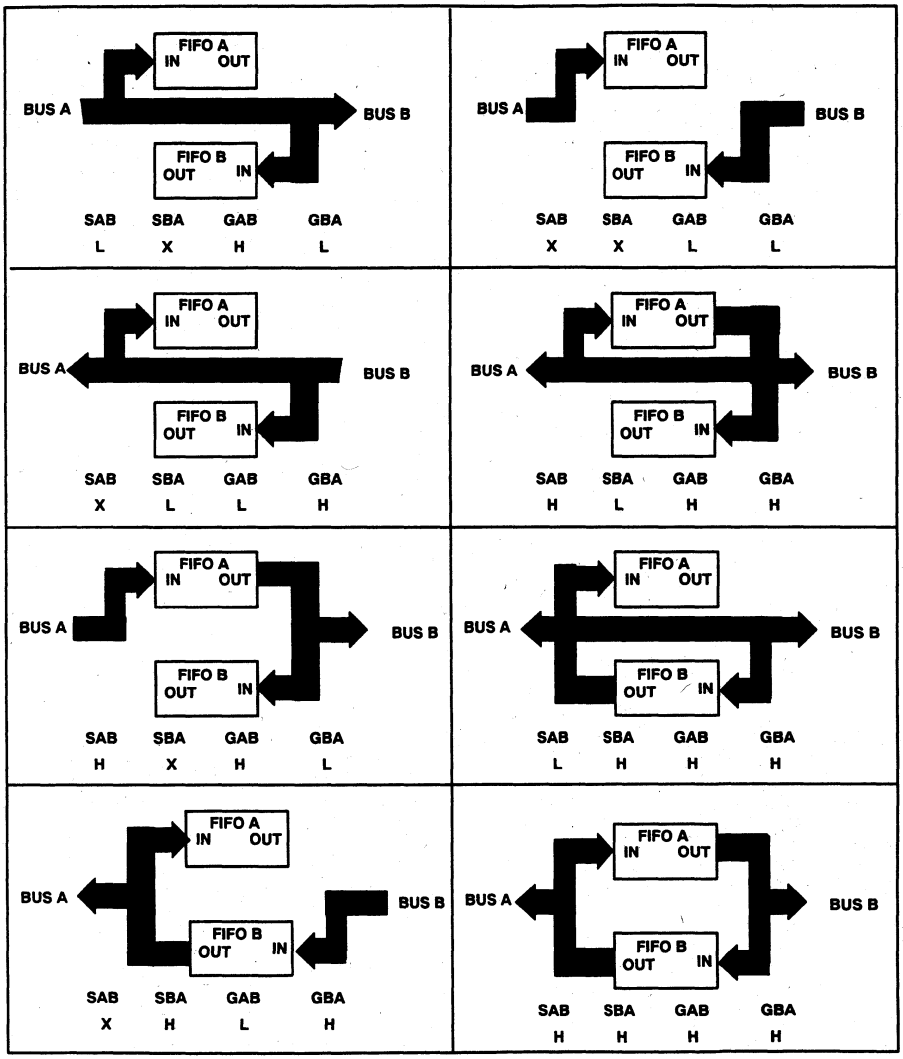
† This symbol is in accordance with ANSI/IEEE Std 91-1984.
Pin numbers shown are for the N package.

logic diagram (positive logic)

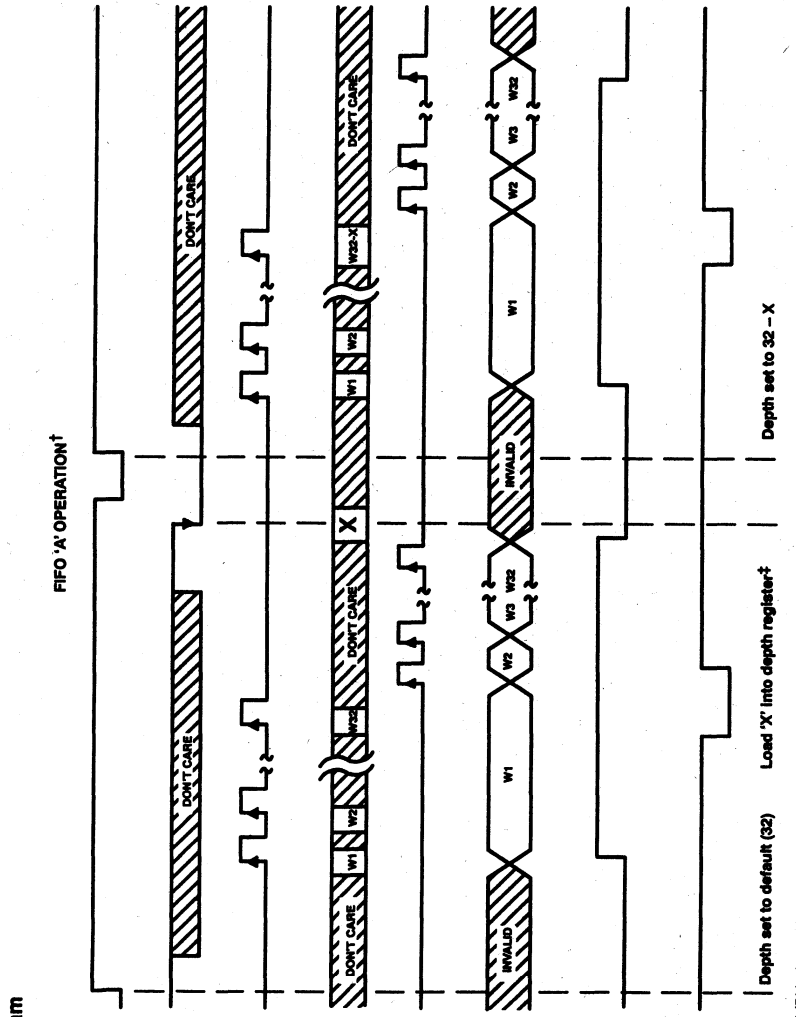


TEXAS INSTRUMENTS

operating modes



timing diagram



† Operation of FIFO 'B' is the same as shown above.
‡ 'X' includes A0 through A4 only. A5 through A8 are ignored.

TEXAS INSTRUMENTS

FUNCTION TABLES

SELECT MODE CONTROL TABLE

CONTROL		OPERATION	
SBA	SAB	A Bus	B Bus
L	L	Real Time B to A Bus	Real Time A to B Bus
H	L	FIFO B to A Bus	Real Time A to B Bus
L	H	Real Time B to A Bus	FIFO A to B Bus
H	H	FIFO B to A Bus	FIFO A to B Bus

OUTPUT ENABLE CONTROL TABLE

CONTROL		OPERATION	
GBA	GAB	A Bus	B Bus
H	H	A Bus Enabled	B Bus Enabled
H	L	A Bus Enabled	Isolation/Input to B Bus
L	H	Isolation/Input to A Bus	B Bus Enabled
L	L	Isolation/Input to A Bus	Isolation/Input to B Bus

programming procedure for depth of FIFO A†

PROGRAM:

Step 1. With $\overline{\text{RSTA}}$ at a high level, take $\overline{\text{DAF}}$ from a high level to a low level. The high-to-low transition on $\overline{\text{DAF}}$ stores the binary value of A0-A4 for use as the value of 'X' in defining the depth of FIFO A.

Step 2. With $\overline{\text{DAF}}$ held low, pulse the $\overline{\text{RSTA}}$ signal low. On the low-to-high transition of $\overline{\text{RSTA}}$, FIFO A is set to a depth of 32 minus 'X', where X is the value of A0-A4 stored above.

Step 3. To redefine the depth of FIFO A to 32 words, hold $\overline{\text{DAF}}$ at a high level and pulse the $\overline{\text{RSTA}}$ signal low.

† The programming procedures used to define the depth of FIFO B are the same as the procedure above.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} ..... – 0.5 V to 7 V
Input voltage: Control inputs ..... 7 V
I/O ports ..... 5.5 V
Voltage applied to a diabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Maximum junction temperature ..... 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	A or B Ports			−15	mA
		Status flags			−0.4	
I_{OL}	Low-level output current	A or B Ports			24	mA
		Status flags			8	
f_{clock}	Clock frequency	LDCKA or LDCKB	0		40	MHz
		UNCKA or UNCKB	0		40	
t_w	Pulse duration	$\overline{RSTA}$ or $\overline{RSTB}$ low	17			ns
		LDCKA or LDCKB low	12.5			
		LDCKA or LDCKB high	10			
		UNCKA or UNCKB low	12.5			
		UNCKA or UNCKB high	10			
		$\overline{DAF}$ or $\overline{DBF}$ high	10			
t_{su}	Setup time	Data before LDCKA or LDCKB↑	7			ns
		Define Depth: D4-D0 before $\overline{DAF}$ or $\overline{DBF}$↓	6			
		Define Depth: $\overline{DAF}$ or $\overline{DBF}$↓ before $\overline{RSTA}$ or $\overline{RSTB}$↑	45			
		Define Depth (32): $\overline{DAF}$ or $\overline{DBF}$ high before $\overline{RSTA}$ or $\overline{RSTB}$↑	32			
		LDCKA or LDCKB (inactive) before $\overline{RSTA}$ or $\overline{RSTB}$↑	5			
t_h	Hold time	Data after LDCKA or LDCKB↑	3			ns
		Define Depth: D4-D0 after $\overline{DAF}$ or $\overline{DBF}$↓	4			
		Define Depth: $\overline{DAF}$ or $\overline{DBF}$ low after $\overline{RSTA}$ or $\overline{RSTB}$↑	0			
		Define Depth (32): $\overline{DAF}$ or $\overline{DBF}$ high after $\overline{RSTA}$ or $\overline{RSTB}$↑	0			
		LDCKA or LDCKB (inactive) after $\overline{RSTA}$ or $\overline{RSTB}$↑	5			
T_A	Operating free-air temperature		0		70	°C

NOTE 1: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCKA or LDCKB and UNCKA or UNCKB clock inputs. Any excessive noise or glitching on the clock inputs (which violates the V_{IL}, V_{IH}, or minimum pulse duration limits) can cause a false clock or improper operation of the internal read and write pointers.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	Status flags	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
	A or B ports	V_{CC} = 4.5 V,	I_{OH} = −2 mA	V_{CC}−2			
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2			
V_{OL}	A or B ports	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
	Status flags	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_I	$\overline{DAF}$, $\overline{DBF}$, $\overline{RSTA}$, $\overline{RSTB}$, GAB, GBA, SAB, SBA, LDCKA, LDCKB, UNCKA, UNCKB	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
	A or B ports					0.2	
I_{IH}	$\overline{DAF}$, $\overline{DBF}$, $\overline{RSTA}$, $\overline{RSTB}$, GAB, GBA, SAB, SBA, LDCKA, LDCKB, UNCKA, UNCKB	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
	A or B ports‡					40	
I_{IL}	$\overline{DAF}$, $\overline{DBF}$, $\overline{RSTA}$, $\overline{RSTB}$, GAB, GBA, SAB, SBA, LCKA, LDCKB, UNCKA, UNCKB	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
	A or B ports‡					−0.4	
I_O§	A or B ports‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−130	mA
	Status flags			−15		−100	
I_{CC}		V_{CC} = 5.5 V			190	350	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the offstate output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output ccurrent, I_{OS}.

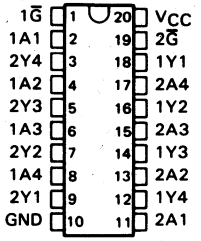
switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX			UNIT
			MIN	TYP†	MAX	
f_{max}	LDCK		40			MHz
	UNCK		40			
t_{pd}	LDCKA↑, LDCKB↑	B/A	7	22	33	ns
t_{pd}	UNCKA↑, UNCKB↑	B/A	7	20	29	ns
t_{PLH}	LDCKA↑, LDCKB↑	$\overline{EMPTYA}$, $\overline{EMPTYB}$	5	12	22	ns
t_{PHL}	UNCKA↑, UNCKB↑	$\overline{EMPTYA}$, $\overline{EMPTYB}$	5	12	22	ns
t_{PHL}	$\overline{RSTA}$↓, $\overline{RSTB}$↓	$\overline{EMPTYA}$, $\overline{EMPTYB}$	5	12	22	ns
t_{PHL}	LDCKA↑, LDCKB↑	$\overline{FULLA}$, $\overline{FULLB}$	5	12	22	ns
t_{PLH}	UNCKA↑, UNCKB↑	$\overline{FULLA}$, $\overline{FULLB}$	5	12	23	ns
t_{LH}	$\overline{RSTA}$↓, $\overline{RSTB}$↓	$\overline{FULLA}$, $\overline{FULLB}$	6	15	28	ns
t_{pd}	SAB/SBA‡	B/A	2	11	18	ns
t_{pd}	A/B	B/A	2	8	15	ns
t_{en}	GBA/GAB	A/B	2	6	15	ns
t_{dis}	GBA/GAB	A/B	1	5	12	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

- **Bidirectional Quadruple Bus Transceivers for Driving MOS Devices**
- **I/O Ports have 25 Ohm Series Resistors so No External Resistors are Required**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS2240 . . . DW OR N PACKAGE
(TOP VIEW)

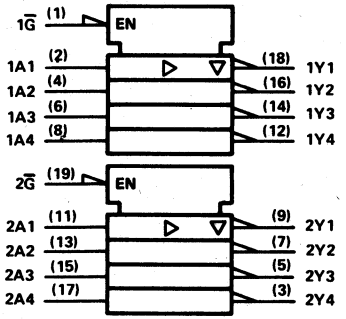


description

These octal buffers and line drivers are designed to drive the capacitive inputs of MOS devices and to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices feature high fan-out and improved fan-in.

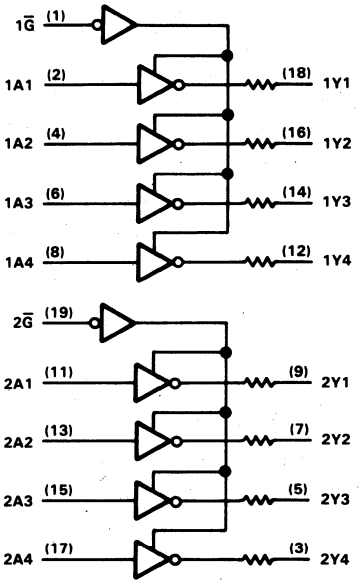
The SN74ALS2240 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN74ALS2240 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74ALS2240			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS2240			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.5	V
	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.8	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{OH}	V_{CC} = 4.5 V,	V_O = 2 V	−15			mA
I_{OL}	V_{CC} = 4.5 V,	V_O = 2 V	15			mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		6	11	mA
		Outputs low		13	23	
		Outputs disabled		12	20	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

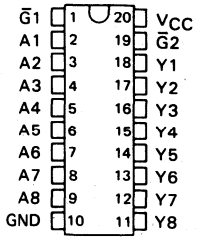
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			'ALS2240	SN74ALS2240		
			TYP	MIN	MAX	
t_{PLH}	A	Y	6	2	10	ns
t_{PHL}			6	2	10	
t_{PZH}	$\overline{G}$	Y	10	5	17	ns
t_{PZL}			12	7	20	
t_{PHZ}	$\overline{G}$	Y	7	2	10	ns
t_{PLZ}			9	4	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

JUNE 1984 – REVISED MAY 1986

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce D-C Loading**
- **Outputs have 25 Ω Series Resistor, No External Resistors are Required**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS2541 . . . DW OR N PACKAGE
(TOP VIEW)



description

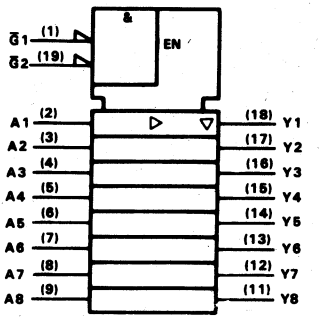
These octal buffers and line drivers are designed to drive capacitive input characteristics of MOS devices and have the performance ot the popular SN74ALS240 series. At the same time, they offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

The three-state control gate is a 2-input NOR such that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

The 'ALS2541 offers true data at the outputs.

logic symbol†

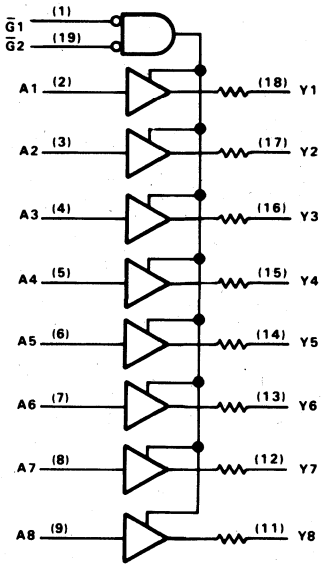
'ALS2541



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

'ALS2541



All output resistors are 25 Ω.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN74ALS2541 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74ALS2541			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−0.4	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS2541			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.5	V
	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.8	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20	µA
I_{OH}	V_{CC} = 4.5 V,	V_O = 2 V	−15			mA
I_{OL}	V_{CC} = 4.5 V,	V_O = 2 V	30			mA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		6	14	mA
		Outputs low		15	25	
		Outputs disabled		13.5	22	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS2541 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			'ALS2541	SN74ALS2541		
			TYP	MIN	MAX	
t_{PLH}	A	Y	8.7	2	15	ns
t_{PHL}			7	2	12	
t_{PZH}	$\overline{G}$	Y	9	5	15	ns
t_{PZL}			12.6	8	20	
t_{PHZ}	$\overline{G}$	Y	4	1	10	ns
t_{PLZ}			7	2	12	

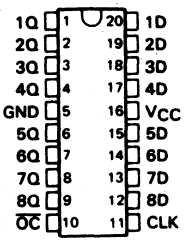
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN74AS3374
METASTABLE-RESISTANT OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D3060, FEBRUARY 1989

- **Meta-Flops™ Series — Metastable-Resistant Flip-Flops**
- **Specifically Designed for Data Synchronization Applications**
- **Improved Metastable Characteristics Provide Greater System Reliability**
- **3-State Outputs Drive Bus Lines Directly**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

The 'AS3374, a member of the Meta-Flops™ Series, is an 8-bit metastable-resistant bus interface circuit designed specifically for data synchronization applications where the normal setup and hold time specifications will frequently be violated.

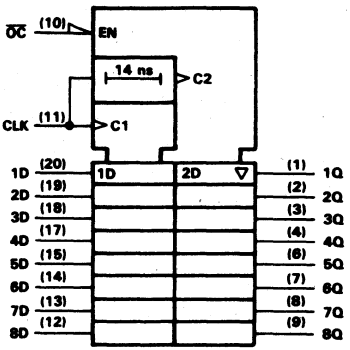
Synchronization of two digital signals operating at different frequencies is a common system dilemma. This problem is typically solved by synchronizing one of the signals to the local clock through a flip-flop. This solution, however, presents a problem. The setup and hold time specifications associated with the flip-flop's output are certain to be violated. Whenever the setup or hold times of a flip-flop are violated, its output response is uncertain. A flip-flop is metastable if its output hangs up in the region between V_{IL} and V_{IH}. The metastable state lasts until the flip-flop recovers into one of its two stable states. For conventional flip-flops, this recovery time can be longer than the specified propagation delay time.

Evaluating the metastable characteristics for a particular flip-flop is not an easy task. The number of times the output hangs up in the metastable region is extremely small compared to the total number of clock transitions.

Conventional test equipment is not designed to measure these parameters. Measuring these parameters on a production basis is impractical. Resistance to metastable failure is ensured by design only. For additional information on metastability, please refer to the application note located on page 4-51 of the *ALS/AS Logic Data Book*, 1986.

The SN74AS3374 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

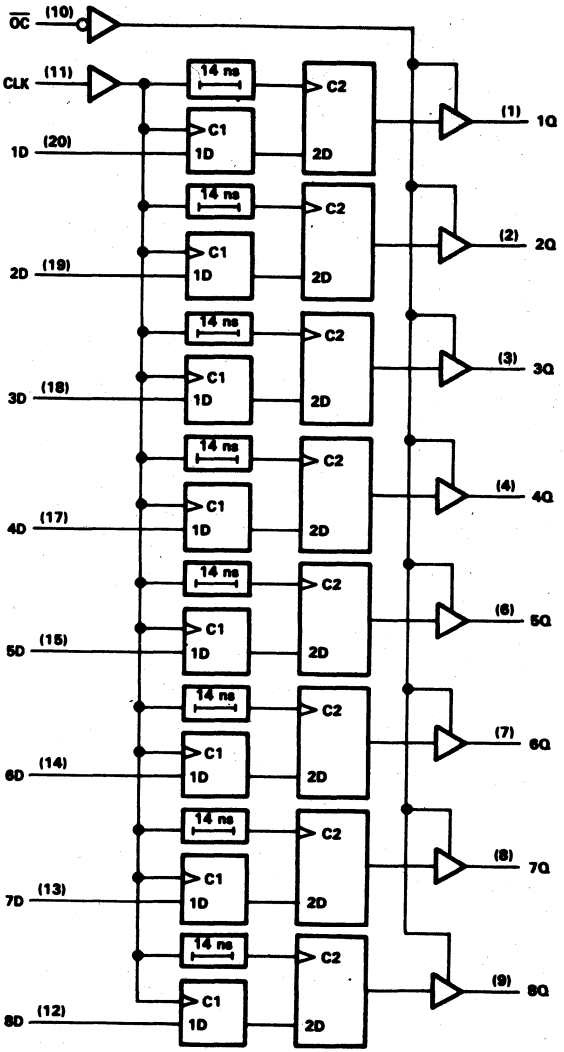
FUNCTION TABLE
(EACH DUAL-RANK FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
H	X	X	Z
L	↑	L	L
L	↑	H	H
L	L	X	Q_0

Meta-Flops is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

logic diagram (positive logic)



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−15	mA
I_{OL}	Low-level output current				48	mA
f_{clock}	Clock frequency		0		45	MHz
t_w	Pulse duration	CLK high	5			ns
		CLK low	5			
t_{su}	Setup time, data before CLK↑†		4			ns
t_h	Hold time, data after CLK↑†		2			ns
T_A	Operating free-air temperature		0		70	°C

† The data setup and hold times are specified for synchronous operation. These parameters also help guarantee overall speed characteristics of the device. Since production testing for metastability is impractical, conformance to conventional switching characteristics verifies metastable-failure resistance.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = −3 mA	2.4	3.2		V
	V_{CC} = 4.75 V,	I_{OH} = −15 mA	2			
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 32 mA		0.25	0.4	V
	V_{CC} = 4.75 V,	I_{OL} = 48 mA		0.35	0.5	
I_I	V_{CC} = 5.25 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.25 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0.4 V			−0.2	mA
I_{OZH}	V_{CC} = 5.25 V,	V_I = 2.4 V			20	μA
I_{OZL}	V_{CC} = 5.25 V,	V_O = 0.4 V			−20	μA
I_O§	V_{CC} = 5.25 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	V_{CC} = 5.25 V,	$\overline{OC}$ high		100	140	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.

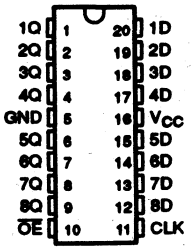
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 1)

PARAMETER	FROM	TO	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.75 V to 5.25 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}				50		45		MHz
t_{PLH}	CLK	Q		18	20	14	23	ns
t_{PHL}				18	20	14	23	
t_{PZH}	$\overline{OC}$	Q		7	9	2	11	ns
t_{PZL}				7	9	2	11	
t_{PHZ}	$\overline{OC}$	Q		5	7	1	8	ns
t_{PLZ}				5	7	1	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **3-State Outputs Drive Bus Lines Directly**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

This 8-bit flip-flop features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'AS4374B are edge-triggered D-type flip-flops. On the second positive transition of the clock (CLK) input, the Q outputs will be set to the logic levels that were set up at the data (D) inputs.

The output-enable ($\overline{OE}$) input does not affect internal operations of the flip-flops. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

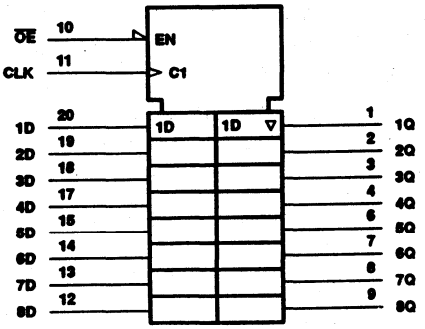
The SN74AS4374B is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D‡	Q
H	X	X	Z
L	↑	L	L
L	↑	H	H
L	L	X	Q_0

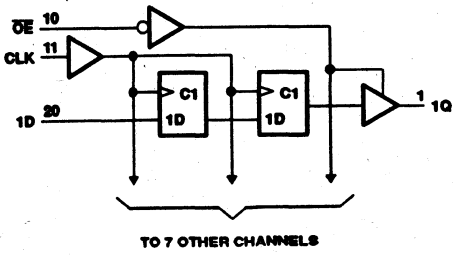
‡ Data presented at the D inputs require two clock cycles to appear at the Q outputs.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I ..... –1.2 V to 7 V
Voltage applied to any output in the high state or power-off state, V_O ..... –0.5 V to 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–15	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –3 mA	2.4	3.2		V
	V_{CC} = 4.5 V,	I_{OH} = –15 mA	2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OH} = 48 mA		0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			–20	µA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_O = 0.4 V			–0.2	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	mA
I_{CC}	V_{CC} = 5.5 V,	$\overline{OE}$ high		100	150	mA

‡ All typical values are at V_{CC} = 5 V, 25° C..
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

timing requirements over recommended operating free-air temperature range

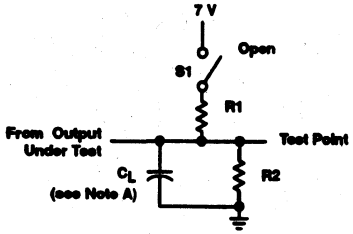
		MIN	MAX	UNIT
f_{clock}	Clock frequency	0	125	MHz
t_w	Pulse duration, CLK high or low	4		ns
t_{su}	Setup time, data before CLK ↑	4		ns
t_h	Hold time, data before CLK ↑	1		ns

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			125			125		MHz
t_{PLH}	CLK	Q		5	7.5	2	8	ns
t_{PHL}				5	7.5	2	8	
t_{PZH}	OE	Q		3.5	5	1.5	6	ns
t_{PZL}				5	6.5	2.5	8	
t_{PHZ}	OE	Q		4	5.5	2	6.5	ns
t_{PLZ}				4.5	6	2.5	7	

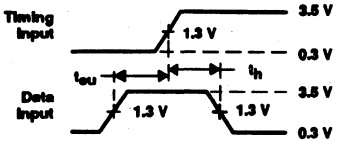
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION

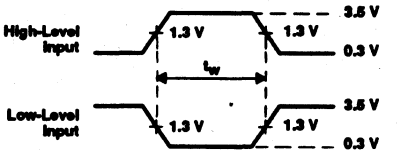


TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed

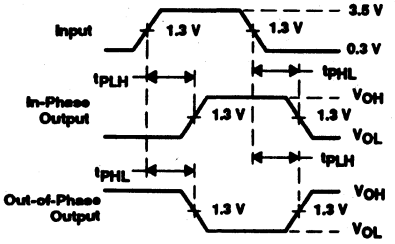
LOAD CIRCUIT FOR
3-STATE OUTPUTS



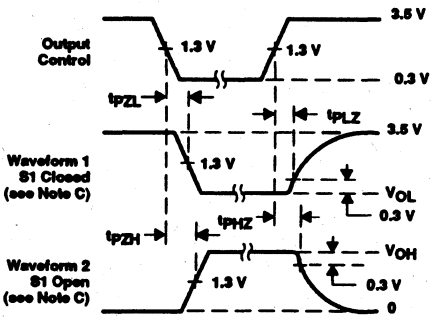
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

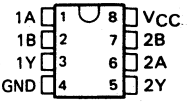
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

D2746, JULY 1983 – REVISED JULY 1987

- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS8003A . . . D OR P PACKAGE
(TOP VIEW)



description

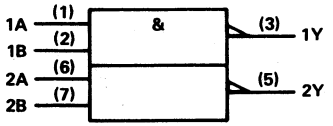
These devices contain two independent 2-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN74ALS8003A is characterized for operation from 0°C to 70°C.

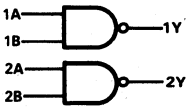
FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D and P packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN74ALS8003A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74ALS8003A			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS8003A			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.22	0.43	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.81	1.5	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX		UNIT
			SN74ALS8003A		
			MIN	MAX	
t_{PLH}	A or B	Y	3	11	ns
t_{PHL}			2	8	

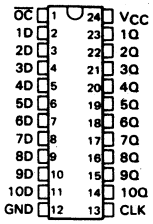
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

D2825, JANUARY 1986 – REVISED MARCH 1988

- **Functionally Equivalent to AMD AM29821 and AM29822**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity**
- **Outputs Have Undershoot Protection Circuitry**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Buffered Control Inputs to Reduce DC Loading Effects**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS29821 . . . DW OR NT PACKAGE
(TOP VIEW)



description

These 10-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

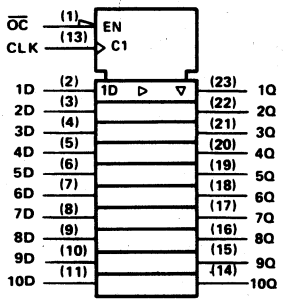
The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock the Q outputs on the 'ALS29821 will be true to the data input.

A buffered output-control ($\overline{OC}$)input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

FUNCTION TABLE (EACH FLIP-FLOP)

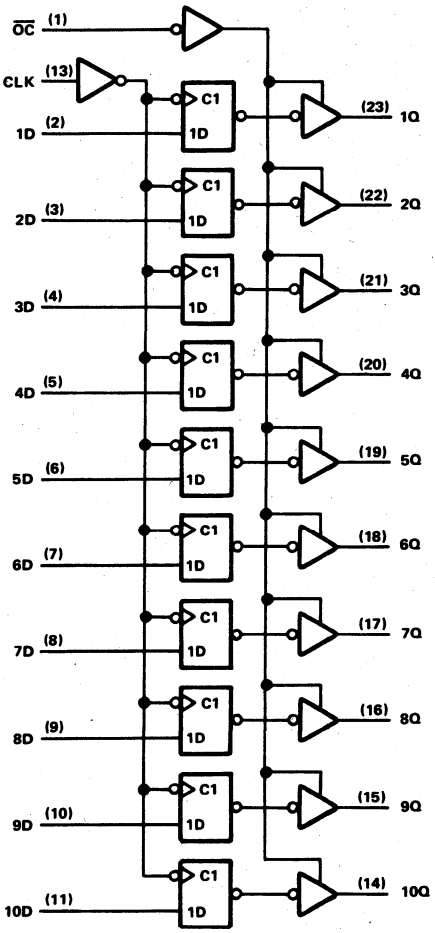
INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW and NT Packages.

logic diagram (positive logic)



Pin numbers shown are for DW and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			5		4.75	5	5.25	V
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage							0.8	V
I_{OH}	High-level output current							−24	mA
I_{OL}	Low-level output currrent							48	mA
t_w	Pulse duration	CLK high or low	5			7			ns
t_{su}	Setup time, data before CLK↑		2			4			ns
t_h	Hold time, data after CLK↑		2			2			ns
T_A	Operating free-air temperature			25		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = −15 mA	2.4	3.3		V
	V_{CC} = MIN,	I_{OH} = −24 mA	2	3.1		
V_{OL}	V_{CC} = MIN,	I_{OL} = 48 mA		0.35	0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			20	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.4 V			−20	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V			−0.2	mA
I_{OS}§	V_{CC} = MAX,	V_O = 0	−75		−250	mA
I_{CC}	V_{CC} = MAX,	Outputs open		80	115	mA

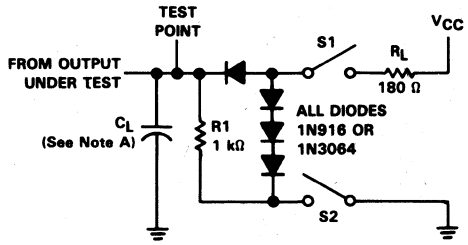
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V_{CC} = 5 V, T_A = 25°C			V_{CC} = MIN TO MAX,† T_A = MIN TO MAX†		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	C_L = 50 pF	2		8.5	2	10	ns
t_{PHL}				2		8.5	2	10	
t_{PLH}			C_L = 300 pF			14		16	
t_{PHL}						14		16	
t_{PZH}	$\overline{OC}$	Any Q	C_L = 50 pF		11.5	12		14	ns
t_{PZL}					11	12		14	
t_{PZH}			C_L = 300 pF			17		20	
t_{PZL}						21		23	
t_{PHZ}	$\overline{OC}$	Any Q	C_L = 50 pF			11		14	ns
t_{PLZ}						9		12	
t_{PHZ}			C_L = 5 pF		5.2	8		9	
t_{PLZ}					5.2	8		9	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

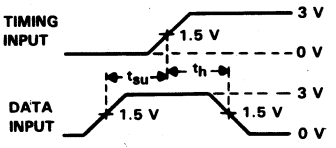
PARAMETER MEASUREMENT INFORMATION



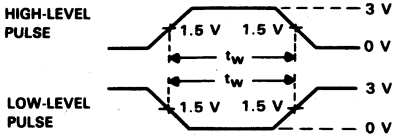
LOAD CIRCUIT

SWITCH POSITION TABLE

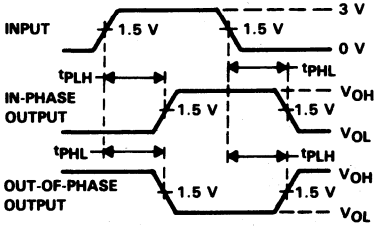
TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



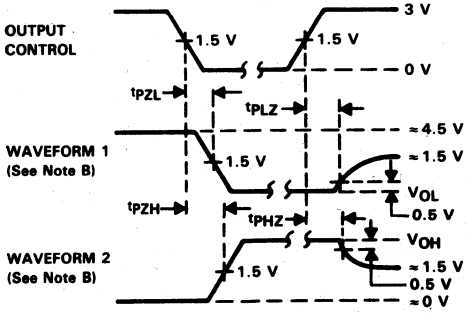
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

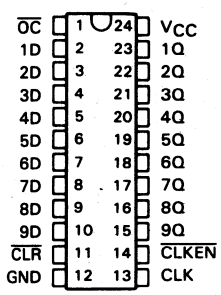
FIGURE 1

9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

D2825, JANUARY 1986 – REVISED MARCH 1990

- **Functionally Equivalent to AMD's AM29823**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity**
- **Outputs Have Undershoot Protection Circuitry**
- **Power-Up High-Impedance State**
- **Buffered Control Inputs to Reduce DC Loading Effects**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic and Ceramic 300-mil DIPs**

SN54ALS29823 . . . JT PACKAGE
SN74ALS29823 . . . DW OR NT PACKAGE
(TOP VIEW)



description

These 9-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

With the clock enable ($\overline{CLKEN}$) low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high will disabled the clock buffer, thus latching the outputs. The 'ALS29823 has noninverting D inputs. Taking the $\overline{CLR}$ input low causes the nine Q outputs to go low independently of the clock.

A buffered output-control input ($\overline{OC}$) can be used to place the nine outputs in either normal logic state (high or low level) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops.

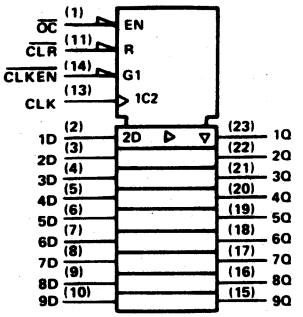
Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS29823 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS29823 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

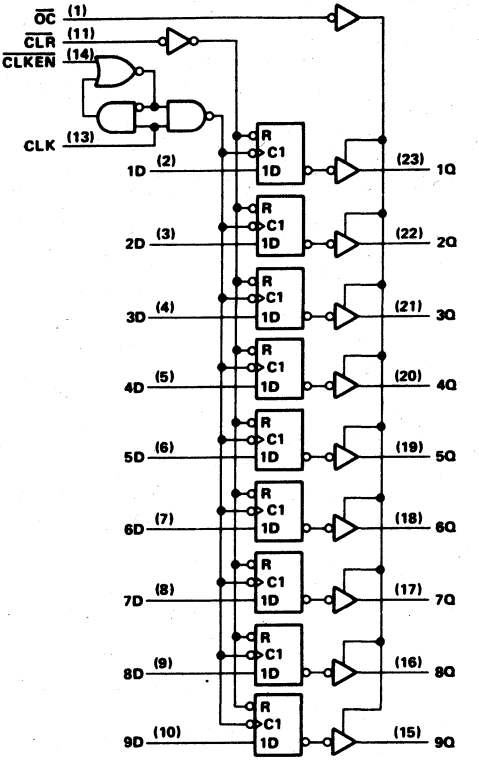
INPUTS					OUTPUT
$\overline{OC}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

logic diagram (positive logic)



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			5		4.5	5	5.5	V
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage							0.8	V
I_{OH}	High-level output current							−18	mA
I_{OL}	Low-level output current							32	mA
t_w	Pulse duration	$\overline{CLR}$ low	7			7			ns
		CLK high or low	8			8			
t_{su}	Setup time befdore CLK↑	$\overline{CLR}$ inactive	7			7			ns
		Data	4			4			
		$\overline{CLKEN}$ high or low	8			8			
t_h	Hold time	$\overline{CLKEN}$	2			2			ns
		Data	4			4			
T_A	Operating free-air temperature			25		−55		125	°C

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			5		4.75	5	5.25	V
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage							0.8	V
I_{OH}	High-level output current							−24	mA
I_{OL}	Low-level output current							48	mA
t_w	Pulse duration	$\overline{CLR}$ low	5			7			ns
		CLK high or low	5			7			
t_{su}	Setup time befdore CLK↑	$\overline{CLR}$ inactive	5			7			ns
		Data	2			4			
		$\overline{CLKEN}$ high or low	6			6			
t_h	Hold time	$\overline{CLKEN}$	0			2			ns
		Data	2			2			
T_A	Operating free-air temperature			25		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = MIN	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = −12 mA	2.4	3.3		V
	V_{CC} = MIN,	I_{OH} = −18 mA	2			
V_{OL}	V_{CC} = MIN,	I_{OL} = 32 mA		0.25	0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			50	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.4 V			−50	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V			−0.5	mA
I_{OS}§	V_{CC} = MAX,	V_O = 0 V	−75		−250	mA
I_{CC}	V_{CC} = MAX,	Outputs open		80	115	mA

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V_{CC} = 5V, T_A = 25°C			V_{CC} = MIN TO MAX†, T_A = MIN to MAX†		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	C_L = 50 pF	2		8.5	2	11.5	ns
t_{PHL}				2		8.5	2	11.5	
t_{PLH}			C_L = 300 pF	2		14	2	21	
t_{PHL}				2		17.5	2	21	
t_{PHL}	$\overline{CLR}$	Any Q	C_L = 50 pF	1	6	14.5	1	17.5	ns
t_{PZH}	$\overline{OC}$	Any Q	C_L = 50 pF	1	11.5	12	1	17	ns
t_{PZL}				1	11	12.5	1	17	
t_{PZH}			C_L = 300 pF	1		17	1	25	
t_{PZL}				1		23	1	29.5	
t_{PHZ}	$\overline{OC}$	Any Q	C_L = 50 pF	1		11	1	16	ns
t_{PLZ}				1		9	1	14	
t_{PHZ}			C_L = 5 pF	1	5.2	9	1	12	
t_{PLZ}				1	5.2	8	1	11	

† For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

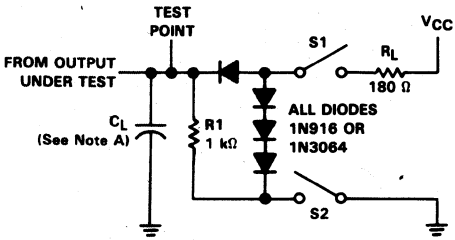
PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = MIN	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = −15 mA	2.4	3.3		V
	V_{CC} = MIN,	I_{OH} = −24 mA	2	3.1		
V_{OL}	V_{CC} = MIN,	I_{OL} = 48 mA		0.35	0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			20	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.4 V			−20	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V			−0.2	mA
I_{OS}§	V_{CC} = MAX,	V_O = 0 V	−75		−250	mA
I_{CC}	V_{CC} = MAX,	Outputs open		80	115	mA

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V_{CC} = 5V, T_A = 25°C			V_{CC} = MIN TO MAX†, T_A = MIN to MAX†		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	C_L = 50 pF	2		8.5	2	10	ns
t_{PHL}				2		8.5	2	10	
t_{PLH}			C_L = 300 pF			14		16	
t_{PHL}						14		16	
t_{PHL}	$\overline{CLR}$	Any Q	C_L = 50 pF		6	10		12	ns
t_{PZH}	$\overline{OC}$	Any Q	C_L = 50 pF		11.5	12		14	ns
t_{PZL}					11	12		14	
t_{PZH}			C_L = 300 pF			17		20	
t_{PZL}						21		23	
t_{PHZ}	$\overline{OC}$	Any Q	C_L = 50 pF			11		14	ns
t_{PLZ}						9		12	
t_{PHZ}			C_L = 5 pF		5.2	8		9	
t_{PLZ}					5.2	8		9	

† For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

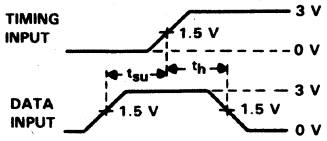
PARAMETER MEASUREMENT INFORMATION



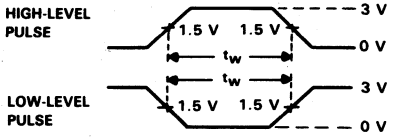
LOAD CIRCUIT

SWITCH POSITION TABLE

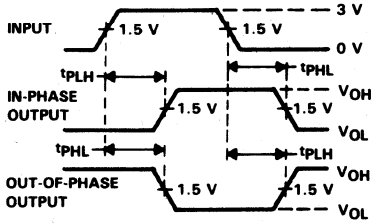
TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



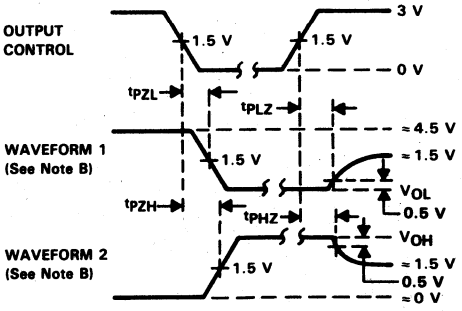
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

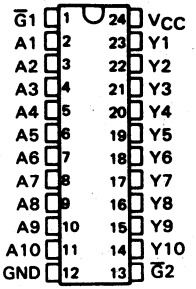
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

D2912, JANUARY 1986 – REVISED 1987

- **Functionally Equivalent to AM29827 and AM29828**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce D-C Loading**
- **Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DW OR NT PACKAGE
(TOP VIEW)



description

These 10-bit buffers and bus drivers provide high-performance bus interface for wide data paths or busses carrying parity.

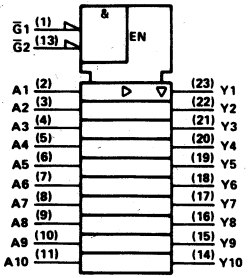
The three-state control gate is a 2-input NOR such that if either $\overline{G1}$ or $\overline{G2}$ is high, all ten outputs are in the high-impedance state.

The SN74ALS29827 provides true data and the SN74ALS29828 provides inverted data at the outputs.

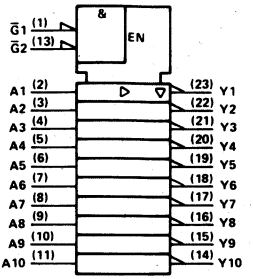
The SN74' family is characterized for operation from 0°C to 70°C.

logic symbols†

'ALS29827



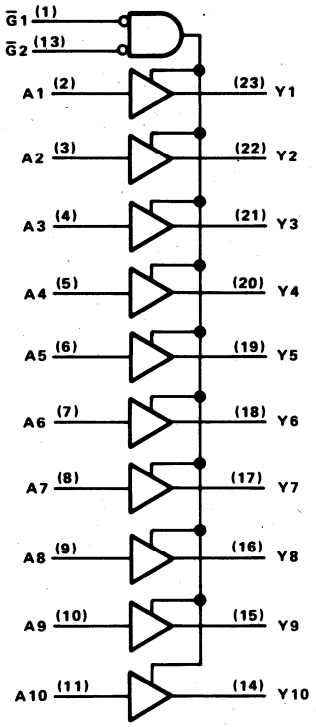
'ALS29828



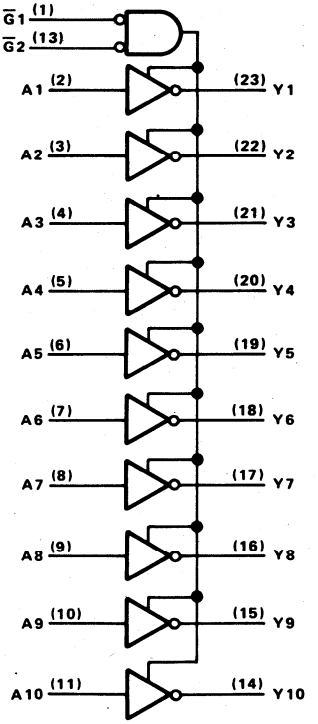
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

'ALS29827



'ALS29828



Pin numbers shown are DW and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V, I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.75 V, I_{OH} = −15 mA	2.4			V
		V_{CC} = 4.75 V, I_{OH} = −24 mA	2			
V_{OL}		V_{CC} = 4.75 V, I_{OL} = 48 mA		0.35	0.5	V
I_{OZH}		V_{CC} = 5.25 V, V_O = 2.4 V			20	μA
I_{OZL}		V_{CC} = 5.25 V, V_O = 0.4 V			−20	μA
I_I		V_{CC} = 5.25 V, V_I = 5.5 V			0.1	mA
I_{IH}		V_{CC} = 5.25 V, V_I = 2.7 V			20	μA
I_{IL}		V_{CC} = 5.25 V, V_I = 0.4 V			−0.1	mA
I_{OS}‡		V_{CC} = 5.25 V, V_O = 0 V	−75		−250	mA
I_{CC}	'ALS29827	V_{CC} = 5.25 V		25	40	mA
	'ALS29828	V_{CC} = 5.25 V		25	40	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

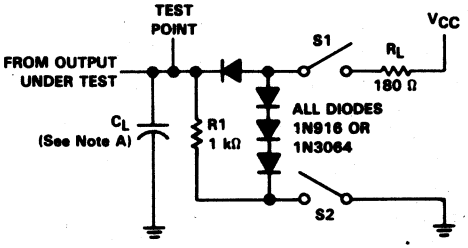
SN74ALS29827 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.75 V to 5.25 V, T_A = 0°C to 70°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 300 pF		8	11		15	ns
t_{PHL}					10.8	13.2		15	
t_{PLH}			C_L = 50 pF		4.8	6		8	
t_{PHL}					5.2	6.2		8	
t_{PZH}	$\overline{G}$	Y	C_L = 300 pF		11	17		20	ns
t_{PZL}					18	21		23	
t_{PZH}			C_L = 50 pF		6.5	12		15	
t_{PZL}					9.5	12		15	
t_{PHZ}	$\overline{G}$	Y	C_L = 50 pF		11.2	16		17	ns
t_{PLZ}					4.5	9		12	
t_{PHZ}			C_L = 5 pF		3.5	8		9	
t_{PLZ}					3.5	8		9	

SN74ALS29828 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.75 V to 5.25 V, T_A = 0°C to 70°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 300 pF		7.3	10		14	ns
t_{PHL}					8.5	12.9		14	
t_{PLH}			C_L = 50 pF		4	5.2		7	
t_{PHL}					3	5.9		7.5	
t_{PZH}	$\overline{G}$	Y	C_L = 300 pF		13	17		20	ns
t_{PZL}					16	21		23	
t_{PZH}			C_L = 50 pF		6.5	12		15	
t_{PZL}					9.5	12		15	
t_{PHZ}	$\overline{G}$	Y	C_L = 50 pF		10	16		17	ns
t_{PLZ}					4	9		12	
t_{PHZ}			C_L = 5 pF		4.5	8		9	
t_{PLZ}					4.5	8		9	

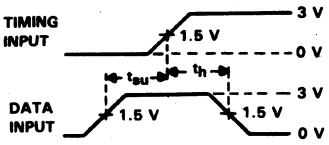
PARAMETER MEASUREMENT INFORMATION



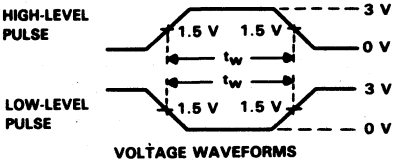
LOAD CIRCUIT

SWITCH POSITION TABLE

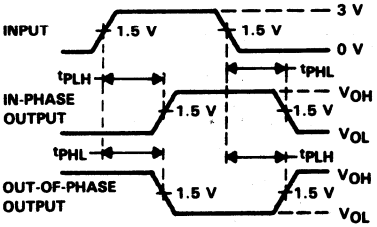
TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



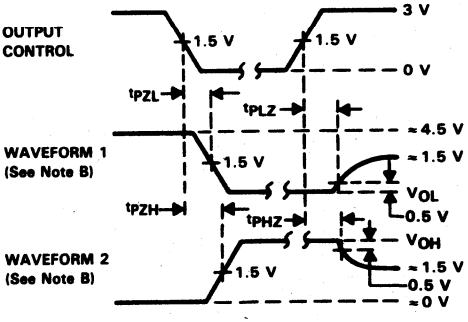
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

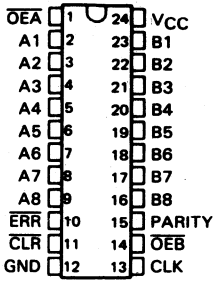
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

FIGURE 1

D2990, FEBRUARY 1987 – REVISED OCTOBER 1991

- **Functionally Similar to AMD Am29833**
- **High-Speed Bus Transceivers with Parity Generator/Checker**
- **Parity Error Flag with Open-Collector Outputs**
- **Has a Register for Storage of the Parity Error Flag**
- **Choice of True ('ALS29833) Logic**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**

SN74ALS' ... DW OR NT PACKAGE
(TOP VIEW)



description

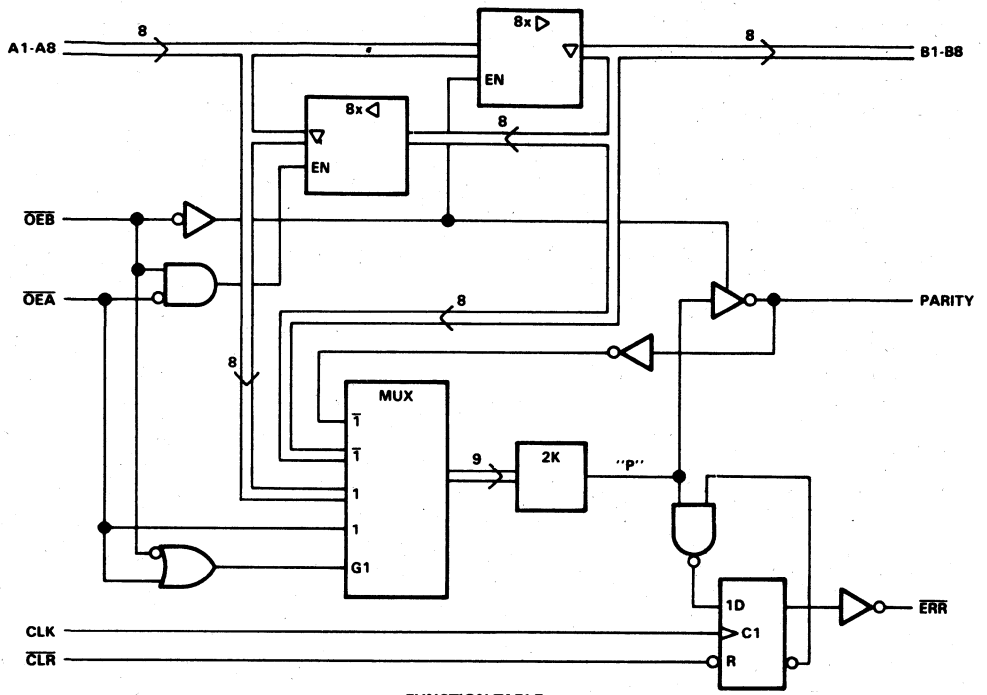
The SN74ALS29833 is a 8-bit to 9-bit parity transceiver designed for two-way communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the $\overline{ERR}$ output will indicate whether or nor an error in the B data has occurred. The output enable inputs $\overline{OEA}$ and $\overline{OEB}$ can be used to disable the device so that the buses are effectively isolated.

A 9-bit parity generator/checker generates a parity-odd output (PARITY), and monitors the parity of the I/O ports with an open-collector parity error flag ($\overline{ERR}$). $\overline{ERR}$ is clocked into the register on the rising edge of the CLK input. The error flag register is cleared with a low pulse on the $\overline{CLR}$ input. When both $\overline{OEA}$ and $\overline{OEB}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

The SN74ALS29833 is characterized for operation from 0 °C to 70 °C.

logic diagram (positive logic)

SN74ALS29833



FUNCTION TABLE

INPUTS						OUTPUT & I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	$\overline{CLK}$	Ai Σ of H's	Bi† Σ of L's	A	B	PARITY	$\overline{ERR}$*	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A Data to B Bus and Generate Parity
H	L	H	↑	NA	Odd Even	B	NA	NA	H L	B Data to A Bus and Check Parity
X	X	L	X	X	X	X	NA	NA	H	Clear Error Flag Register
H	H	H L H H	No↑ No↑ ↑ ↑	X X Odd Even	X	Z	Z	Z	NC H H L	Isolation§
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A Data to B Bus and Generate Inverted Parity

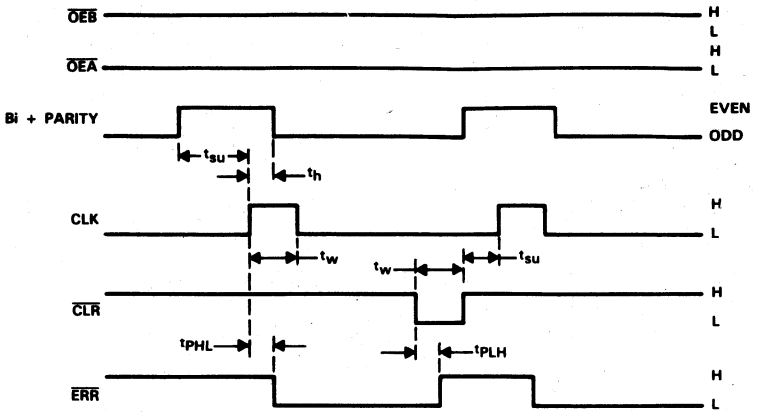
NA = Not applicable, NC = No change, X = Don't care

† Summation of high-level inputs includes PARITY along with Bi inputs.

* Output states shown assume the $\overline{ERR}$ output was previously high.

§ In this mode the $\overline{ERR}$ output, when clocked, shows inverted parity of the A bus.

error flag waveforms



ERROR FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT	FUNCTION
$\overline{CLR}$	CLK	POINT "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	
H	↑	H	H	H	SAMPLE
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	CLEAR

$\overline{ERR}_{n-1}$ represents the state of the $\overline{ERR}$ output before any changes at $\overline{CLR}$, CLK, or point "P"

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled I/O port . . . . . 5.5 V
Operating free-air temperature range . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			MIN	NOM	MAX	MIN	MAX	UNIT
V_{CC}	Supply voltage			5		4.75	5.25	V
V_{IH}	High-level input voltage					2		V
V_{IL}	Low-level input voltage						0.8	V
V_{OH}	High-level output voltage, $\overline{ERR}$						5.5	V
I_{OH}	High-level output current						−24	mA
I_{OL}	Low-level output current						48	mA
t_w	Pulse duration	CLK high				10		ns
		CLK low				10		
		$\overline{CLR}$ low				10		
t_{su}	Setup time before CLK↑	Bi and PARITY		15		17		ns
		$\overline{CLR}$ inactive				15		
t_h	Hold time, Bi and PARITY after CLK↑					0		ns
T_A	Operating free-air temperature			25		0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

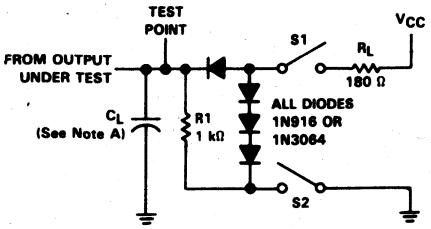
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA			1.2	V
V_{OH}	All inputs/outputs except $\overline{ERR}$	V_{CC} = 4.75 V	I_{OH} = −15 mA	2.4			V
			I_{OH} = −24 mA	2			
I_{OH}	$\overline{ERR}$	V_{CC} = 4.75 V,	V_{OH} = 5.5 V			0.1	mA
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 48 mA		0.35	0.5	V
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V			0.1	mA
I_{IH}*		V_{CC} = 5.25 V,	V_I = 2.7 V			20	μA
I_{IL}*	Data	V_{CC} = 5.25 V,	V_I = 0.4 V			−0.2	mA
	Control					−0.75	
I_{OS}§		V_{CC} = 5.25 V,	V_O = 0 V	−75		−250	mA
I_{CC}		V_{CC} = 5.25 V			70	100	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
* For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics (see Figure 1)

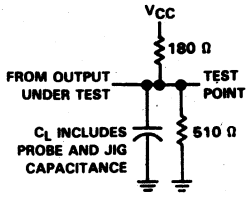
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 5 V, T_A = 25 °C			V_{CC} = 4.75 V to 5.25 V, T_A = MIN to MAX		UNIT
				MIN	TYP	MAX	MIN	MAX	
tPLH	A or B	B or A	C_L = 50 pF		4	6		8	ns
tPHL					4	6		8	
tPLH			C_L = 300 pF		9	12		15	
tPHL					9	12		15	
tPLH	A	PARITY	C_L = 50 pF		10	13		15	ns
tPHL					12	15		19	
tPLH			C_L = 300 pF		12	16		22	
tPHL					16	20		24	
tPZH	$\overline{OEA}$ or $\overline{OEB}$	A or B	C_L = 50 pF		10	13		17	ns
tPZL					10	13		17	
tPZH			C_L = 300 pF		15	20		23	
tPZL					15	20		23	
tPHZ	$\overline{OEA}$ or $\overline{OEB}$	A or B	C_L = 5 pF		4	6		9	ns
tPLZ					4	6		9	
tPHZ			C_L = 50 pF		10	15		15	
tPLZ					4	6		8	
tPHL	CLK	$\overline{ERR}$	C_L = 50 pF		7	11		13	ns
tPLH	$\overline{CLR}$	$\overline{ERR}$	C_L = 50 pF		7	11		13	ns
tPLH	$\overline{OEA}$	PARITY	C_L = 50 pF		11	15		17	ns
tPHL					11	15		19	
tPLH			C_L = 300 pF		14	18		22	
tPHL					15	20		25	

PARAMETER MEASUREMENT INFORMATION



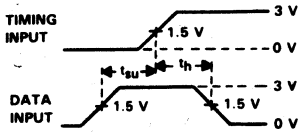
SWITCH POSITION TABLE

TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closes
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

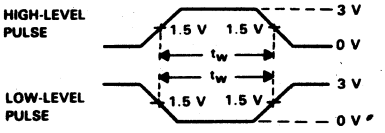


LOAD CIRCUIT 1 ALL OUTPUTS EXCEPT FOR ERROR FLAG

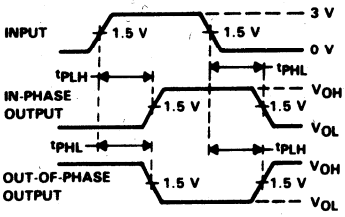
LOAD CIRCUIT 2 ERROR FLAG OUTPUT



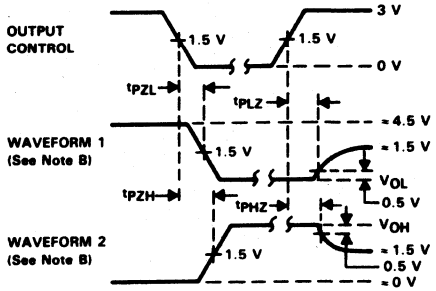
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

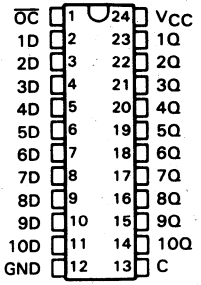
FIGURE 1

10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D3078, JUNE 1988 – REVISED MARCH 1990

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Provide Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity**
- **Buffered Control Inputs to Reduce DC Loading**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**

SN74ALS29841 . . . DW OR NT PACKAGE
(TOP VIEW)



description

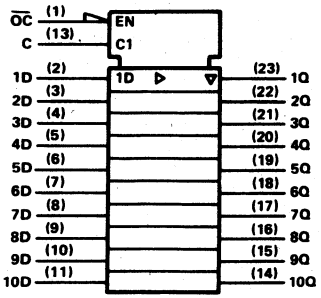
These 10-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type. The 'ALS29841 has noninverting data (D) inputs.

A buffered output control ($\overline{OC}$) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

logic symbol†

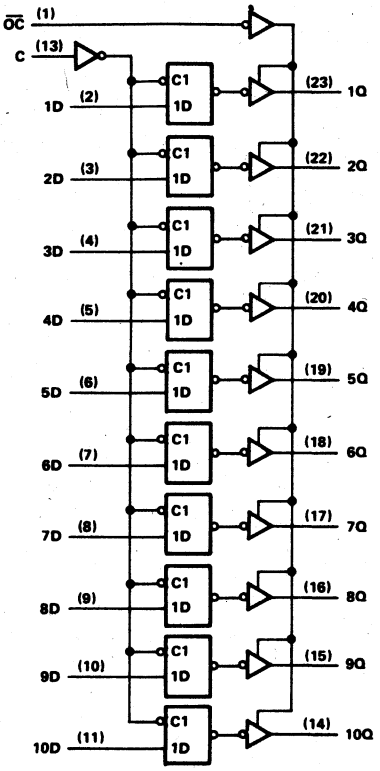


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		5		4.75	5	5.25	V
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
I_{OH}	High-level output current						−24	mA
I_{OL}	Low-level output current						48	mA
t_w	Pulse duration, enable C high	4			6			ns
t_{su}	Setup time, data before enable C↓	2.5			2.5			ns
t_h	Hold time, data after enable C↓	4.5			4.5			ns
T_A	Operating free-air temperature		25		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = −15 mA	2.4	3.3		V
	V_{CC} = MIN	I_{OH} = −24 mA	2	3.1		
V_{OL}	V_{CC} = MIN,	I_{OL} = 48 mA		0.35	0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.4			−20	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V			−0.2	mA
I_{OS}§	V_{CC} = MAX,	V_O = 0	−75		−250	mA
I_{CC}	V_{CC} = MAX,	Outputs low		55	85	mA

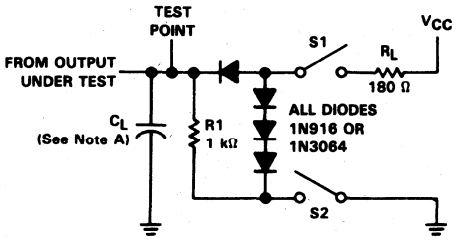
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 5 V, T_A = 25°C			V_{CC} = MIN TO MAX,† T_A = MIN TO MAX†		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	Any Q	C_L = 50 pF	2	5.7	8	2	9.5	ns
t_{PHL}				2	6.2	8	2	9.5	
t_{PLH}			C_L = 300 pF		10	12.5		14	
t_{PHL}					10	14		14	
t_{PLH}	C	Any Q	C_L = 50 pF		8	10.5		12	ns
t_{PHL}					7.5	10		12	
t_{PLH}			C_L = 300 pF			15		16	
t_{PHL}						15		16	
t_{PZH}	$\overline{OC}$	Any Q	C_L = 50 pF		7.3	12		14	ns
t_{PZL}					9.7	12		14	
t_{PZH}			C_L = 300 pF			17		20	
t_{PZL}						21		23	
t_{PHZ}	$\overline{OC}$	Any Q	C_L = 50 pF		10.4	14		15	ns
t_{PLZ}					4.7	11		12	
t_{PHZ}			C_L = 5 pF		3.4	8		9	
t_{PLZ}					3.8	8		9	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

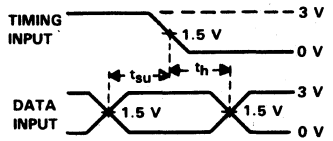
PARAMETER MEASUREMENT INFORMATION



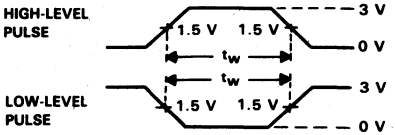
LOAD CIRCUIT

SWITCH POSITION TABLE

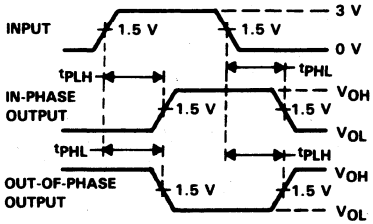
TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



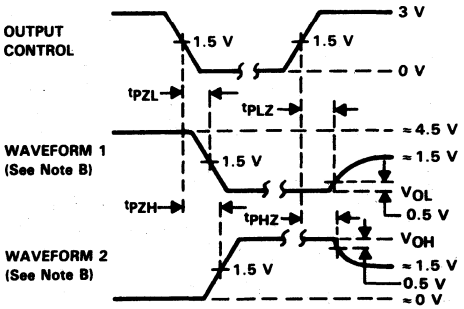
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

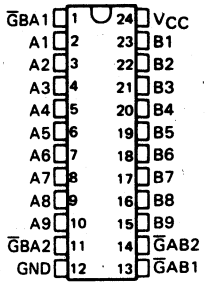
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

D2915, JANUARY 1986 – REVISED AUGUST 1988

- **Functionally Equivalent to Am29863**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DW OR NT PACKAGE
(TOP VIEW)



description

The 9-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}BA1$, $\overline{G}BA2$, $\overline{G}AB1$, and $\overline{G}AB2$).

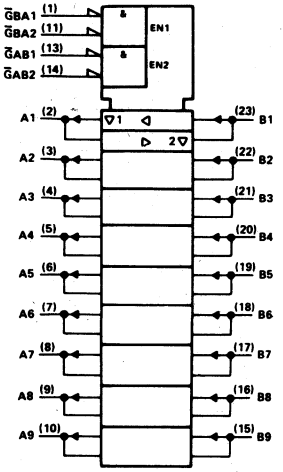
The SN74' family is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

ENABLE INPUTS				OPERATION
$\overline{G}AB1$	$\overline{G}AB2$	$\overline{G}BA1$	$\overline{G}BA2$	'ALS29863
L	L	L	L	Latch A and B
L	L	H	X	A to B
L	L	X	H	
H	X	L	L	B to A
X	H	L	L	
H	X	H	X	Isolation
H	X	X	H	
X	H	X	H	
X	H	H	X	

logic symbol†

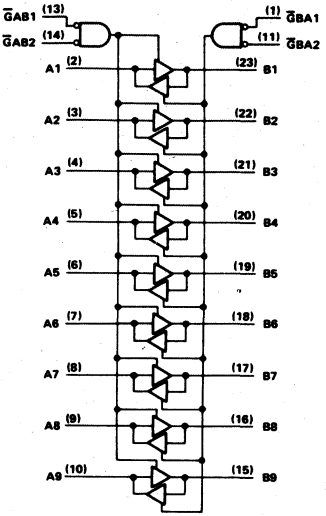
'ALS29863



† Theses symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram

'ALS29863



Pin numbers are for DW and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 5.5 V
Operating free-air temperature range . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted

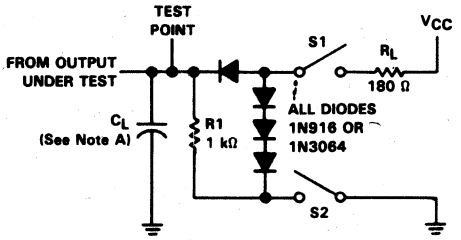
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.75 V,	O_{OH} = −15 mA	2.4			V
		V_{CC} = 4.75 V,	I_{OH} = −24 mA	2			
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 48 mA		0.35	0.5	V
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V			0.1	mA
I_{IH}	Control inputs	V_{CC} = 5.25 V,	V_I = 2.7 V			20	µA
	A or B ports*					20	
I_{IL}	Control Inputs	V_{CC} = 5.25 V,	V_I = 0.4 V			−0.1	mA
	A or B ports*					−0.1	
I_O§		V_{CC} = 5.25 V,	V_O = 0 V	−75		−250	mA
I_{CC}		V_{CC} = 5.25 V			40	65	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
* For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

SN74ALS29863 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V_{CC} = 5 V, T_A = 25 °C			V_{CC} = 4.75 V to 5.25 V, T_A = 0 °C to 70 °C		UNIT
				MIN	TYP	MAX	MIN	MAX	
tPLH	A or B	B or A	C_L = 300 pF		8	11		15	ns
tPHL					11	14		15	
tPLH			C_L = 50 pF		4.8	6		8	
tPHL					5.2	6.2		8	
tPZH	$\overline{G}$AB or $\overline{G}$BA	A or B	C_L = 300 pF		11	17		20	ns
tPZL					17	21		23	
tPZH			C_L = 50 pF		6.5	12		15	
tPZL					9.5	12		15	
tPHZ	$\overline{G}$AB or $\overline{G}$BA	A or B	C_L = 50 pF		10	16		17	ns
tPLZ					4.5	9		12	
tPHZ			C_L = 5 pF		3.5	8		9	
tPLZ					3.5	8		9	

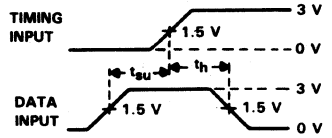
PARAMETER MEASUREMENT INFORMATION



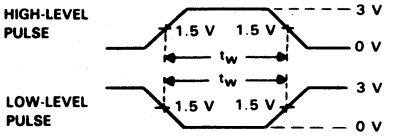
LOAD CIRCUIT

SWITCH POSITION TABLE

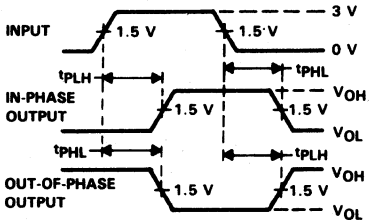
TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closes
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

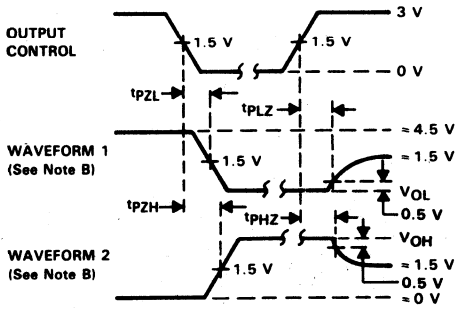


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FIGURE 1

1

2

Application Reports 3

4

Advanced Schottky Family

TEXAS INSTRUMENTS

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Advanced Schottky Family (ALS/AS) Application

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List of Illustrations

List of Illustrations (Continued)

List of Tables

INTRODUCTION

The purpose of this Application Report is to assist the designers of high-performance digital logic systems in the use of the new series of Advanced Schottky-clamped* TTL integrated circuits.

Detailed electrical characteristics of these devices are provided and, if available, tables have been included that compare specific parameters of the devices with those of other logic families. In addition, interfamily information is provided to allow system designers to mix logic families in the same circuit. This allows the designer to use the relative merits of each logic family in high preformance state-of-the-art designs.

The major subject areas covered in this Application Report are as follows:

- Advanced Schottky process
- Fanouts
- Transfer characteristics
- Input and output parameters
- Speed and power information
- Noise margins
- Power supply considerations
- Noise sources and their abatement
- Back panel and printed circuit wiring guidelines
- Line driving and receiving

INTRODUCTION TO ADVANCED SCHOTTKY-CLAMPED TTL

Series 54/74 transistor-transistor logic (TTL) has, since its introduction in 1965, become the most popular digital integrated circuit logic family ever offered. Its popularity has allowed the development of high-volume production techniques which have made it the most economical approach to the implementation of major portions of medium-to-high performance digital logic systems. These systems range from simple decision making to highly complex real-time computer installations that handle worldwide data processing.

The proliferation of and economical impact of these digital logic systems has created a demand for constant improvement in efficiency. In response to demand, Texas Instruments examined the advantages gained by Schottky clamping. An increase in speed and performance was discovered in the use of Schottky barrier-diode clamping. The process was patented in the United States and the Schottky series 54S/74S catalog parts were made available in the early 1970s. A series 54LS/74LS was introduced later. The series 54LS/74LS was slower that the 54S/74S series but had a much lower power consumption.

*Integrated Schottky-Barrier-diode-clamped transistor is patented by Texas Instruments Incorporated, U.S. Patent Number 3,463,975.

Recent innovations in integrated circuit design have made it possible to develop two new families: the Advanced Schottky (54AS/74AS) series and the Advanced Low-Power Schottky (54ALS/74ALS) series. The 'ALS and 'AS series provide considerable higher speeds than the 'LS and 'S series, respectively. The 'ALS series offers a substantial reduction in power consumption over the 'LS series, and the 'AS series offers a substantial reduction in power consumption over the 'S series. The 'ALS/'AS series is pin-to-pin compatible with the 'LS/'S series.

SPEED-POWER SLOTS FILLED BY 'ALS AND 'AS TTL

Digital integrated circuits have historically been characterized for both speed and power. The series 54S/74S devices contain 19 mW NAND gates and 125-MHz flip-flops and the series 54LS/74LS devices contain 2-mW NAND gates and 45-MHz flip-flops. Either of these logic families could be used to design a 2-MHz system, therefore categorization strictly on the basis of power and speed is inconclusive with respect to system efficiency. To provide a means of measuring the overall circuit efficiency and performance, a speed-power product efficiency index for integrated circuits was developed. The rating of an integrated circuit is obtained by multiplying the gate propagation delay by the gate power dissipation.

Table 1 provides propagation delay times, power dissipation, and speed-power product for the Texas Instruments TTL series. In addition, it provides flip-flop frequency for each family as an indicator of system performance. The speed-power product rating system (measured in picojoules) is divided into circuits where speed is the prime factor and circuits where low-power is the prime factor. The 'ALS series speed-power product is approximately 4 times less than that of the 'LS series and the 'AS series speed-power product is approximately 4 times less than the 'S series. Figure 1 is a graphic analysis of the speed-power points for the various TTL families.

ADDITIONAL ADVANTAGES OFFERED BY 'ALS AND 'AS DEVICES

The 'ALS and 'AS devices offer the following additional advantages:

1. TTL compatible with 54/74, 54S/74S, 54L/74L, 54LS/74LS, and 54H/74H series gates for selectively upgrading existing systems
2. Suppresses the effects of line ringing and significantly reduces undershoot
3. Higher thresholds (noise immunity) and better stability across operating free-air temperature range
4. Input current requirement reduced by up to 50%

Table 1. Typical Performance Characteristics by TTL Series

CIRCUIT TECHNOLOGY	MINIMIZING POWER					MINIMIZING DELAY TIME				
	FAMILY	PROP DELAY (ns)	PWR DISS (mW)	SPD/PWR PRODUCT (pJ)	MAXIMUM FLIP-FLOP FREQ (MHz)	FAMILY	PROP DELAY (ns)	PWR DISS (mW)	SPD/PWR PRODUCT (pJ)	MAXIMUM FLIP-FLOP FREQ (MHz)
Gold Doped	TTL	10	10	100	35	TTL	10	10	100	35
	L TTL	33	1	33	3	H TTL	6	22	132	50
Schottky Clamped	LS TTL	9	2	18	45	S TTL	3	19	57	125
	'ALS	4	1.2	4.8	70	'AS	1.7	8	13.6	200

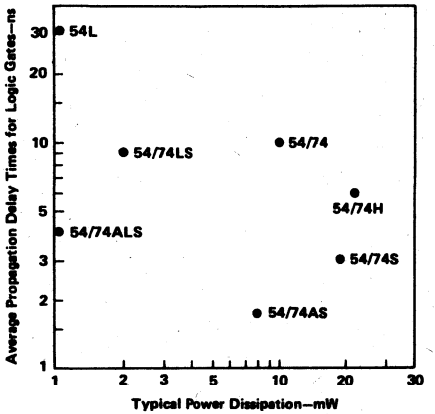


Figure 1. Speed-Power Relationships of Digital Integrated Circuits

5. Fanout is doubled
6. Terminated lines or controlled impedance circuit boards are normally not required.
7. The 'AS series offers shorter propagation delays and higher clock frequencies with relatively low power consumption.
8. The maximum flip-flop frequency has been increased to 200 MHz.

CONCEPTS OF DEFINING SERIES 'AS AND 'ALS

Both the 'ALS and 'AS series are electrically and pinout compatible with existing TTL series. The 'ALS series is suitable for replacing all TTL families except in the very highest frequency applications. Replacement with 'ALS will result in lower power consumption, smaller power supply current spikes, and, in some cases, better noise immunity than the other families. In those cases where a very high operating frequency is required, the 'AS series can be used. The 'AS devices require less than one-half of the supply current of the 'S series and has approximately twice the clocking frequency. The 'ALS devices are ideal for improving effeciency at the lower speeds. The 'AS devices are ideal for replacement of high-speed logic families including ECL 10K series.

Compatibility With Other TTL Families

To ensure complete electrical compatibility in systems using or intending to use a mixture of existing TTL families and the new 'ALS/'AS families, specific guidelines have been implemented. These guidelines ensure the continuation of desirable characteristics and incorporate newer techniques to improve performance and/or simplify the use of TTL families. Figure 2 illustrates the comparison of essential parameters of each family and shows that complete compatibility is maintained throughout the 54/74 families.

Fanout

The compatible ratings for fanout simplify the implementation of logic and provide a freedom of choice in the use of any of the seven performance ranges to design a digital logic system. Any of the Texas Instruments TTL series gates can be used to drive any other gate without the use of an interface or level-shifting circuit. The use of totem-pole-(push-pull) type output stages provides a low output impedance and the capability for both sourcing and sinking current. The output is easily adapted for driving MOS and CMOS circuits as well as the interface circuits between the output and the devices it controls. Figure 3 illustrates fanout capability.

USING THE SCHOTTKY BARRIER DIODE

The Advanced Schottky Family has been developed from two earlier concepts: the Baker Clamp and the Schottky Barrier-Diode (SBD). The use of the Baker Clamp and SBD concepts resulted in the Schottky Clamped Transistor. The Schottky clamped transistor produced the increased switching speed associated with the S series integrated circuits. The additional advances that have led to the development of 'ALS and 'AS gates and the actual gates are discussed later.

Analysis of the Schottky Clamped Transistor

The use of the Baker Clamp, shown in Figure 4, is a method of avoiding saturation of a discrete transistor. The diode forward voltage is 0.3 V to 0.4 V as compared to 0.7 V for the base-emitter junction diode. When the transistor is turned on, base current drives the transistor toward

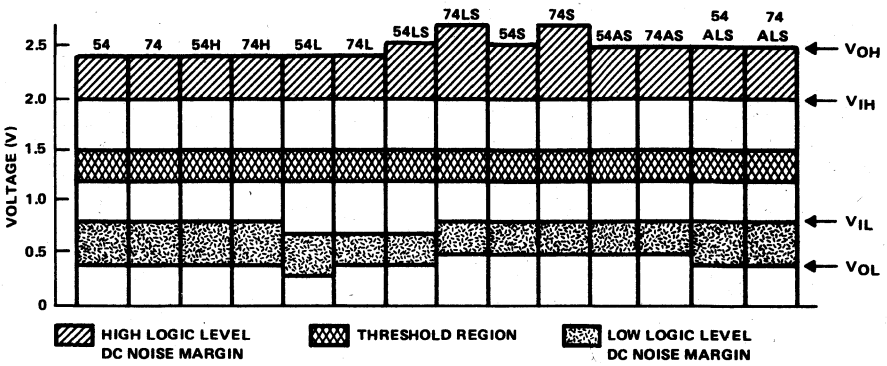


Figure 2. Series 54/74 TTL Family Compatible Levels Showing DC Noise Margins

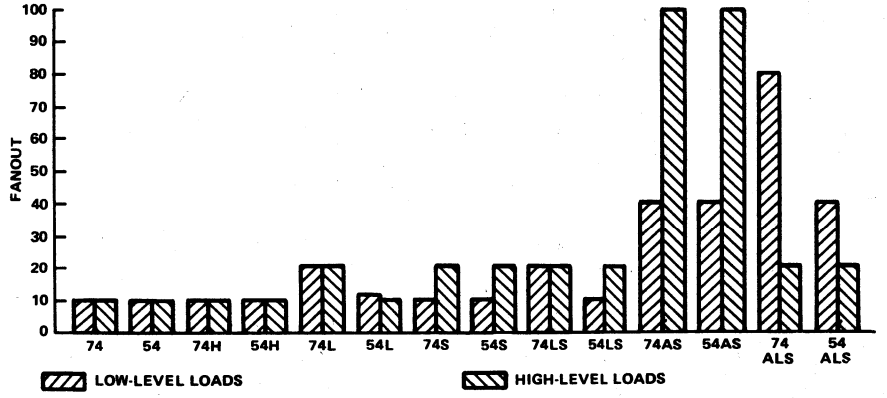


Figure 3. Fanout Capability

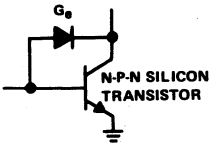


Figure 4. Baker Clamp

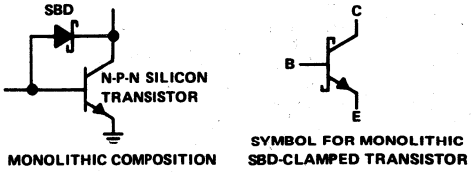


Figure 5. The Schottky-Clamped Transistor

saturation. The collector voltage drops, the germanium diode begins to conduct forward current, and excess base drive is diverted from the base-collector junction of the transistor. This causes the transistor to be held out of deep saturation, the excess base charge to not be stored, and the turn-off time to be dramatically reduced.

A germanium diode cannot be incorporated into a monolithic silicon integrated circuit. Therefore, the germanium diode must be replaced with a silicon diode which has a lower forward voltage drop than the base-collector junction of the transistor. A normal p-n diode will not meet this requirement. The SBD illustrated in Figure 5 can be used to meet the requirement.

The SBD illustrated in Figure 6 is a rectifying metal-semiconductor contact formed between a metal and a highly doped N semiconductor.

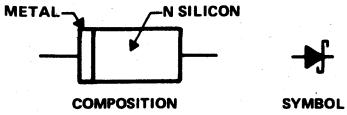


Figure 6. Schottky Barrier-Diode

The qualitative physics of an SBD is illustrated in Figure 7. The valence and conduction bands in a metal overlap make available a large number of free-energy states. The free-energy states can be filled by any electrons which are injected into the conduction band. A finite number of electrons exist in the conduction band of a semiconductor. The number of electrons depends mainly upon the thermal energy and the level of impurity atoms in the material. When a metal-semiconductor junction is formed, free electrons flow across the junction from the semiconductor, via the conduction band, and fill the free-energy states in the metal. This flow of electrons builds a depletion potential across the barrier. This depletion potential opposes the electron flow and, eventually, is sufficient to sustain a balance where there is no net electron flow across the barrier.

Under forward bias (metal positive), there are many electrons with enough thermal energy to cross the barrier potential into the metal. This forward bias is called "hot injection." Because the barrier width is decreased as forward bias V_F increases, forward current will increase rapidly with an increase in V_F.

When the SBD is reverse biased, electrons in the semiconductor require greater energy to cross the barrier. However, electrons in the metal see a barrier potential from the side essentially independent of the bias voltage and a small net reverse current will flow. Since this current flow is relatively independent of the applied reverse bias, the reverse current flow will not increase significantly until avalanche breakdown occurs.

A simple metal-n semiconductor collector contact is an ohmic contact while the SBD contact is a rectifying contact. The difference is controlled by the level of doping in the semiconductor material. As the doping is increased, the contact becomes more ohmic. Figure 8 illustrates the current-voltage characteristics according the doping applied.

Current in the SBD is carried by majority carriers. Current in the p-n junction is carried by minority carriers. The resultant minority carrier storage causes the switching

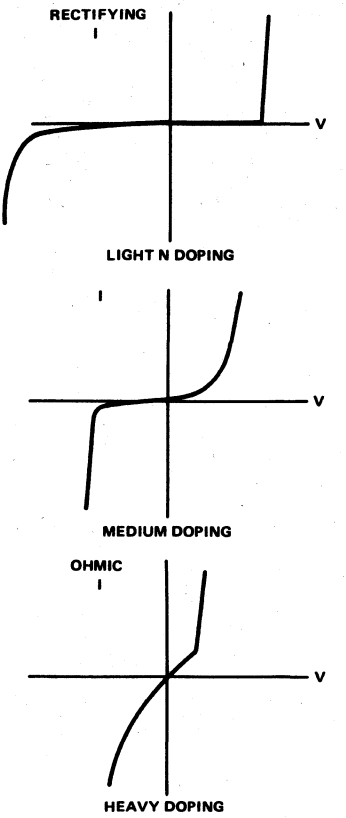


Figure 8. Metal-N Diode Current-Voltage Characteristics

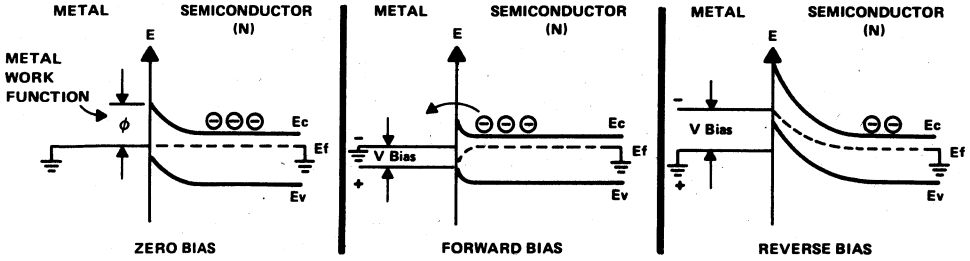


Figure 7. Schottky Barrier-Diode Energy Diagrams

time of a p-n junction to be limited when switched from forward bias to reverse bias. A p-n junction is inherently slower than an SBD even when doped with gold.

Another major difference between the SBD and p-n junction is the forward voltage drop. For diodes of the same surface area, the SBD will have a larger forward current at the same forward bias regardless of the type of metal used. The SBD forward voltage drop is lower at a given current than a p-n junction. Figure 9 illustrates the current carriers and forward current-voltage characteristics differences between the SBD and p-n junction. The SBD meets the requirements of a silicon diode which will clamp a silicon n-p-n transistor out of saturation.

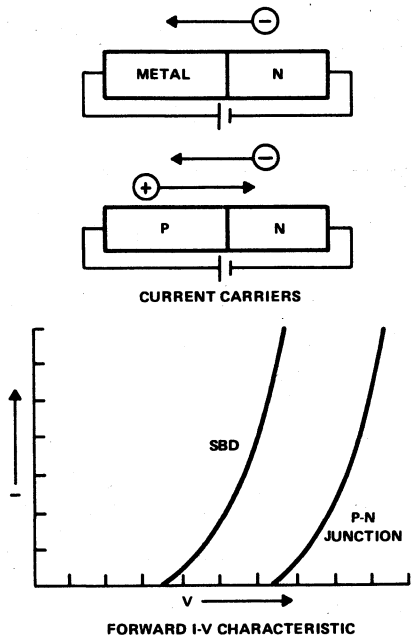


Figure 9. Differences Between P-N and Schottky Barrier-Diodes

The Advanced Schottky process differs from the Schottky process in that it uses ion implantation of impurities instead of diffusion. Ion implantation gives greater control on the depth of doping and resolution. Because of a thinner epitaxial layer and smaller all around geometries, smaller parasitic capacitances are encountered. The performance of the SBD is also enhanced by the use of oxide isolation of the transistors. This reduces the collector-substrate capacitance. Figure 10 illustrates the 'LS/'S process which consists of conventional masks, junction isolation, and a

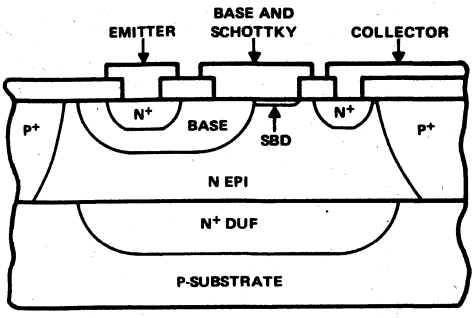


Figure 10. Standard Process ('LS/'S)

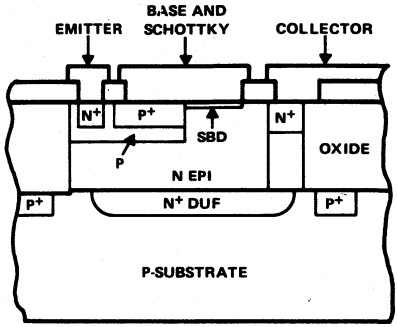


Figure 11. Advanced Process ('ALS/'AS)

standard metal system and Figure 11 illustrates the 'ALS/'AS process which consists of composed masks, ion implantation, oxide isolation, and a standard metal system.

Analysis of 'ALS and 'AS NAND Gates

The 'ALS and 'AS NAND gates in Figures 12 and 13 combine the desirable features of improved TTL circuits with the technological advantages of full Schottky clamping, ion implantation, and oxide isolation to achieve very fast switching times at a reduced speed-power product. The improvements and advantages are as follows:

1. Full Schottky clamping of all saturating transistors virtually eliminates storing excessive base charge and significantly enhances turn-off time of the transistors.
2. Elimination of transistor storage time provides stable switching times across the temperature range.
3. An active turn-off is added to square up the transfer characteristic and provide an improved high-level noise immunity.

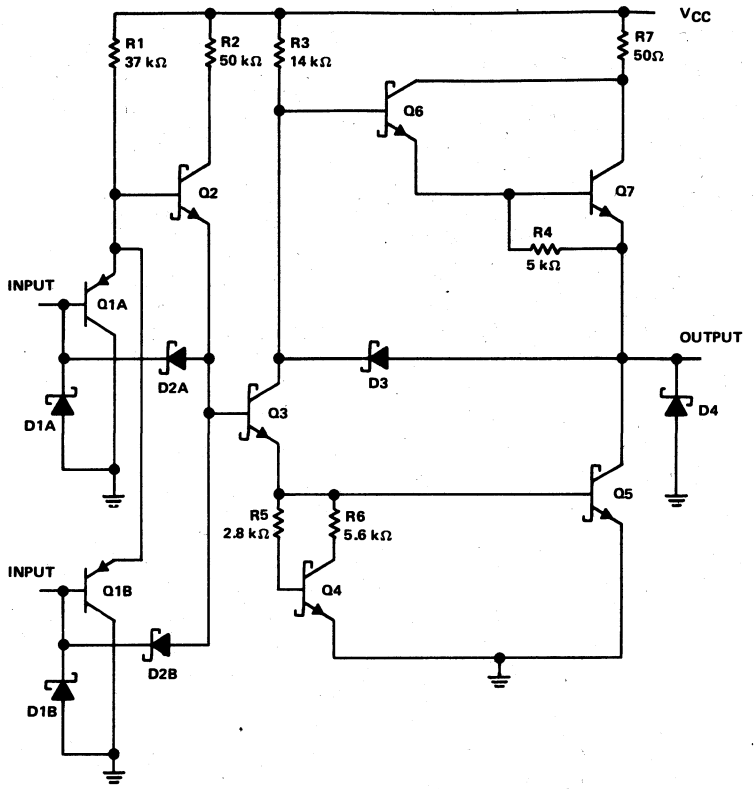


Figure 12. 'ALS00A NAND Gate Schematic

4. Input and output clamping is implemented with Schottky diodes to reduce negative-going excursions on the inputs and outputs. Because of its lower forward voltage drop and fast recovery time, the Schottky input diode provides improved clamping action over a conventional p-n junction diode.
5. The ion implantation process allows small geometries giving less parasitic capacitances so that switching times are decreased.
6. The reduction of the epi-substrate capacitance using oxide isolation also decreases switching times.

A key feature of the 'ALS and 'AS families is the improvement in typical input-threshold voltage. Figure 12 is a schematic diagram of the 'ALS00A NAND gate. Figure 13 is a schematic diagram of the 'AS00 NAND gate. The input threshold voltage of the devices is determined by the equation:

$$VT = V_{BE} \text{ of Q2} + V_{BE} \text{ of Q3} + V_{BE} \text{ of Q5} - V_{BE} \text{ of Q1A (or } V_{BE} \text{ of Q1B)} \quad (1)$$

From Eq. (1) it can be determined that the input threshold voltage is two times V_{BE} or approximately 1.4 V. Low-level input current I_{IL} is reduced in the 'ALS00A/'AS00 gates because of the improved input circuits. Buffering by transistors Q1A (or Q1B) and Q2 causes a significant reduction in low-level input current. Low-level input current is determined by the equation:

$$I_{IL} = V_{CC} - V_{BE} \text{ of Q1A} - V_I/[R(h_{FE} \text{ of Q1A} + 1)] \quad (2)$$

By using Eq. (2) low-level input current is reduced by at least the factor of h_{FE} of Q1A + 1 and is typically $-10\ \mu A$ for the 'ALS00A and $-50\ \mu A$ for the 'AS00. High-level output voltage V_{OH} is determined primarily by V_{CC},

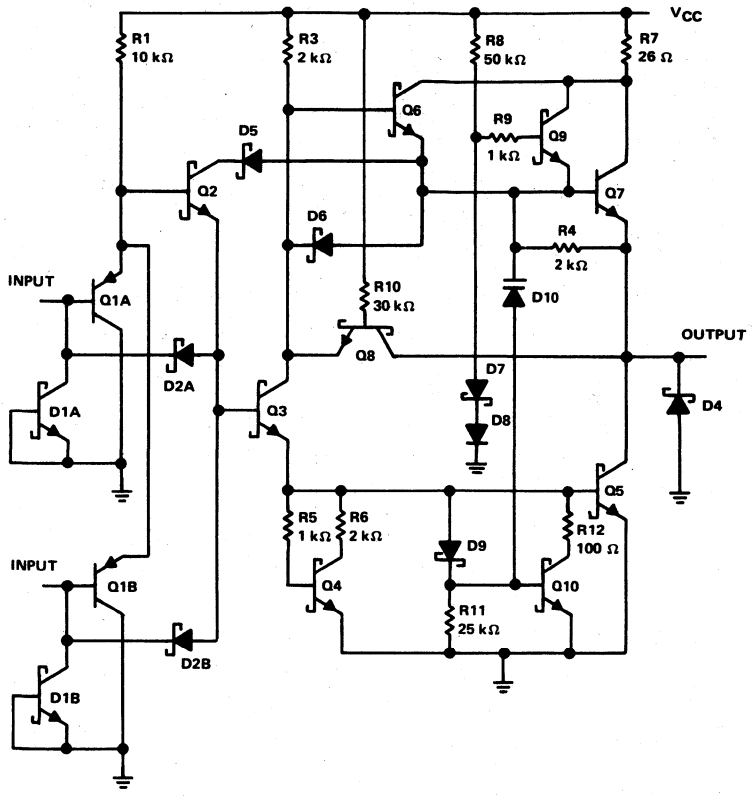


Figure 13. 'AS00 NAND Gate Schematic

resistors R4 and R7, and transistors Q6 and Q7. With no load, the high-level output voltage is approximately equal to $V_{CC} - V_{BE}$ of Q6 because the voltage across resistor R4 is 0 V. For medium-level currents, the high-level output voltage is equal to $V_{CC} - V_{BE}$ of Q6 $- V_{BE}$ of Q7 because of the Darlington gain of transistors Q6 and Q7. The current through resistor R3 is typically less than 1 μA and, therefore, the voltage drop is negligible. As conduction through transistors Q6 and Q7 is increased, the voltage drop across limiting resistor R7 will increase until the Schottky clamping diode of transistor Q6 starts to become forward biased. At this point, the current through resistor R3 (and the voltage drop) is no longer negligible and the high-level output voltage is determined by:

$$V_{OH} = V_{CC} - I_{OH \text{ through R7}} \times R7 - V_{CE} \text{ of Q6} - V_{BE} \text{ of Q7} \quad (3)$$

Low-level output voltage V_{OL} is determined by the turning on of transistor Q5. When the input is high and transistor Q2 is turned on, high-current transistor Q5 is turned on by a current path through transistor Q3 and resistor R3. Sufficient base drive is supplied to keep transistor Q5 fully turned on at an apparent output resistance of 14 Ω for 'ALS and 6Ω for 'AS.

The fanout is up to 40 for a '54ALS device that is driving a '54ALS device and up to 80 for a '74ALS device, that is driving a '74ALS device and provides a guaranteed low-level output current of 4 mA and 8 mA, respectively.

The increase in speed-power product of '54ALS/'74ALS devices, a factor four times better than '54LS/'74LS devices, is due to the design consideration of the quiescent and switching operations of the circuit. In the quiescent state, transistor Q2 allows the use of a reduced low-level input current. This reduces the fanout and reduces the overall quiescent current requirements.

The design of diodes D2 and D3 (or transistor Q8) and transistor Q4 enhances the speed-power product of the device. Transistor Q4 reduces the turn-off time and consequently the current transients caused by conduction

overlap of transistor Q5. The same principle is used by diodes D2 and D3 and transistor Q3 in turning off transistor Q7. In addition, the active turn-off design produces a square transfer characteristic.

The 'AS00 gate has additional circuits not on the 'ALS00A gate. The circuits are added to enhance the throughput of the 'AS Family.

Transistor Q10 has been added as a discharge path for the base-collector capacitance of transistor Q5. Without transistor Q10, rising voltages at the collector of transistor Q5 would force current, via the base-collector capacitance, into the base of transistor Q5 causing it to turn on. However, diode D10 causes transistor Q10 to turn on (during rising voltage) and keeps transistor Q5 turned off. Diodes D6 and D9 serve as a discharge path for capacitor-diode D10.

CIRCUIT PARAMETERS

Worst-case testing of 'ALS/'AS devices provides a margin of safety. [All dc limits shown on the data sheet are guaranteed over the entire temperature range ($-55\,°C$ to $125\,°C$) for series 54ALS/54AS and $0\,°C$ to $70\,°C$ for series 74ALS/74AS)]. In addition, the dc limits are guaranteed over the entire supply voltage range (4.5 V to 5.5 V).

Transfer Characteristics

Since the most common application for a logic gate is to drive a similar logic gate, the input and output logic levels must be compatible. The input and output logic levels for 'ALS/'AS devices are as follows:

- V_{IL} — The voltage value required for a low-level input voltage that guarantees operation
- V_{IH} — The voltage value required for a high-level input voltage that guarantees operation
- V_{OL} — The guaranteed maximum low-level output voltage of a gate
- V_{OH} — The guaranteed minimum high-level output voltage of a gate.

With the exception of high-level ouput voltage (which is a direct function of supply voltage), these values remain virtually unchanged over the temperature range and under normal operating conditions of the device.

Analysis of the input and output response characteristics of 'ALS/'AS TTL gates is necessary to understand the operation of these devices in most system applications. The dc response characteristics can best be depicted by an input voltage V_I versus output voltage V_O transfer plot.

Figure 14 plots the 'ALS/'AS characteristics as compared with members of other TTL logic families.

As shown in Figure 14, the 'ALS and 'AS devices exhibit a much better output savings when compared with standard TTL devices. The better high-level output voltage is primarily because of the active turn off of the low-level output transistor. The diode voltage drop in the normal output is replaced by a low-current V_{BE} voltage drop. This provides

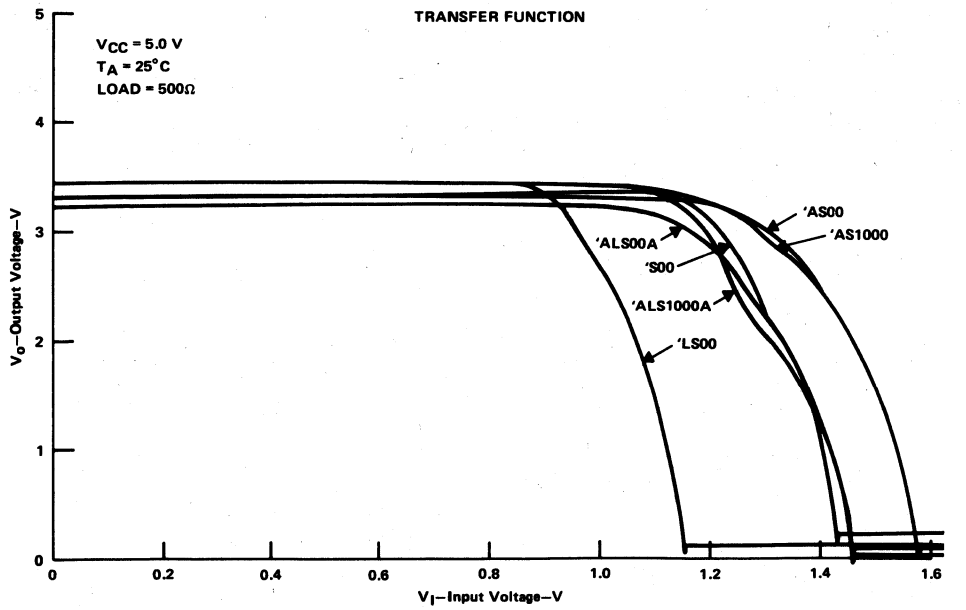


Figure 14. Input Voltage vs Output Voltage of 'ALS/'AS

a better high-level noise immunity in 'ALS and and 'AS over standard TTL devices.

Input Characteristics

To use 'ALS/'AS devices fully, a knowledge of the input and output characteristics is required. This is particularly true when a device interfaces with a device not in the same TTL series. In addition, knowledge of voltage and current relationships for all elements is important for proper design.

Figure 15 illustrates a typical plot for input current I_I versus input voltage, V_I, characteristics for 'ALS/'AS gate inputs during normal operation. A typical series 54/74 characteristic plot is also shown for reference. Any device used to drive a TTL gate must source and sink current. Conventionally, current flowing toward a device input terminal is designated as positive and current flowing out of a device input terminal is designated as negative. Low-level input current is negative current because it flows out of the input terminal. High-level input current is a positive current because it flows into the input terminal.

For transmission line conditions, a more accurate plot of the reverse bias section of these curves is required. These curves, Figure 16, are characteristic of the input clamping diode.

Low-Level Input Current

Figure 17 illustrates the dc equivalent of a standard 'ALS/'AS input circuit and shows the input current paths during a low-level input state. The low-level input current is primarily determined by resistor R1. However, low-level input current is also a function of the supply voltage, the ambient temperature, and the low-level input voltage. To

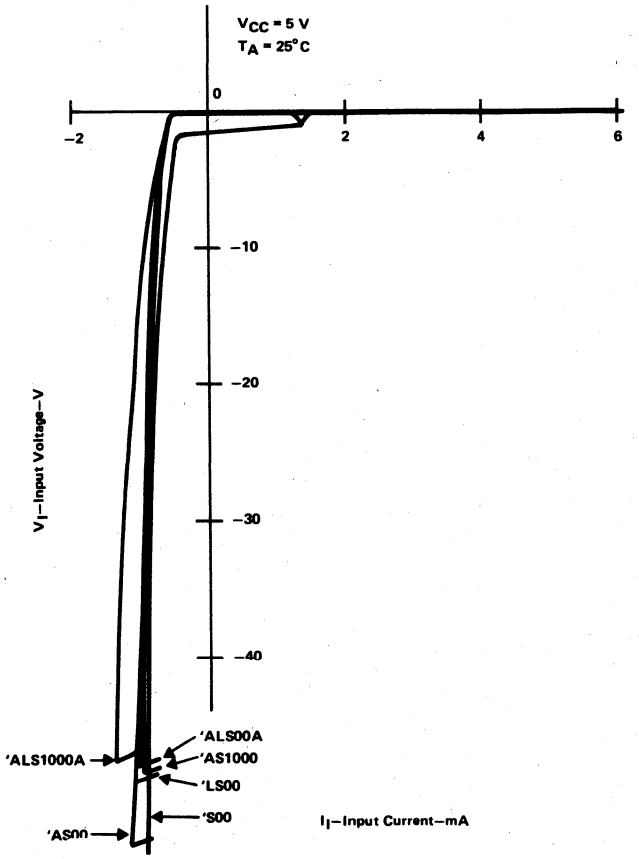


Figure 15. Input Current vs Input Voltage for TTL Families

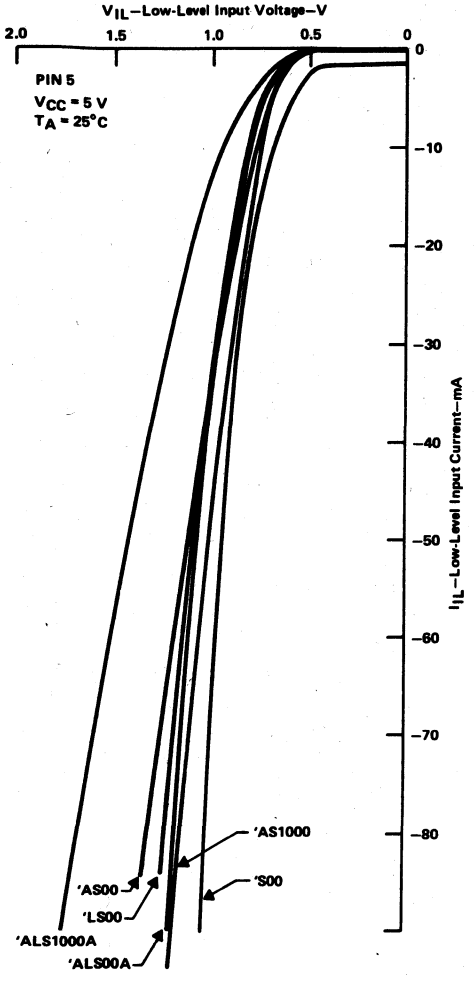


Figure 16. Low-Level Input Current vs High-Level Input Voltage for TTL Families

assure desired device operation under all possible conditions, the worst-case test is performed on all devices. Supply voltage is taken to the highest allowable value to cause the low-level input current to be at a maximum. With the exception of the input under test, all unused inputs are taken to a high level. This enhances any contribution of these inputs to the low-level input current of the emitter under test.

Input Clamping Diode Test

The quality of the input clamping SBD (D2 in Figure 17) is tested by ensuring that the forward voltage drop is not

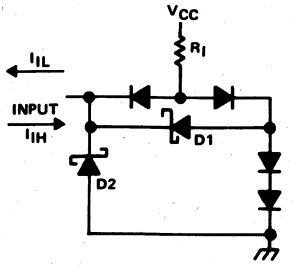


Figure 17. DC Equivalent Input Circuit for Series 'ALS Gate

greater than −1.2 V for 'AS and −1.5 V for 'ALS with a forward current of 18 mA. These values are guaranteed at minimum supply voltage and are valid across the operating temperature range. The characteristic of the input diode is illustrated in Figure 16.

High-Level Input Current

Another input parameter that must be measured and controlled is high-level input current. To ensure desired device operation under all possible conditions, the worst-case test is performed with all unused inputs grounded and supply voltage at its maximum value. This provides the highest value of low-level input current. Those devices with a high-level input current of sufficient magnitude to cause a degradation of high-level output voltage at an output must be screened out.

Input Breakdown Test

An additional high-level input current test is performed to check for base-emitter breakdown under the application of the full range of input voltages. This test is performed under the worst-case supply voltage conditions and is important because the base-emitter junction is small and can easily be overdissipated during the breakdown conditions.

Output Characteristics

The most versatile TTL output configuration is the push-pull (totem-pole) type. The totem-pole output has a low output impedance drive capability at both high and low logic levels. Both 'ALS and 'AS families use this configuration and have fanouts of 40 in both the high- and low-level states.

High-Level Output Characteristics

The ability of the totem-pole output to supply high-level output current is parametrically tested by applying a high-level input current value during measurement of high-level output voltage. However, the quality of the output stage is best indicated by parametrically measuring its current sourcing I_{OS} capability when connected to ground. Figure 18 shows the equivalent output circuit under high-level output conditions.

Figure 19 illustrates typical high-level characteristics. When measuring worst-case high-level output voltage, minimum supply voltage is used. A worst-case low-level

input voltage is applied to an input and all unused inputs are tied to supply voltage.

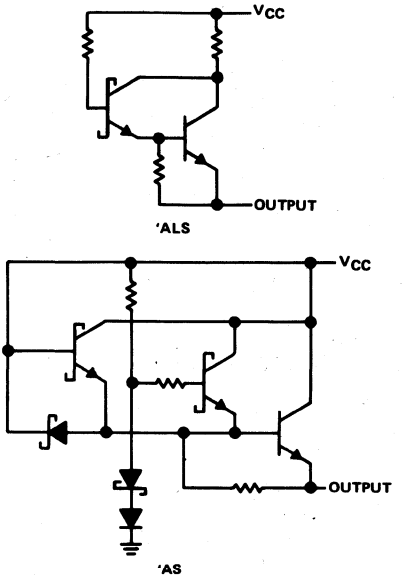


Figure 18. Equivalent Output Circuit for 'ALS/'AS Gates

Low-Level Output Characteristics

Figure 20 shows that section of the output drive circuit which produces a low-level output voltage V_{OL}. This characteristic is also tested at minimum supply voltage. Figure 21 illustrates the typical curve.

Switching Speed

Two switching-speed parameters are guaranteed on Series 'ALS and 'AS gates: propagation delay time for a high-level to a low-level at the output t_{PHL}, and a low-level to high-level transition time t_{PLH}. Both parameters are specified with respect to the input pulse using standard test conditions as follows:

V_{CC} = 4.5 V to 5.5 V
C_L = 50 pF
R_L = 500
T_A = MIN to MAX

Under these conditions, times in the order of 4 ns for 'ALS and 1.7 ns for 'AS are typical. Figures 22 and 23 illustrate how the propagation delay time for 'ALS and 'AS devices vary with load capacitance.

Most current in the output stage is drawn when both output transistors are on (i.e., during output transitions, the average power dissipation of a gate with a totem-pole output increases with operating frequency). This is caused by more high-current transitions per second at the output as the frequency increases. Figure 24 illustrates the effect for both 'ALS and 'AS devices.

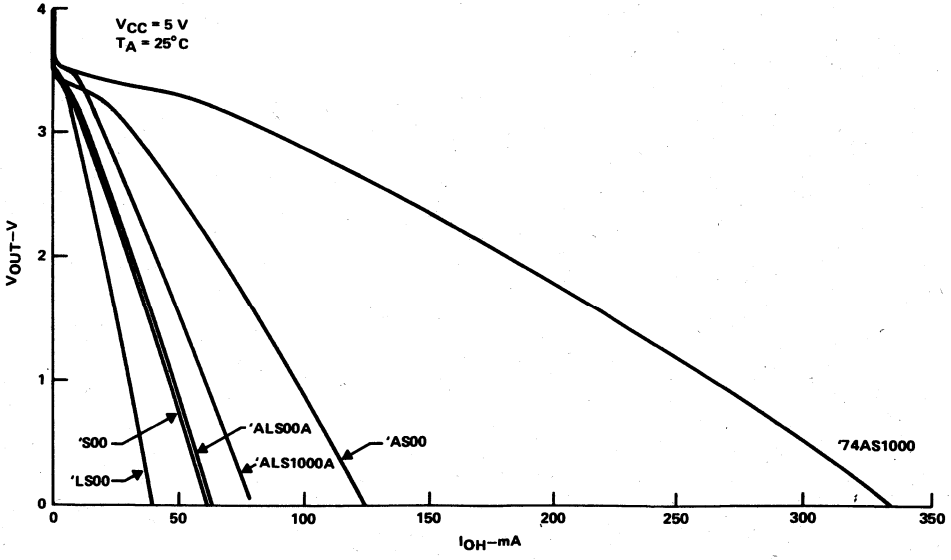


Figure 19. High-Level Output Voltage vs High-Level Output Current

DC Noise Margins

Noise margin is a voltage specification which guarantees the static dc immunity of a circuit to adverse operating conditions. Noise margin is defined as the difference between the worst-case input logic level (V_{IH} minimum or V_{IL} maximum) and the guaranteed worst-case output (V_{OH} minimum or V_{OL} maximum) specified to drive the inputs. Table 2 lists the worst-case output limits for the 'AS and 'ALS families.

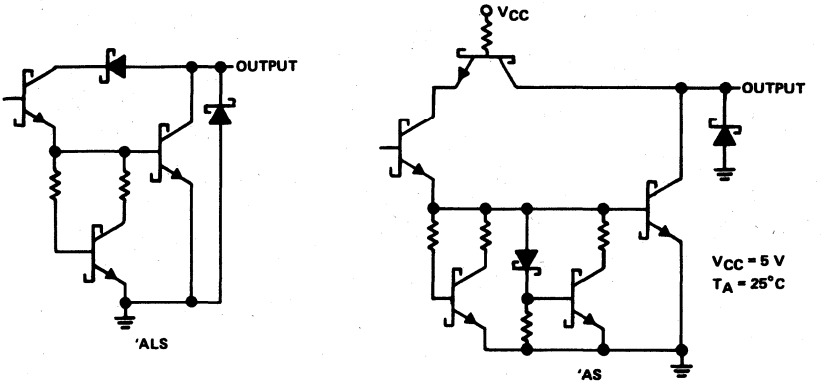


Figure 20. Low-Level Output Circuit for 'ALS/'AS Gates

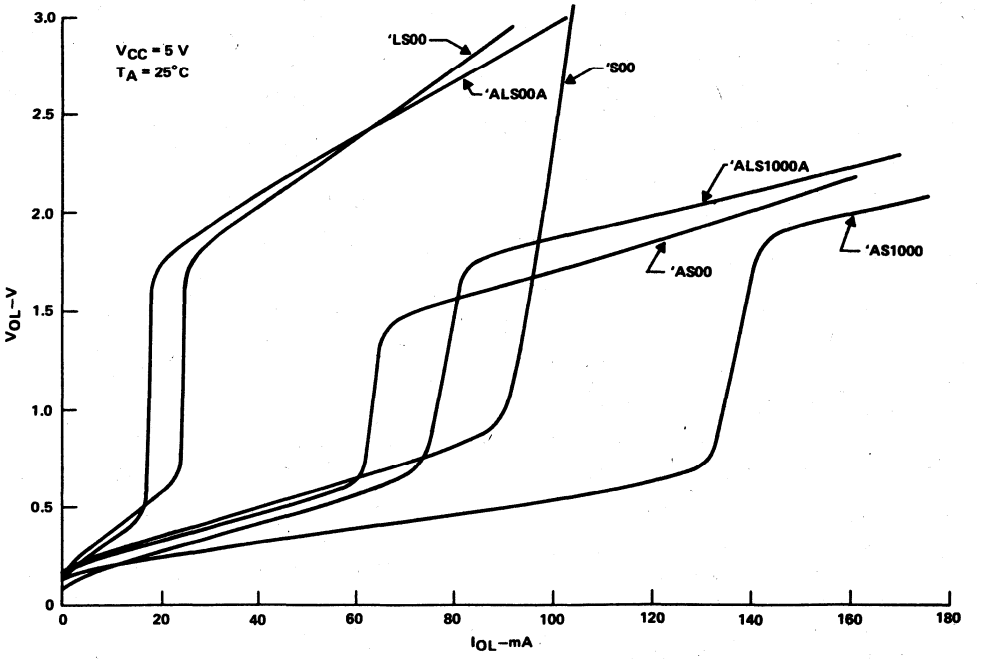


Figure 21. Low-Level Output Voltage vs Low-Level Output Current

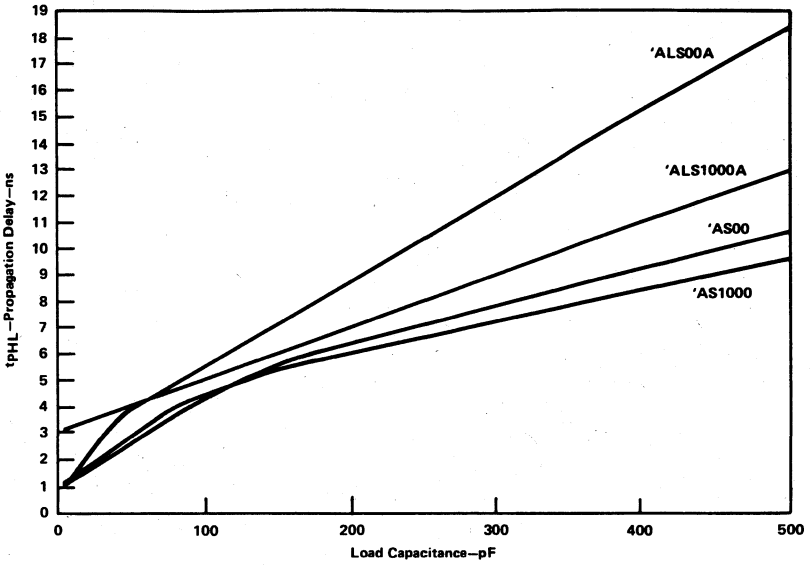


Figure 22. High- to Low-Level Propagation Delay vs Load Capacitance

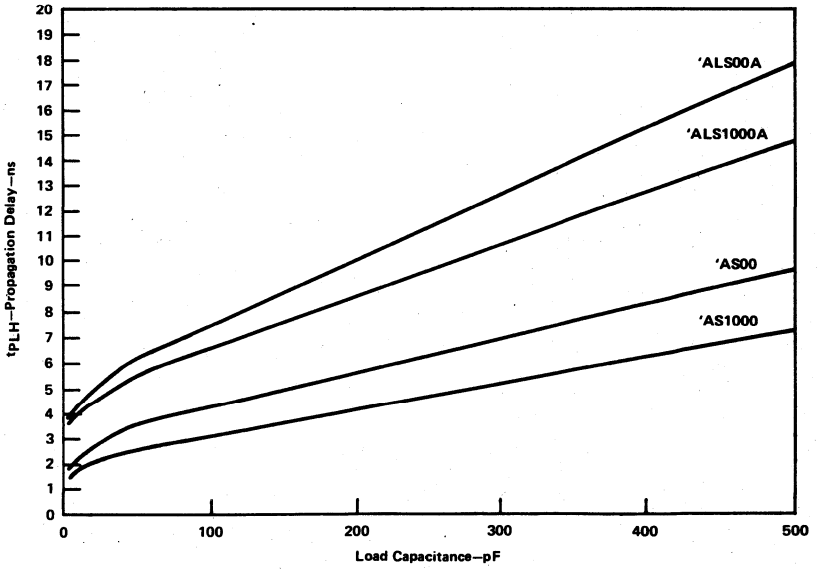


Figure 23. Low- to High-Level Propagation Delay vs Load Capacitance

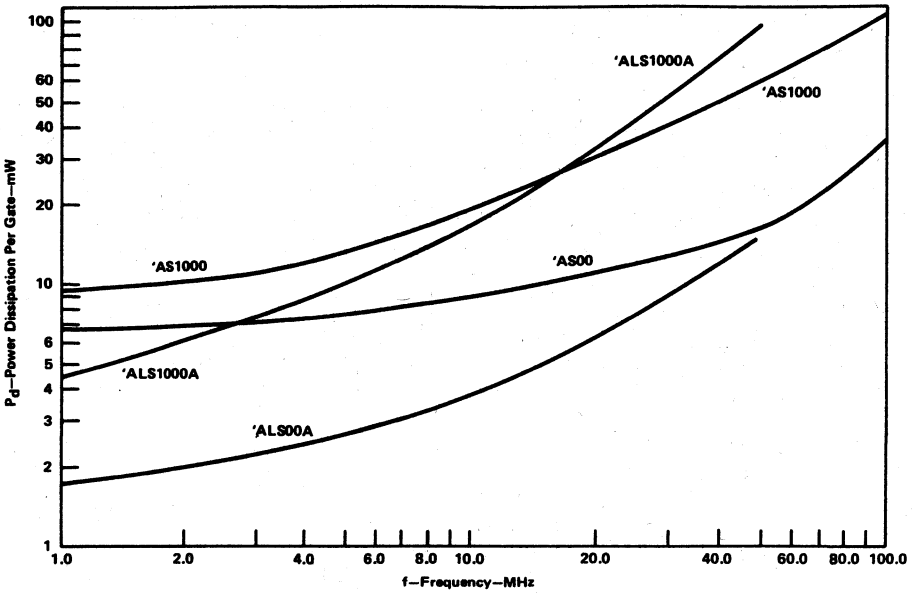


Figure 24. Power Dissipation per Gate vs Frequency

Specified Logic Levels and Thresholds

The high-level noise margin is obtained by subtracting V_{OH} minimum from V_{IH} minimum. The low-level noise margin is obtained by subtracting V_{IL} maximum from V_{OL} maximum. The worst-case high-level noise margin is guaranteed to be at least 500 mV for both 'AS and 'ALS devices and at least 300 mV for low-level noise immunity across the operating free-air temperature ranges.

The usefulness of noise margins at the system design level is the ability of a device to be impervious to noise spikes at the input. The input voltage falls into one of three categories: low-logic state (between ground and 0.8 V), threshold region (between 0.8 V and 2 V), or high-logic state (between 2 V and V_{CC}). If an input voltage remains exclusively in the low-logic or high-logic state, it can undergo any excursions within that state. A level change from 5.5 V to 2 V or from ground to 0.8 V should not affect the output state of the device. To guarantee an expected output level change, the appropriate input has to undergo a change from one input state to the other input state (i.e., a transition through the threshold region). If a device will not remain in the correct state when voltage excursions on the input are occurring, it is violating its truth table.

Noise Rejection

The ability of a logic element to operate in a noise environment involves more than the dc or ac noise margins previously discussed. To present a problem, an externally generated noise pulse must be received into the system and cause a malfunction. Stable logic systems with no storage

Table 2. Worst Case Output Parameters

PARAMETER (V)	'AS (0°C to 70°C)	'ALS (0°C to 70°C)	'AS (−55°C to 125°C)	'ALS (−55°C to 125°C)
V_{IH}(MIN)	2	2	2	2
V_{IL}(MAX)	0.8	0.8	0.8	0.8
V_{OH}(MIN) @ V_{CC} = 4.5 V*	2.5	2.5	2.5	2.5
V_{OL}(MAX)	0.5	0.5	0.5	0.4
High Level Noise Margin ($V_{OH}-V_{IH}$)	0.5	0.5	0.5	0.5
Low Level Noise Margin ($V_{IL}-V_{OL}$)	0.3	0.3	0.3	0.4

*Actual specification for $V_{OH(min)}$ is V_{CC} − 2 V.

elements are practically impervious to ac noise. However, large dc voltages could cause noise problems. Systems with triggerable storage elements or those operating fast enough for the noise to appear as a signal are much more susceptible to noise.

The noise voltage must be radiated or coupled into the circuit. The amount of noise required to develop a given voltage is a function of the circuit impedance. Because of the low output impedance of TTL circuits, noise immunity is improved. Noise is transferred from the source (with some arbitrary impedance) through a coupling impedance to the impedance of the circuit under consideration.

Figure 25 shows a circuit where the coupling impedance is stray capacitance and the load impedance is provided by the gates. The relatively tight coupling of this circuit and the loading effect on the driving source is significant enough

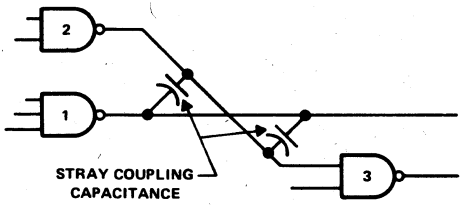


Figure 25. Stray Coupling Capacitance

to be considered. However, since the source effect is difficult to assess and is in a direction to improve rather than degrade the noise rejection, its effects are ignored. This results in a worst-case type of response indication. In the case of radiated noise, the source resistance is a definite factor in noise coupling and essentially replaces the reactive coupling impedance.

By ignoring the driving source impedance to make conditions more nearly standard, it is possible to determine a set of curves relating the developed noise pulse to the noise source amplitude, the noise rise or fall time, the coupling impedance, and the load impedance. Curves have been developed[1] for several different input waveforms. Since the 'ALS waveform is essentially a ramp with a dv/vt of 1 V/ns (approximately 2.5 V/ns for 'AS), the most applicable curve is that for a ramp input.

Figure 26(a) shows the equivalent circuit from which the ramp response plot in Figure 26(b) was developed. The input pulse shown in Figure 26(c) is a ramp input.

$$e_i(t) = \frac{E_i}{T}\ t$$

where

E_i = Maximum input voltage and
T = Total rise time of input voltage

The output pulse is represented analytically by

$$e_0(t) = \frac{E_i}{T}\ RC\left(1 - e^{-\frac{t/T}{RC/T}}\right)$$

$$e_0(i) = E_i\ \tau\left(1 - e^{-i/\tau}\right)$$

where

$$\tau = \frac{RC}{T}$$

$$\theta(i) = \tau\left(1 - e^{-i/\tau}\right)$$

$$\theta(i) = \frac{e_{0(i)}}{E_i}$$

with holding for unit time. This is followed by an exponentially decaying voltage with a time constant τ. Values of τ and i on the figure are normalized by the value of the total rise time of the stimulated noise pulse e_i. Using Figure 26(b), the pulse width and amplitude of the coupled noise pulse can be estimated.

As an example, using the circuit shown in Figure 25, apply a noise pulse of 3 V in amplitude and rising at 1 V/ns

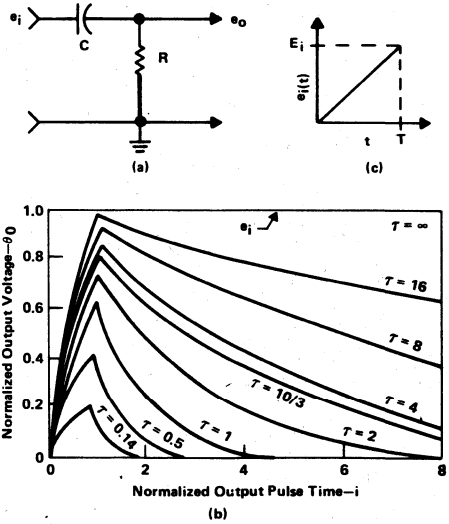


Figure 26. Evaluations of Gate Response to Fast Input Pulses

with gate 2 at a high-logic state. Assume a nominal output impedance of 58 Ω (30 Ω for 'AS) and coupling capacitance of 10 pF. Use the following formula:

$$\text{Total rise time } T = \frac{3\text{ V}}{1\text{ V/ns}^{**}} = 3\text{ ns}^{\dagger}$$

$$\tau = \frac{RC}{T} = \frac{(10 \times 10^{-12})(58)}{3}$$

$$= \frac{0.58 \times 10^{-9}}{3} = 0.19\text{ ns}$$

**2.5 V/ns for 'AS
†1.2 ns for 'AS

To convert the normalized values of τ and i in Figure 26(b) to actual values, multiply by 3 ns. The output voltage scale will be multiplied by 3 V. Using the $\tau = 0.19$ curve gives a peak e_o of 0.57 V (0.19 × 3) and a pulse width of 3 ns at the 50% points. To determine whether this pulse will cause interference, enter these values (0.57 V and 3 ns) on the graph shown in Figure 27. Since the gates have approximately 1.8 V of noise immunity at this point, they should not be affected.

If an open-collector gate is used with a passive 1 kΩ pull-up resistor, the situation would change. Use the following formula:

$$\text{Total rise time} = \frac{3\text{ V}}{1\text{ V/ns}^{**}} = 3\text{ ns}^{\dagger}$$

$$\tau = \frac{(10 \times 10^{-12})(1 \times 10^{3})}{3}$$

$$= \frac{10 \times 10^{-9}}{3} = \frac{10}{3}\text{ ns}$$

**2.5 V/ns for 'AS
†1.2 ns for 'AS

Now the amplitude (from the curves) approaches 2.58 V (0.86 × 3) and the pulse width at the 50% points is approximately 8.52 ns (2.84 × 3). The next gate will propagate this pulse.

This example is an oversimplification. The coupling impedances are complex (but resolvable into RLC series coupling elements) and the gate output impedance changes with load. Our purpose is to show why and how the low impedance of the active TTL output rejects noise and to make a comparison with a passive pull-up.

The ability to operate in a noisy environment is an interaction of the built-in operating margins, the time required for the device to react, and the ease with which a noise voltage is developed. In all cases, except the ability to react to short noise pulses, the TTL design has emhasized noise rejection.

Nothing has been discussed concerning noise in devices other than gate circuits. Many MSI devices are complex gate networks and, because of their small size, are more superior in a noisy environment operation than their discrete gate equivalents. Noise tolerance of latching devices is implied in the setup times, hold times, clock pulse width, data pulse widths, and similar parameters. Output impedances and input noise margins are quite similar to those of the gates and may be treated in a similar manner. If a latching device does become noise triggered, the effective error is stored and does not disappear with the noise.

Parameter measurement information is shown in Figure 28.

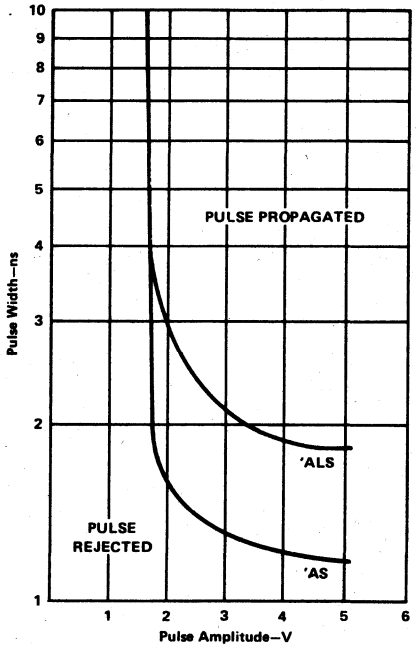
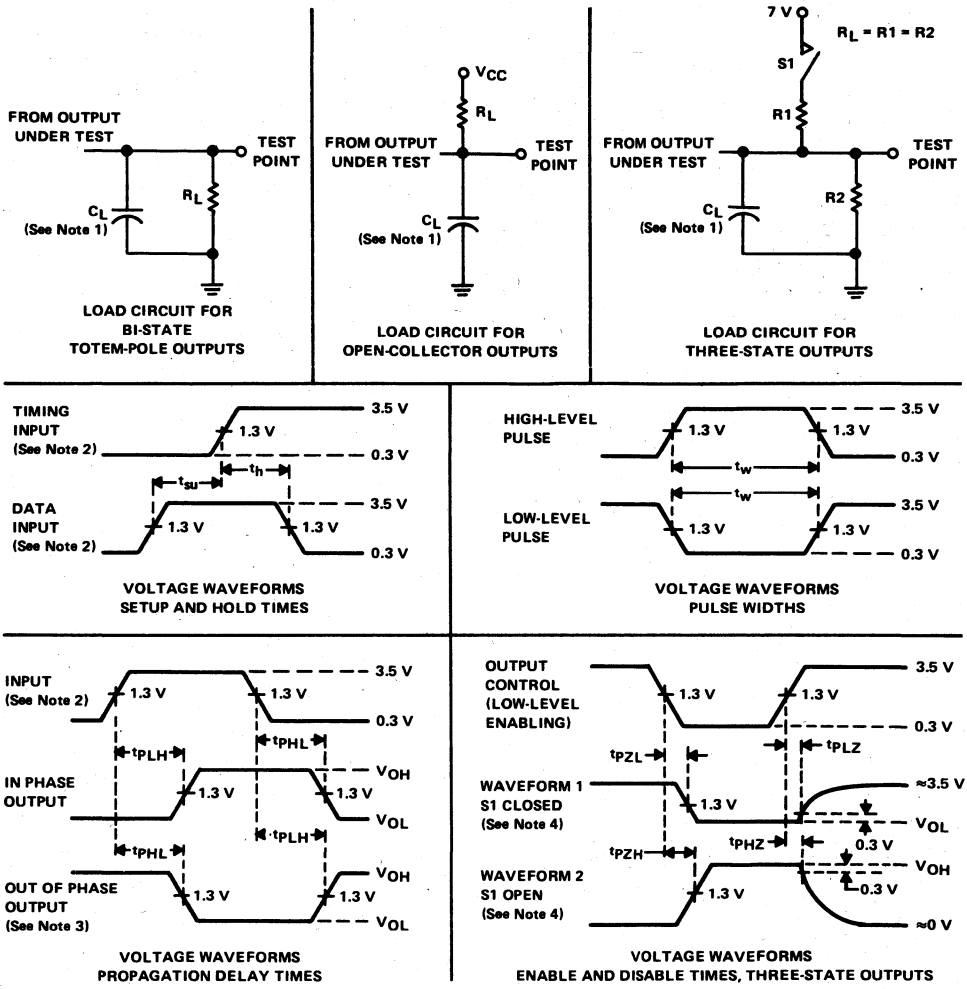


Figure 27. Theoretical Required Pulse Width vs Pulse Amplitude for 'AS and 'ALS Inputs

GUIDELINES FOR SERIES 'ALS/'AS TTL SYSTEM DESIGN

System layout and design requirements for Advanced Schottky TTL circuits are essentially the same as those guidelines which have previously been established and are applicable for all high-performance digital systems. Tables 3 through 6 provide a brief summary of the solutions to most design decisions needed to implement systems using Advanced Schottky TTL. Supplementary data which may be useful for developing specific answers to unique problems is provided later.



NOTES: 1. C_L includes probe and jig capacitance.
2. All input pulses have the following characteristics PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
3. When measuring propagation delay times of 3-state outputs, switch S1 is open.
4. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 28. Parameter Measurement Information

POWER SUPPLY REGULATION

Power supply regulation cannot be treated as if it is an independent characteristic of the device involved. Power supply regulation, along with temperature range, affects noise margins, fanout, switching-speed, and several other parameters. The characteristics most affected are noise margin and fanout. When these two parameters are within the specified limits, the power-supply regulation will normally be within specified limits. However, on a device where auxiliary parameters are more critically specified, a more restrictive power-supply regulation is normally required. When power-supply regulation is slightly outside the specified limits for TTL devices, the device may still

operate satisfactorily. However, if high ambient-noise levels and extreme temperatures are encountered, failures may occur.

Application of a supply voltage above 7 V (absolute maximum rating) will result in damage to the circuit.

Since power dissipation in the package is directly related to supply voltage, the maximum recommended supply voltage for TTL devices is specified at 5.5 V. This provides an adequate margin to ensure that functional capability and long-term reliability are not jeopardized.

High-level output voltage is almost directly proportional to supply voltage (i.e., a drop in supply voltage causes a drop in high-level output voltage and an increase in supply voltage results in an increase in high-level output voltage). Because of this relationship, high-level output voltage for 'ALS/'AS devices is specified as supply voltage -2 V (V_{CC} -2 V).

Since high-level output voltage is directly related to supply voltage, the output current of the device is also directly related. The output current value is established by choosing output conditions to produce a current that is approximately one-half of the true short-circuit current.

It is advantageous to regulate or clamp the maximum supply voltage at 5.5 V including noise ripple and spikes. When this conditions exists, unused AND and NAND gates can be connected directly to the supply voltage.

Table 3. Guidelines for Systems Design for Advanced Schottky TTL

ITEM	GUIDELINE
Single wire connections	Wire lengths up to approximately 12 inches may be used. A form of ground plane is desirable. Use point-to-point routing rather than parallel. If the wire is longer than 12 inches, use either a dense ground plane with the wire routed as close to it as possible, or use a twisted-pair cable.
Coaxial and twisted-pair cables	Design around approximately 80 Ω to 100 Ω of characteristic impedance. Cross talk increases at higher impedances. Use a coaxial cable of 93 Ω impedance (e.g., Microdot 293−3913). For twisted-pair cable, use number 26 or number 28 wire with the insulation twisted at the rate of 30 turns per foot.
Transmission-line-ground	Ensure that transmission-line ground returns are carried through at both transmitting and receiving ends. V_{CC} decoupling ground, device ground, and transmission-line ground should have a common tie point.
Cross talk	Use point-to-point back-panel wiring to minimize noise pickup between lines. Avoid long unshielded parallel runs. However, if they must be used, they should carry signals that propagate in the same direction.
Reflections	Reflections occur when data interconnects become long enough that 2-line propagation delays are pulse transition times. For series TTL, reflections are normally of no importance for lines shorter than 12 inches.
Resistive pull-up	If fanout of driving output permits, use approximately 300 Ω of resistive pull-up at the receiving end of long cables. This provides added noise margin and more rapid rise times.

Table 4. Guidelines for Printed Circuit Board Layout for Advanced Schottky TTL

ITEM	GUIDELINE
Signal connections	Whenever possible, distribute loads along direct connections. Signal leads should be kept as short as possible. However, lead lengths of up to 15 inches will perform satisfactorily. This is especially for large boards that use a ground plane, ground, and/or V_{CC} plane. In addition, it will perform satisfactorily for small boards using ground mesh or grid. In high-frequency applications, avoid radial fanouts and stubs. If they must be used to drive some loads, reduce lead length proportionally and, avoid sharp bends. Normal on-board fanouts and interconnections do not require terminations. Response of lines driving large numbers or highly capacitive loads can be improved with terminations of 300 Ω to V_{CC} and 600 Ω to ground in parallel with the last load if fanout of the driving output permits.
Conductor widths	Signal-line widths down to 0.015 inch are adequate for most signal leads.
Signal-line spacing	Signal-lead spacing on any layer down to 0.015 inch can be used especially if care is taken to avoid adjacent use of maximum length and minimum spacing. Increase spacing wherever layout permits. Pay particular attention to clock and/or other sensitive signals.
Insulator material	Thickness of insulation material used for a multilayer board is not critical. If ground and V_{CC} planes or meshes are used, their capacitive proximity can be used to reduce the number of decoupling capacitors needed and this also supplements the supply bypass capacitor.

Table 5. Guidelines for General Usage of Advanced Schottky TTL

ITEM	GUIDELINE
Power supply	For RF bypass supply primary, maintain ripple and regulation at less than or equal to 10%.
V_{CC} decoupling	Decouple every 2 to 5 packages with RF capacitors of 0.01 to 0.1 μF. Capacitors should be located as near as possible to the decoupled devices. Decouple line driving or receiving devices separately with 0.1 μF capacitors between V_{CC} and the ground pins.
On-board grounding	A ground plane is essential when the PCB is relatively large (over 12 inches). Smaller boards will work with ground and/or V_{CC} mesh or grid.
System grounding	Try to simulate bus bars with a width to thickness ratio greater than or equal to 4. This can be accomplished by multiple parallel wires or by using flat braid. Performance will be enhanced when a copper or silver-copper bus is used. The width to thickness ratio required will vary between systems, but greater than or equal to 4 will satisfy most systems.

Table 6. Guidelines for Gates and Flip-Flops Using Advanced Schottky TTL

ITEM	GUIDELINE
Data input rise and fall times	Reduce input rise and fall times as driver output impedance increases. Rise and fall times should be equal to or less than 15 ns/V and essentially free of noise ripple.
Unused input of AND and NAND gates and unused preset and clear inputs of flip-flops	Tie the unused input of AND and NAND gates and the unused preset and/or clear inputs of flip-flops as follows: 1. Directly to V_{CC}, if the input voltage rating of 5.5 V maximum is not exceeded. 2. Through a resistor equal to or greater than 1 kΩ to V_{CC}. Several inputs can be tied to one resistor. 3. Directly to a used input of the same gate, if maximum fanout of driving device will not be exceeded. Only the high-level loading of the driver is increased. 4. Directly to an unused gate output, if the gate is wired to provide a constant high-level output. Input voltage should not exceed 5.5 V.
Unused input of NOR gates	Tie unused input to used input of same gate, if maximum fanout of driving device will not be exceeded or tie unused input to ground.
Unused gates	Tie input of unused NAND and NOR gates to ground for lowest power drain. Tie inputs of unused AND gates high and use output for driving unused AND or NAND gate inputs.
Increasing gate/buffer fanout	Connect gates of same package in parallel.
Clock pulse of flip-flops	Drive clock inputs with a TTL output. If not available, rise and fall times should be less than 50 ns/V and free of ripple noise spikes.

SUPPLY VOLTAGE RIPPLE

Ripple in the supply voltage is generally considered a part of the supply voltage regulation. However, when combined with other effects (e.g., slow rise times), ripple voltage is more significant.

The effect of ripple voltage V_R can appear on either the supply voltage V_{CC} or the ground supply GND. When ripple appears on the supply voltage, it causes modulation of the input signal. The extent of the effect depends upon circuit parameters and source impedance.

The turning on of transistor Q5, shown in Figures 12 and 13, is controlled by the voltage at the base of transistor Q2 with respect to ground in accordance with the formula:

$$V_B = V_{BE} \text{ of Q2} + V_{BE} \text{ of Q3} + V_{BE} \text{ of Q5}$$

When ripple voltage is modulated onto the input voltage, the amplitude depends on the source impedance (Figure 29). The amplitude can be determined by the following equation:

$$\Delta V_R = V_R\left(\frac{R1/\beta}{R1/\beta + R2}\right)$$

$$= V_R\left(\frac{R1}{R1 + \beta R2}\right)$$

where $R1$ = source impedance
β = gain of transistor Q1.

Ripple voltage has the effect of adding extra pulses to the input signal (Figure 30). When ripple voltage appears in the ground supply, the threshold voltage is modulated and extra pulses occur (Figure 31).

Although decreasing the source impedance will reduce the effects of ripple voltage, it cannot be eliminated entirely because the emitter-base junction has an apparent resistance of approximately 30 Ω. Because of cancellation between the driving gate and the driven gate, low-frequency ripple is not a problem.

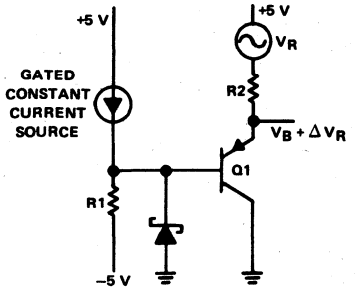


Figure 29. Effect of Source Impedance on Input Noise

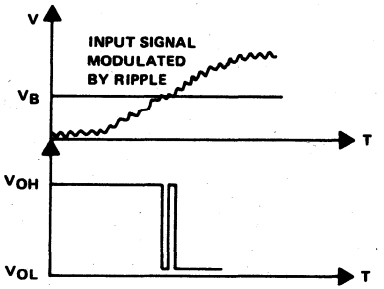


Figure 30. Spurious Output Produced by Supply Voltage Ripple

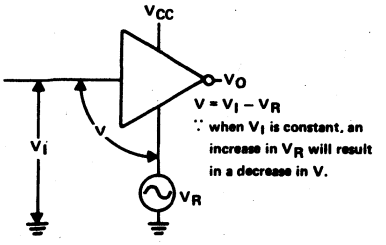


Figure 31. Effect of Ground Noise on Noise Margin

NOISE CONSIDERATIONS

Extraneous voltages and currents (called noise) introduced into a digital logic circuit are discussed in the following paragraphs. Figure 32(a) is a typical digital logic

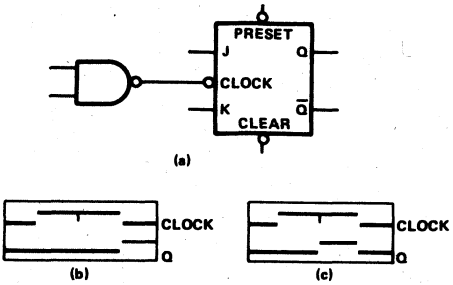


Figure 32. Typical Logic Circuit with Noisy Input

circuit consisting of a NAND gate and a J-K flip-flop. When a small noise pulse is coupled onto the clock input [(Figure 32(b)], the flip-flop does not respond and the Q output is correct. However, when a large noise pulse is coupled onto the clock input [(Figure 32(c)], the flip-flop sees the pulse as a clock transition and an erroneous Q output occurs. Therefore, it is essential to protect digital logic circuits from noise.

Noise Types and Control Methods

The noise types encountered in digital logic systems, their source, and the method of controlling them are as follows:

1. External noise — External noises radiated into the system. The sources include circuit breakers, motor brushes, arcing relay contacts, and magnetic-field-generating. The methods of controlled to be considered are shielding, grounding, or decoupling.
2. Power-line noise — Noise coupled through the ac or dc power distribution system. The initial sources and controlling methods are the same as for external noise.
3. Cross talk — Noise induced into signal lines from adjacent signal lines. Controlling methods to consider are shielding, grounding, decoupling, and, where possible, increasing the distance between the signal lines.
4. Signal-current noise — Noise generated in stray impedances throughout the circuit. The controlling methods to consider are shielding, grounding, decoupling, and, where possible, reduction of stray capacitance in the circuit.
5. Transmission-line reflections — Noise from unterminated transmission lines that cause ringing and overshoot. The method of control is to use, where possible, terminated transmission lines.
6. Supply-current spikes — Noise caused by switching several digital loads simultaneously. The controlling method is to design, where possible, the system so that digital loads are not switched simultaneously.

Shielding

In addition to its own internally generated noise, electrical equipment must operate in an extremely noisy environment. Noise pulses, which may come from a number of sources, consist of an electrostatic field, and electromagnetic field, or both. The noise waveform must be prevented from entering the equipment. This is accomplished by shielding. Since the noise fields are usually changing at a rapid rate, the shield required to exclude them may be very small. For effective exclusion, the sensitive circuits must be completely shielded.

Aluminum or similar materials are effective in stopping electrostatic noise. However, only a ferrous metal can successfully protect equipment against magnetic fields. While it is helpful to connect the system to earth ground, the shield system must be complete and must be grounded to the system ground to prevent the shield from coupling noise into the system.

External noise may be conducted into the system by the power lines. Decoupling and filtering of these lines should be standard design procedure.

Grounding and Decoupling

The total propagation delay is of secondary importance in generation of internal noise. The actual transition time determines the amplitude and frequency spectrum of the generated signal at the higher harmonics. Application of the Fourier integral to series 'ALS/'AS waveforms shows frequency components of significant amplitude that exceed 100 MHz. Because of the frequency spectrum generated when an 'ALS/'AS device switches, a system using these devices must consider problems caused by radio frequency (RF) even though the repetition rates may be only a few megahertz. The transient currents generated by charging capacitors, changes in the levels of dc, line driving, etc., must be considered. In Figure 33 for example, a gate driving a transmission line is represented by a voltage source E, having an output impedance Z_S connected to an impedance Z_0, and loaded with a resistance R_L.

Until after a reflected pulse returns from the termination of the transmitting device, line termination is not a factor in drive current. In a practical TTL circuit, the line termination must be high relative to the line impedance. For explanation purposes, assume that the source voltage is 5 V in amplitude, the output impedance of the source is 50 Ω and the line impedance is 50 Ω. When the source voltage makes the transition from 0 V to 5 V, the voltage across the input of the line V_I is determined by the following equation:

$$V_I = E\frac{Z_0}{Z_S + Z_0} = 2.5 \text{ V}$$

where E = source voltage
Z_0 = line impedance
Z_S = source impedance

For the 50 Ω line to become charged, the current that must flow onto the line is determined by the following equation:

$$I_{line}\ \frac{V_{in}}{Z_0} = \frac{2.5}{50} = 50 \text{ mA}$$

In addition, this current flows in the ground return, which, in this case, is the transmission-line ground. If the line and return are originated and terminated close to the driving and receiving devices, there is no discontinuity in the line. Where the ground is poorly returned, the current flow sees the discontinuity in the cable as a high impedance and a noise spike is generated (i.e., the ground current sees a low impedance and a current cancellation if the ground is properly carried through and, if not, it sees a high impedance). Figure 34 presents a specific example. Assume that the gate driving the line is switched from the high to low state. Current flow is indicated by the arrow marked with an I. Since the line is improperly returned to the driver, a pulse is developed across the impedance. A possible consequence is the false output of gate 3 (G3).

If the ground return is properly connected, the proper results are obtained. The impedance discontinuity is eliminated and current cancellation occurs at the ground point. Undesirable voltage spikes are then eliminated. Two empirical rules to reduce transmission-line currents have been established and have been found to be effective (Figure 35).

1. Carry all returns, including twisted pair and coaxial cables, to a good ground termination. Ground line returns close to the driving and receiving devices.

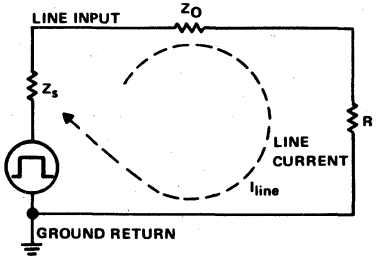


Figure 33. Diagram Representing a Gate Driving a Transmission Line

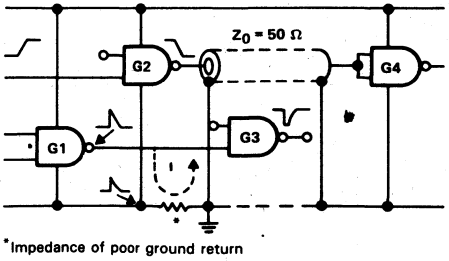


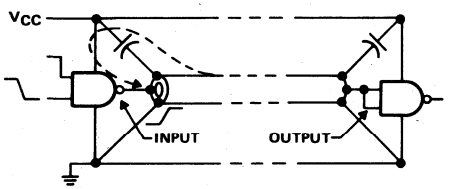
Figure 34. Noise Generation Caused by Poor Transmission-Line Return

2. Decouple the supply voltage of line-driving and line-receiving gates with a 0.1-μF disk ceramic capacitor.

As the devices change state, current levels change because of the different device currents required in each state, the external loading, the transients caused by charging and discharging capacitive loads, and the conduction overlap in the totem-pole output stage. When a gate changes states, its internal supply current changes from high to low (these values are stated on the data sheet for each device). In addition, any capacitance, stray or otherwise, must be charged or discharged for a logic state change. The capacitance must be charged by a current determined by

$$I = C \frac{dv}{dt} \quad (4)$$

If the total stray capacitance on a gate output, the logic-level voltage excursion, and the associated rise or fall times are known, then the ideal-case instantaneous current during the transition can be calculated.

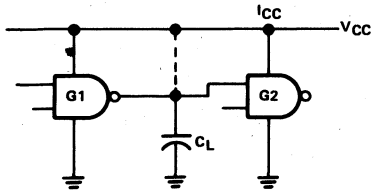


Broken arrow shows path of line-charging current

Figure 35. Ideal Transmission-Line Current Handling

From Eq. (4) it can be determined that the current transient for charging load capacitance will increase with higher speed TTL circuits. Therefore, the Series 54ALS/74ALS devices will have lower transient current than the Series 54AS/74AS devices. Another parameter that should be considered is the value of R7 (shown in Figures 12 and 13). Resistor R7 acts as a limit on the charging current.

The current required for charging load capacitance C_L (Figure 36) is supplied by the supply voltage when the transition is from logic low to logic high at the output of gate 1 (G1). When the output of G1 goes from high to low, the load capacitance is shorted to ground by transistor Q5 (shown in Figures 12 and 13) and has no effect on supply current.



C_L includes all capacitance: stray, device, etc.

Figure 36. Circuit with Effective Capacitive Loading

A characteristic common to all TTL totem-pole output stages contributes an additional current transient when the output changes from a logic low to a logic high. This transient, or spike, is caused by the overlap in conduction of the output transistors Q7 and Q5 (shown in Figures 12 and 13). The situation arises because transistor Q7 can turn on faster than transistor Q5 can turn off. This places a direct circuit consisting of transistors Q7 and Q5 and resistor R4 between supply voltage and ground. For all series 'ALS TTL circuits, the maximum possible peak current can be determined by

$$I_{CC}max = \frac{V_{CC} - V_{CEQ6} - V_{BEQ7} - V_{CEQ5}}{R7}$$

However, due to the active turnoff circuit (consisting of R5, R6, and Q4), Q5 will be only slightly in the linear region and the current spike will be less.

The total supply-current switching transient is then a combination of three major effects: the difference in high-level and low-level supply current, the charging of load capacitance, and the conduction overlap. Tests were performed to demonstrate these effects. The results are shown in Figure 37. Six types of series TTL devices were tested with no load (i.e., the oscilloscope was connected to the output only when measuring V_O and the photographs were double exposed). This was to approximate the effects of conduction overlap isolated from the transient caused by charging load capacitance. Different vertical scales were used on some of the photographs.

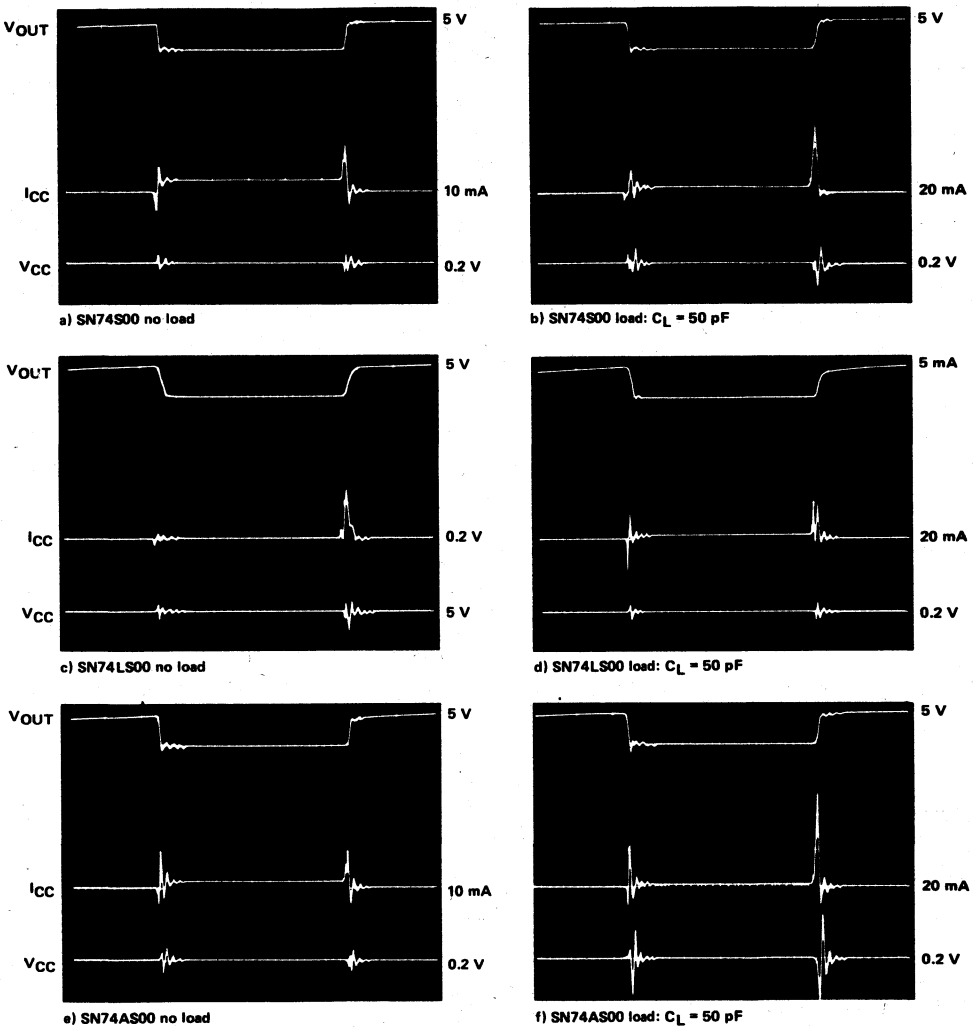
The results are almost as predicted. The low-power devices have the lower transients. Since it is the fastest circuit, the SN74AS00 device should be highest. However, a decrease is shown, and the reason for the decrease is explained (Figure 39). The additional circuits to reduce conduction overlap of the output transistors result in a smaller transient even though the typical switching time is 1.7 ns compared to 9 ns for the Series 54/74LS.

The second series of tests shown in Figure 37 cover a capacitive load of 50 pF. For this test, all of the supply current transient peaks increase in amplitude and width.

Because of the larger transient currents, voltage spikes on the supply voltage measured at the IC package are also increased.

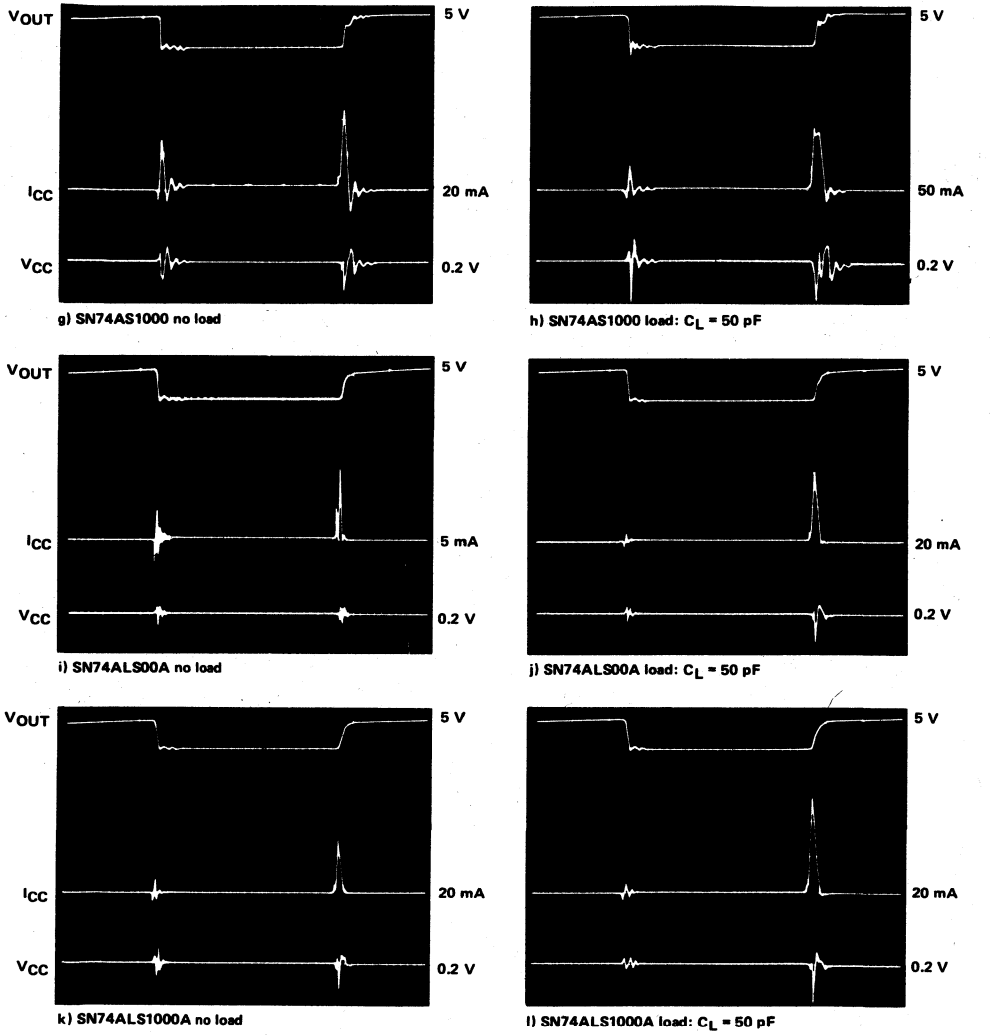
From these tests, it can be concluded that the condition to be avoided (the only one that can be avoided) is unnecessary stray capacitance in circuit wiring. The charging of load capacitance, in most cases, overshadows the other two effects with respect to noise produced on the supply voltage line by switching current transients.

The flow paths of these currents have been investigated to determine the grounding and decoupling necessary to counteract their effects. Supply voltage decoupling may be accomplished by one of two methods. Maintaining low impedance from the individual circuit supply voltage to



NOTES: 1. V_{CC} = 5 V
2. Sweep is 50 ns/division
3. Rise and fall times of input pulse are 1 ns
4. Vertical scales are in units shown per division

Figure 37(a). Supply-Current Transient Comparisons



NOTES: 1. V_{CC} = 5 V
2. Sweep is 50 ns/division
3. Rise and fall times of input pulse are 1 ns
4. Vertical scales are in units shown per division

Figure 37(b). Supply-Current Transient Comparisons

ground is common to both methods. In the first method, the supply voltage line may be considered as a transmission line back to a low impedance supply. The positive bus can be laminated with a ground bus to form a strip transmission line of extremely low impedance. This line can be electrically approximated with lumped capacitances as shown in Figure 38. The inductances are usually a distributed component which must be minimized to lower the line impedance.

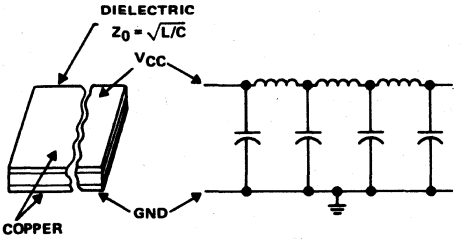


Figure 38. Transmission-Line Power Buses

The second method is to consider the supply voltage bus as a dc connecting element only and to provide a low-impedance path near the devices for the transient currents to be grounded (Figure 39).

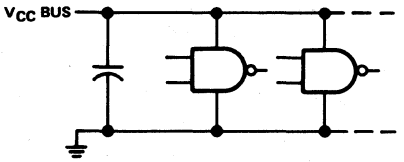


Figure 39. Capacitive Storage Supply Voltage System

For effective filtering and decoupling, the capacitors must be able to supply the change in current for a period of time greater than the pulse width of this current. Since the problem is essentially one of dc changes due to logic state coupled with high-frequency transients associated with the changes, two different values of time constant must be considered. Capacitors combining the high capacitance required for long periods with the low series reactance required for fast transients are prohibitive in cost and size. A good compromise is the arrangement shown in Figure 40.

The typical component values may be found for the RF capacitor C1 by assuming that the parameters have common values as follows:

$\Delta I_{CC} = 50$ mA
$\Delta V = 0.1$ V
$\Delta T = 20$ ns

Then the equation is as follows:

$$C1 = \frac{\Delta I_{CC}}{\Delta V/\Delta T} = \frac{(50)(20) \times 10^{-12}}{0.1/(20 \times 10^{-9})}$$

$$= \frac{50 \times 10^{-3}}{0.1} = 10{,}000 \times 10^{-12}$$

$$= 0.01\ \mu F$$

The same method may be used for the low-frequency capacitor C2. However, the factor ΔT, which was a worst-case transient time for calculating C2, now becomes a bit ambiguous. An analysis of the current cycling on a statistical basis is the best method in all but the simplest systems. The recommended procedure is to decouple using 10 μF to 50 μF capacitors.

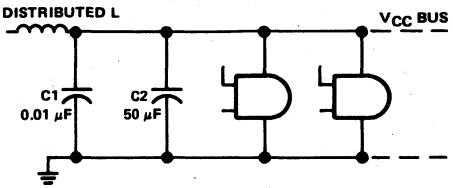


Figure 40. Commonly Used Power Distribution and Decoupling System

A discrete inductance of 2 μH to 10 μH is sometimes used for additional decoupling. However, its benefits are questionable and its usefulness should be evaluated for the individual system. The low-pass filter formed must be capable of keeping the transients confined and off the distribution bus. The possibility of resonance in the inductor or LC combination must be considered.

Noise spikes on the supply voltage line that do not force the gate output below the threshold level do not present a serious problem. Downward spikes as large as 3 V can be tolerated on the supply voltage line without propagating through the logic system. The system designer can be confident that supply voltage noise can be handled even with minimal consideration.

Ground noise, however, cannot be treated lightly. Pulses on a high-impedance ground line can easily exceed the noise threshold. Only if a good ground system is maintained can this problem be overcome. If proper attention is paid to the ground system, noise problems can be minimized.

The concept of a common-ground-plane structure as used in RF and high-speed digital systems is quite different from the concept of the common-ground point as used in low-frequency circuits. The more closely the chassis and ground can approach to being an integral unit, the better the noise suppression characteristics of the system. Consequently, all

parts of the chassis and ground bus system must be bound tightly together both electrically and mechanically. Floating or poorly grounded sections not only break the integrity of the ground system, but may actually act as a noise distribution system.

For grounds and decoupling on printed circuit boards, the most desirable arrangement is a double-clad or multilayer board with a solid ground plane or a mesh. Where component density prohibits this, the ideal should be relaxed only as far as necessary. Cross talk and ground noise can be reduced on large boards with a ground plane. Some suggestions for board grounds where a plane is not practical are as follows:

1. Use as wide a ground strap as possible.
2. Form a complete loop around the board by bringing both sides of the board through separate pins to the system ground.

The supply voltage line can provide part of the ground mesh on the board, provided it is properly decoupled. For a TTL system, a good guideline is 0.01 μF per synchronously driven gate and at least 0.1 μF for each 20 gates, regardless of synchronization. This capacitance may be lumped, but is more effective if distributed over the board. A good rule is to permit no more than 5 inches of wire between any two package supply-voltage points. Radio-frequency-type capacitors must be used for decoupling. Disk ceramics are best. It is sometimes a good practice to decouple the board from the external supply-voltage line with a 2.2 μF capacitor. However, this is optional and the RF capacitors are still required. In addition, it is recommended that gates driving long lines have the supply voltage decoupled at the gate supply voltage terminal and that the capacitor ground, device ground, and transmission-line ground be connected to a common point.

Cross Talk

When currents and voltages are impressed on a connecting line in a system, it is impossible for adjacent lines to remain unaffected. Static and magnetic fields interact and opposing ground currents flow, creating linking magnetic fields. These cross-coupling effects are lumped together and called cross talk.

Back-Panel Interconnections

Interconnecting signal lines can be grouped into three broad categories: coaxial lines, twisted-pair lines, and straight wire lines. Because of the low impedance and shielding characteristics of coaxial cable, its cross talk is minimal and is not a problem with TTL.

Figure 41 illustrates a practical type of signal transmission line. The mutual reactances L_m and C_m which form the noise coupling paths and the line parameters L_s and C_g which govern the line impedance, will vary with the type of line used. Since cross talk is a function of the ratio of the mutual impedances to the line characteristic impedances, the selection of transmission-line type must be at least partially a factor in cross-talk considerations.

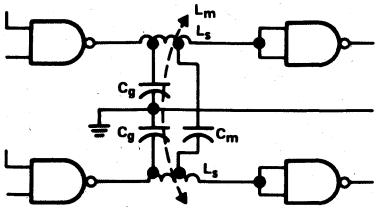


Figure 41. Equivalent Circuit for Sending Line

The use of direct-wired connections is the simplest and lowest cost method, but they are also the poorest for noise rejection. If the lead is not cabled tightly together with similar leads, direct leads up to 12 inches in length can be used.

When the length of the signal line is increased, the line impedance is seen by the driving and receiving gates. As shown in Figure 42, a pulse sent along the sending line G3 and G4 will be coupled via the coupling impedance Z_c onto the receiving line G1 and G2, which can be in either of the two logic states. The extent to which cross talk will occur depends on the type of lines used and their relationship to each other.

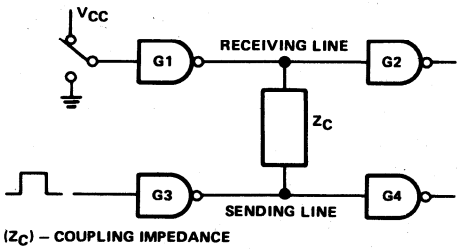


Figure 42. Equivalent Circuit for Cross Talk

The voltage impressed on the sending line by gate G3 is determined by the equation:

$$V_{SL} = \frac{V_{G3}Z_0}{R_{S3} + Z_0} \qquad (5)$$

where

V_{G3} = open-circuit logic voltage swing generated by gate G3
R_{S3} = output impedance of gate G3
Z_0 = line impedance
V_{SL} = voltage impressed on the sending line.

The relationship for the equation is illustrated in Figures 43 and 44.

The coupling from the sending line to the receiving line can be represented by taking coupling impedance Z_c into

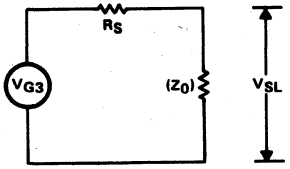


Figure 43. Capacitive Cross Talk Between Two Signal Lines

account. An equivalent circuit to represent the coupling from the sending line to the receiving line is shown in Figure 44.

As the voltage impressed on the sending line propagates farther along the line, it can be represented as voltage source V_{SL} with a source impedance of Z_{01} (Figure 45). V_{SL} is then coupled to the receiving line via the coupling capacitance, where the impedance looking into the line is line impedance in both directions. Therefore the equation becomes

$$V_{RL} = V_{SL} \frac{\frac{Z_0}{2}}{(1.5\ Z_0 + Z_c)}$$

The voltage impressed on the receiving line (V_{RL}) then propagates along the receiving line to gate G2 which can be considered as an open circuit and voltage doubling occurs. Therefore:

$$V_{in(2)} = 2\ V_{RL} = V_{G3}\left(\frac{1}{1.5 + \frac{Z_c}{Z_0}}\right)\left(\frac{Z_0}{RS3 + Z_0}\right)$$

In the switching period, the transistor has a very low output impedance. Then $R_{S3} \ll Z_0$ and $V_{in(2)}$ can be simplified to the following:

$$V_{in(2)} = V_{G3}\left(\frac{1}{1.5 + \frac{Z_c}{Z_0}}\right)$$

The term $V_{in(2)}/V_{G3}$ can be defined as the cross-talk coupling constant.

The worst-case for signal line cross talk occurs when sending and receiving lines are close together but widely separated from a ground return path. The lines then have a high characteristic impedance and a low coupling impedance.

For example, if we assume a coupling impedance of 50 pF at 150 MHz with a line impedance of approximately 200 Ω then:

$$\frac{V_{in(2)}}{V_{G3}} = 0.62$$

This level is unsatisfactory because none of the very high-speed logic circuits has a guaranteed noise margin greater than one-third of the logic swing. Such potential cross talk can be avoided by not using the close spacing of conductors.

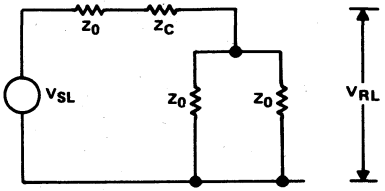


Figure 45. Equivalent Cross-Talk Network

Mutual coupling can be reduced by using coaxial cable or shielded twisted pairs. When mutual inductance and capacitance are decreased, line capacitance is increased and imposes restrictions on the driver. Coaxial cable combines very high mutual impedance with low characteristic impedance and shielding. It effectively eliminates cross talk, but is necessary in only the noisiest environments. Twisted pairs are adequate for most applications and are typically less expensive and easier to use.

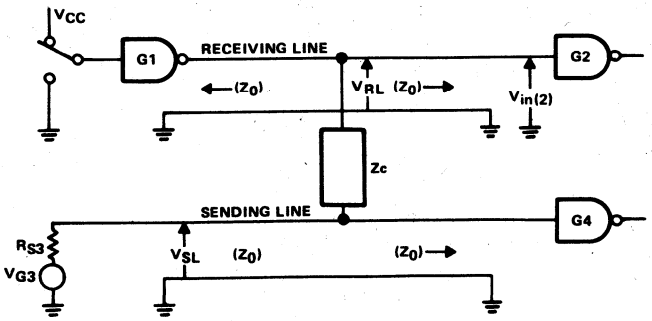


Figure 44. Coupling Impedances Involved in Cross Talk

Printed Circuit Card Conductors

Signal interconnections on a two-sided or multilayer printed circuit card can be grouped into two general categories: microstrip lines and strip lines. The microstrip line (Figure 46) consists of a signal conductor separated from a ground plane by a dielectric insulating material. A strip line (Figure 47) consists of a signal conductor within a dielectric insulating material and the conductor being centered between two parallel conductor planes. The important features of these type of printed circuit conductors are that the impedances are highly predictable, can be closely controlled, and the process is relatively inexpensive because standard printed circuit board manufacturing techniques are used. Typical impedances of these types of conductors with respect to their physical size and relative spacings are shown in Tables 7 and 8.

Table 7. Typical Impedance of Microstrip Lines

Dimensions		Line Impedance	Capacitance
H (mils)	W (mils)	Z_O (Ω)	per Foot (pF)
6	20	35	40
6	15	40	35
15	20	56	30
15	15	66	26
30	20	80	20
30	15	89	18
60	20	105	16
60	15	114	14
100	20	124	13
100	15	132	12

Relative dielectric constant ≈ 5

Table 8. Typical Impedance of Strip Lines

Dimensions		Line Impedance	Capacitance
H'a = H'b = (mils)	W (mils)	Z_O (Ω)	per Foot (pF)
6	20	27	80
6	15	32	70
10	20	34	67
10	15	40	56
12	20	37	57
12	15	43	48
20	20	44	48
20	15	51	42
30	20	55	39
30	15	61	35

Relative dielectric constant ≈ 5, and H'a = H'b

Cross talk on a printed circuit board is also a function of the mutual reactances and the line parameters which govern the line impedance. A microstrip line and a strip line are, by definition, conductors placed relatively close to a ground plane. Therefore, they have at least one inherent property which tends to reduce cross talk. In addition, the thickness (H) of the dielectric and the spacing (S) of the conductors can be implemented selectively to reduce the amount of possible cross talk. The effects of these two dimensions on cross talk have been evaluated and are shown graphically in Figure 48. The data shown can be used to estimate the maximum crosstalk which will be encountered under the most unfavorable conditions.

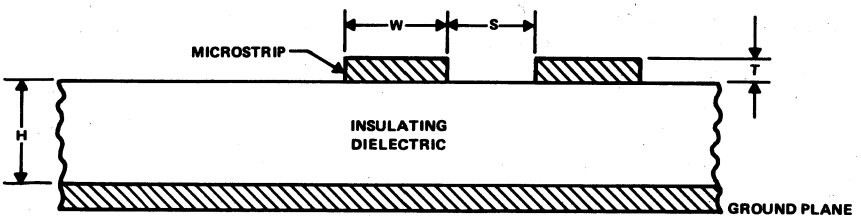


Figure 46. Microstrip Line

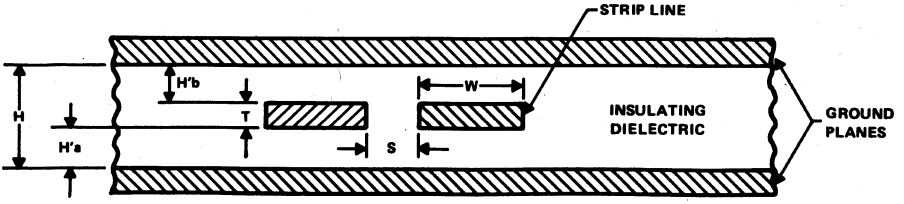


Figure 47. Strip Line

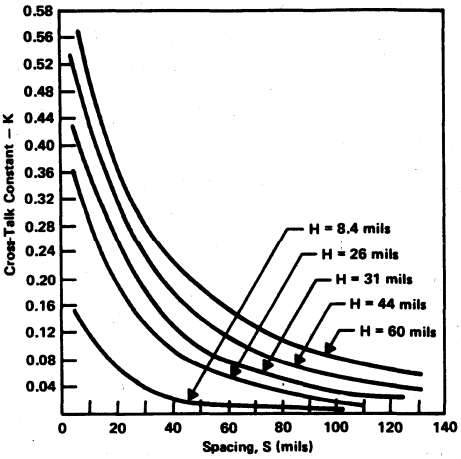


Figure 48. Line Spacing Versus Cross-Talk Constant

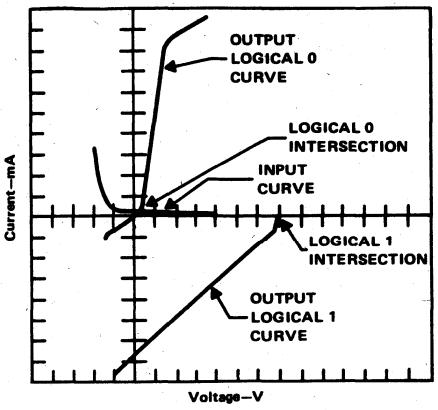


Figure 49. TTL Bergeron Diagram

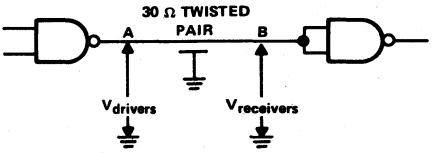


Figure 50. 'ALS/'AS Driving Twisted Pair

Transmission-Line Driving Reflections

When the interconnections used to transfer digital information become long enough so that line propagation delay is equal to or greater than the pulse transition times, the effects of reflections must be considered. These reflections are created because most TTL interconnections are not terminated in their characteristic impedance. Reflections lead to reduced noise margins, excessive delays, ringing, and overshoot. Some method must be used to analyze these reflections. Because neither the gate input nor output impedance is linear, basic transmission-line equations are applicable but unwieldy. Transmission-line characteristics of TTL interconnections can be analyzed by using a simple graphic technique.

Figure 49 shows piecewise linear plots of a gate input and both (logic-high and logic-low) states of the output for a typical TTL device. The output curves are plotted with positive slopes. The input is inverted because it is at the receiving end of a transmission line. The logic-high and logic-low intersections are indicated on the plot. These points are the steady-state values which will be observed on a lossless transmission line (Figure 50).

Figure 50 shows a typical TTL interconnection using a twisted-pair cable which, in this example, has a characteristic impedance of approximately 30 Ω. To evaluate a logic-high to logic-low 'AS transition see Figures 51 and 52. The equation $-1/Z_0$ (Z_0 = 30 Ω), which represents the transmission line, is superimposed on the output characteristic curves in the Bergeron plot. Since evaluation of a logic-high to logic-low transition is desired, the $-1/Z_0$ line starts at the point of intersection of the impedance curves of the input and output for a logic-high state. The slope $-1/Z_0$ then proceeds toward the logic-low output curve. At time t_0, the driver output voltage is determined by the intersection of $-1/Z_0$ and the logic-low output curve (1.2 V). The transmission-line slope now becomes $1/Z_0$ and is drawn toward the input curve. At time t_1 [$t_{(n+1)} - t_n$ = time delay of line], the receiving gate sees −0.7 V. Now the line slope changes back to $-1/Z_0$ and the output curve for a logic low is approached. This action continues until the logic-low intersection is reached. Figure 52 plots driver and receiver voltages versus time for this example.

A logic-low to logic-high transition is treated in approximately the same manner (Figure 53). The Bergeron line $-1/Z_0$ starts at the intersection for a logic low. At time t_0, the driver output rises to 2.2 V and, at time t_1, the receiving gate input goes to approximately 4.35 V. Both output and input voltages are plotted in Figure 54.

Figures 55 through 58 illustrate 'ALS transitions and are treated in the same manner as the 'AS.

The scope photographs in Figures 59 through 66 show the effectiveness of the graphic techniques. In most cases, the calculated and experimental values of voltage steps agree within reason. The ringing that appears for the open wire is not immediately obvious. This is because the input and output curves in this region lie practically along the positive horizontal axis. At the scale used for graphic analysis, it is difficult to go much beyond the first few reflections. The graphic analysis is idealized and stray capacitance and inductance are not considered.

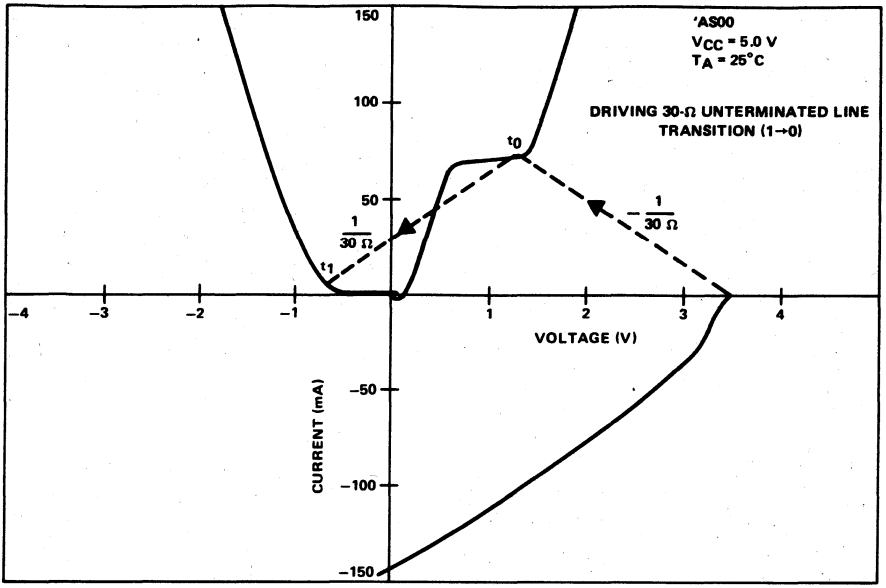


Figure 51. 'AS −ve Transition Bergeron Diagram

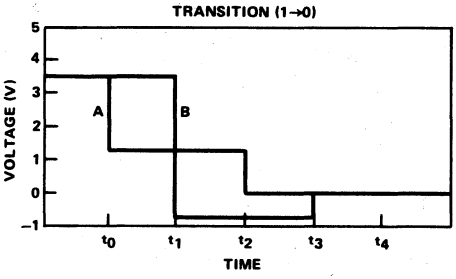


Figure 52. 'AS −ve Voltage/Time Plot

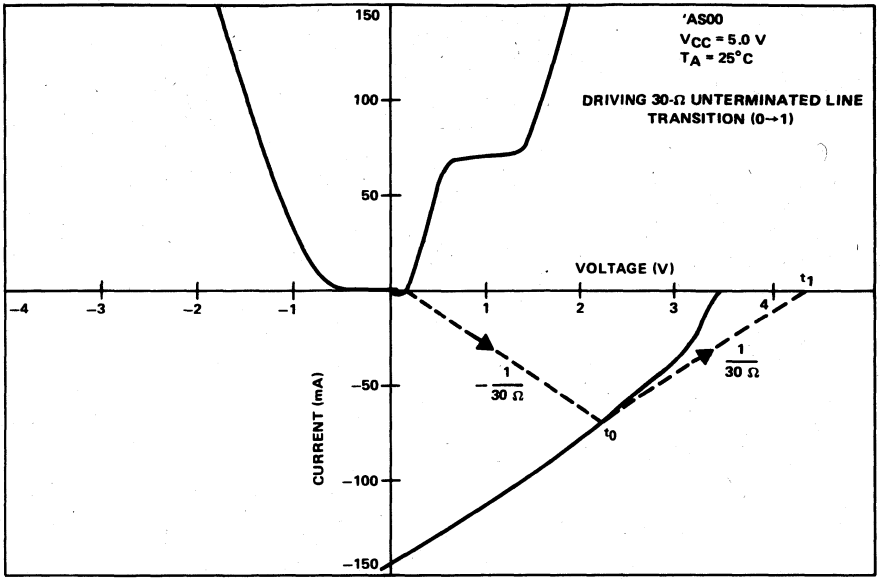


Figure 53. 'AS +ve Transition Bergeron Diagram

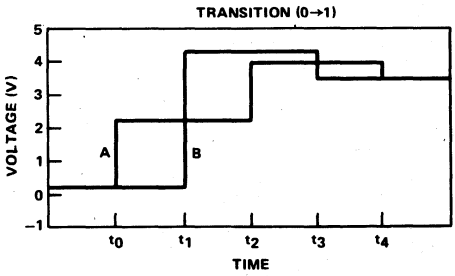


Figure 54. 'AS +ve Voltage/Time Plot

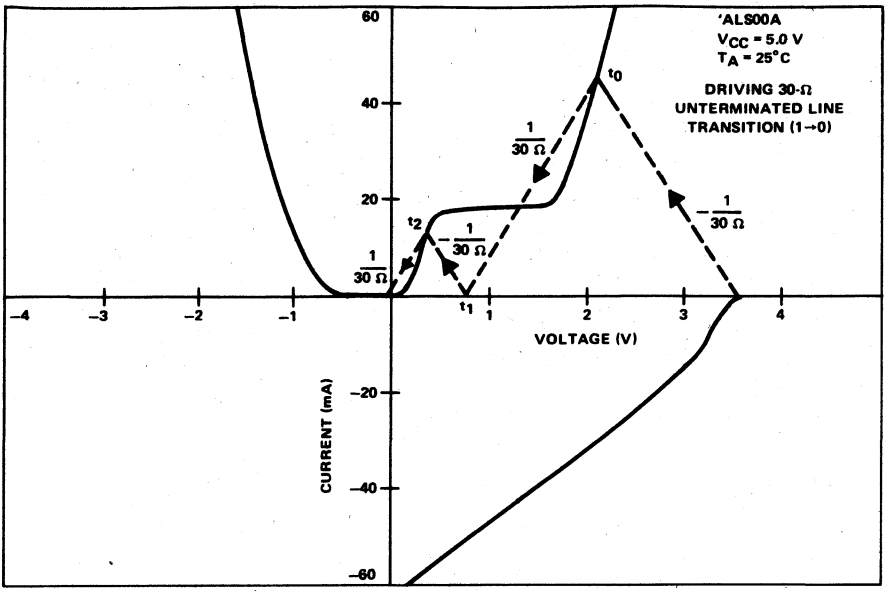


Figure 55. 'ALS −ve Transition Bergeron Diagram

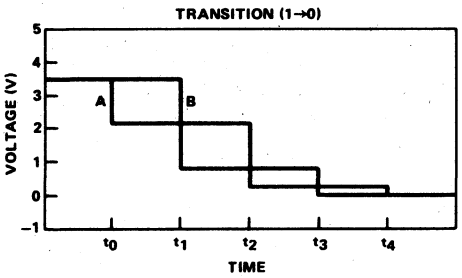


Figure 56. 'ALS −ve Voltage/Time Plot

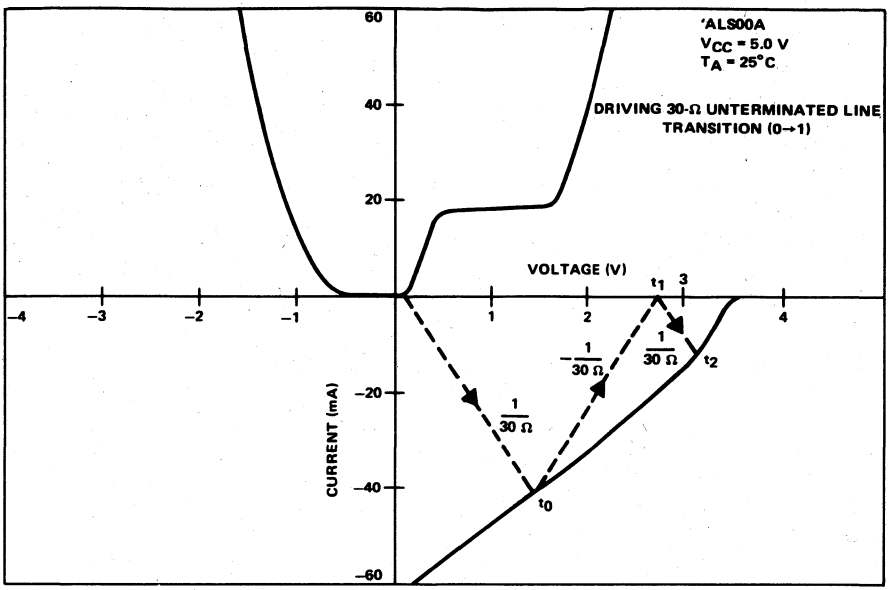


Figure 57. 'ALS +ve Transition Bergeron Diagram

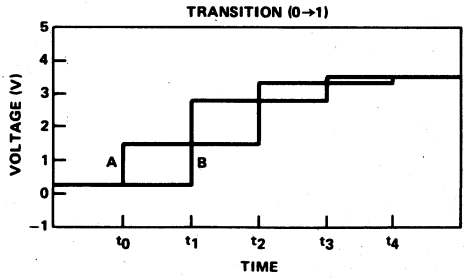


Figure 58. 'ALS +ve Voltage/Time Plot

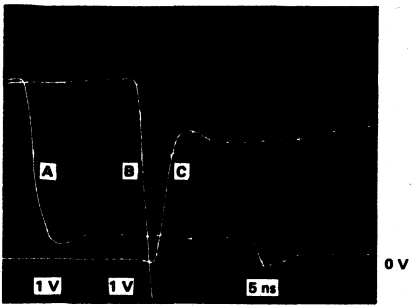


Figure 59. Oscilloscope Photograph of 'AS001 −ve Transition Using 50-Ohm Line

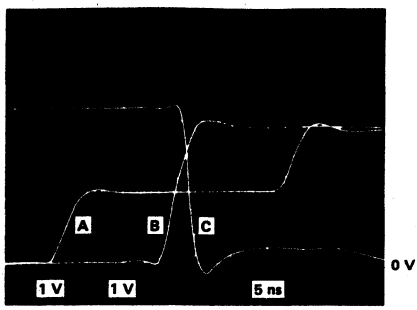


Figure 62. Oscilloscope Photograph of 'AS00 +ve Transition Using 25-Ohm Line

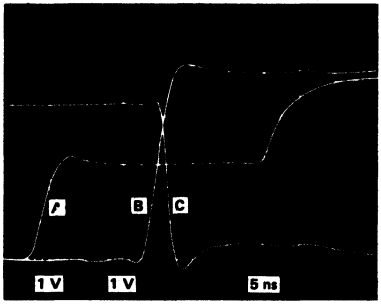


Figure 60. Oscilloscope Photograph of 'AS00 +ve Transition Using 50-Ohm Line

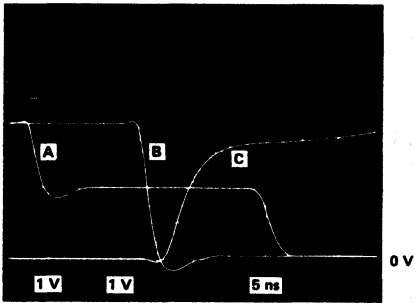


Figure 63. Oscilloscope Photograph of 'ALS00A −ve Transition Using 50-Ohm Line

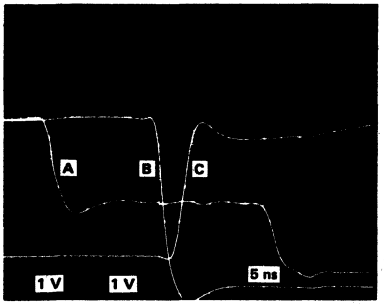


Figure 61. Oscilloscope Photograph of 'AS00 −ve Transition Using 25-Ohm Line

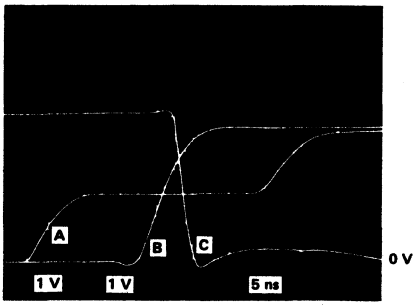


Figure 64. Oscilloscope Photograph of 'ALS00A +ve Transition Using 50-Ohm Line

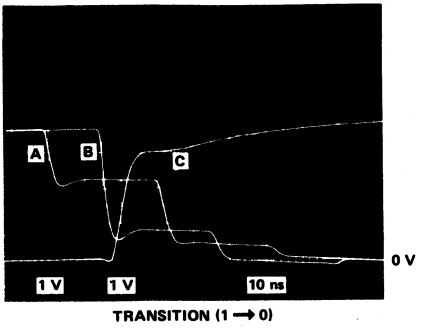


Figure 65. Oscilloscope Photograph of 'ALS00A −ve Transition Using 25-Ohm Line

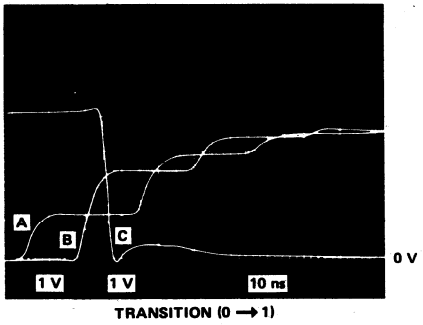


Figure 66. Oscilloscope Photograph of 'ALS00A +ve Transition Using 25-Ohm Line

References

1. W.C. Elmore and M. Sands, *Electronics Experimental Techniques*, McGraw-Hill Book Co., New York, 30ff. (1949).
2. M. Williams and S. Miller, *Series 54ALS/74ALS Schottky TTL Applications B215*, Texas Instruments Limited, Bedford, England, August 1982.

Acknowledgment

This application report is an updated version of Reference 2 with significant contributions by the technical engineering staff at Texas Instruments and particularly by Rock Cozad, Rich Moore, and Bob Strong.

Appendix A
Normalized Load Factors

Normalizing output drive capability and input current requirements can be very useful to designers of systems using two or more of the TI TTL series of devices. It provides a set of load factors (input cuurent requirements in Table A-1), which can be summed and compared directly to the fanout capability (see Table A-2) of the output being considered. The load factor values shown are valid for any input rated at one unit load.

The loading of these type of outputs can be checked from any column. However, most designs use one of the series as the basic building block and, since the tables cover each series individually, the designer has the choice of working from the column containing the normalized fanout. As an example, the designers of a system using series 'AS as the basic circuit will probably find that the use of the 'AS00 and 'AS1000 columns will suit best because both fanout and load factors are expressed for these series of devices.

The use of these simple and easy-to-remember numbers was developed within each series to make the verification of output loading a matter of counting the number of inputs connected to a particular output. When mixtures of series are used, a common denominator (normalized factor) becomes useful.

USE OF TABLES A-1 AND A-2

Every possible combination of the seven 54/74 TTL families is included in these tables. If, for example, the existing system used 74S series logic and it is desired that some of it be replaced by series 74ALS logic, a quick check should be made on whether the 'ALS can be supplied with sufficient input current. By taking the 74S row and 'ALS, column figures of 2.5 and 20 are obtained for high- and low-level loads, respectively (see Table A-1). This indicates that, for high logic levels, two and one-half 'ALS gates can be driven for each 'S series gate removed. However, if more 74S series gates are being driven by this 'ALS device, the fanout between 'ALS and 'S series gate is required, you can now use Table A-2.

The 'ALS row and the 'S column are chosen. The figures are 8 for the high-logic level and 4 for the low-logic level. In this case the lowest figure is taken so that the interconnection is reliable for both logic states. So each 'ALS gate inserted will drive 4 'S series gates.

Table A-1. Normalized Input Currents

SERIES	I/O	INPUT CURRENT (mA)	INPUT CURRENT NORMALIZED								
			'00	'H00	'L00	'LS00	'S00	'AS00	'ALS00A	'AS1000	'ALS1000A
54/7400	HI	0.04	1	0.8	4	2	0.8	2	2	2	2
54/7400	LO	1.6	1	0.8	8.89	4	0.8	3.2	16	3.2	16
54H/74H00	HI	0.05	1.25	1	5	2.5	1	2.5	2.5	2.5	2.5
54H/74H00	LO	2	1.25	1	11.11	5	1	4	20	4	20
54/74L00	HI	0.01	0.25	0.2	1	0.5	0.2	0.5	0.5	0.5	0.5
54/74L00	LO	0.18	0.11	0.09	1	0.45	0.09	0.36	1.8	0.36	1.8
54LS/74LS00	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54LS/74LS00	LO	0.4	0.25	0.2	2.22	1	0.2	0.8	4	0.8	4
54S/74S00	HI	0.05	1.25	1	5	2.5	1	2.5	2.5	2.5	2.5
54S/74S00	LO	2	1.25	1	11.11	5	1	4	20	4	20
54AS/74AS00	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54AS/74AS00	LO	0.5	0.31	0.25	2.78	1.25	0.25	1	5	1	5
54ALS/74ALS00A	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54ALS/74ALS00A	LO	0.1	0.06	0.05	0.56	0.25	0.05	0.2	1	0.2	1
54AS1000	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54AS1000	LO	0.5	0.31	0.25	2.78	1.25	0.25	1	5	1	5
54ALS1000A	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54ALS1000A	LO	0.1	0.06	0.05	0.56	0.25	0.05	0.2	1	0.2	1

Table A-1 is normally used (in combination with Table A-2) when replacing one logic family with another in an existing system.

Table A-2 is normally used when originally designing a system which employs several TTL families to optimize performance.

Table A-2. Fanout Capability (Output Currents Normalized to Input Currents)

SERIES	I/O	OUTPUT CURRENT (mA)	OUTPUT DRIVE NORMALIZED								
			'00	'H00	'L00	'LS00	'S00	'AS00	'ALS00A	'AS1000	'ALS1000A
			*HI 0.04	0.05	0.01	0.02	0.05	0.02	0.02	0.02	0.02
			†LO 1.6	2	0.18	0.4	2	0.5	0.1	0.5	0.1
54/7400	HI	0.4	10	8	40	20	8	20	20	20	20
54/7400	LO	16	10	8	88.89	40	8	32	160	32	160
54H/74H00	HI	0.5	12.5	10	50	25	10	25	25	25	25
54H/74H00	LO	20	12.5	10	111.11	50	10	40	200	40	200
54L00	HI	0.1	2.5	2	10	5	2	5	5	5	5
54L00	LO	2	1.25	1	11.11	5	1	4	20	4	20
74L00	HI	0.2	5	4	20	10	4	10	10	10	10
74L00	LO	3.6	2.25	1.8	20	9	1.8	7.2	36	7.2	36
54LS/74LS00	HI	0.4	10	8	40	20	8	20	20	20	20
54LS00	LO	4	2.5	2	22.22	10	2	8	40	8	40
74LS00	LO	8	5	4	44.44	20	4	16	80	16	80
54S/74S00	HI	1	25	20	100	50	20	50	50	50	50
54S/74S00	LO	20	12.5	10	111.11	50	10	40	200	40	200
54AS/74AS00	HI	2	50	40	200	100	40	100	100	100	100
54AS/74AS00	LO	20	12.5	10	111.11	50	10	40	200	40	200
54ALS/74ALS00A	HI	0.4	10	8	40	20	8	20	20	20	20
54ALS00A	LO	4	2.5	2	22.22	10	2	8	40	8	40
74ALS00A	LO	8	5	4	44.44	20	4	16	80	16	80
54AS1000	HI	40	1000	800	4000	2000	800	2000	2000	2000	2000
54AS1000	LO	40	25	20	222.22	100	20	80	400	80	400
74AS1000	HI	48	1200	960	4800	2400	960	2400	2400	2400	2400
74AS1000	LO	48	30	24	266.67	120	24	96	480	96	480
54ALS1000A	HI	1	25	20	100	50	20	50	50	50	50
54ALS1000A	LO	12	7.5	6	66.67	30	6	24	120	24	120
74ALS1000A	HI	2	65	52	260	130	52	130	130	130	130
74ALS1000A	LO	24	15	12	133.33	60	12	48	240	48	240

*Input Current HI

†Input Curent LO

Appendix B

Letter Symbols, Terms, and Definitions

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronics Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use. The definitions are grouped into sections applying to voltages, currents, switching characteristics, and classification of circuit complexity.

VOLTAGES

V_{IH} High-level input voltage
An input voltage level within the more positive (less negative) of the two ranges of values used to represent the binary variables. A minimum value is specified which is the least-positive (most-negative) value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} Low-level input voltage
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. A maximum value is specified which is the most-positive (least-negative) value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{T+} Positive-going threshold voltage
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

V_{T-} Negative-going threshold voltage
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

V_{OH} High-level output voltage
The voltage at an output terminal for a specified output current I_{OH} with input conditions applied that according to the product specification will establish a high level at the output.

V_{OL} Low-level output voltage
The voltage at an output terminal for a specified output current I_{OL} with input conditions applied that according to the product specification will establish a low level at the output.

$V_{O(on)}$ On-state output voltage
The voltage at an output terminal for a specified output current with input conditions applied that according to the product specification will cause the output switching element to be in the on state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

$V_{O(off)}$ Off-state output voltage
The voltage at an output terminal for a specified output current with input conditions applied that according to the specification will cause the output switching element to be in the off state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

CURRENT

I_{IH} High-level input current
The current flowing into* an input when a specified high-level voltage is applied to that input.

I_{IL} Low-level input current
The current flowing into* an input when a specified low-level voltage is applied to that input.

*Current flowing out of a terminal is a negative value.

I_{OH} **High-level output current**
The current flowing into* the output with a specified high-level output voltage V_{OH} applied.

Note: This parameter is usually specified for open-collector outputs intended to drive other logic circuits.

$I_{O(off)}$ **Off-state output current**
The current flowing into* an output with a specified output voltage applied and input conditions applied that according to the product specification will cause the output switching element to be in the off state.

Note: This parameter is usually specified for open-collector outputs intended to drive devices other than logic circuits or for three-state outputs.

I_{OS} **Short-circuit output current**
The current flowing into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{CCH} **Supply current, output(s) high**
The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a high-level voltage.

I_{CCL} **Supply current, output(s) low**
The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a low-level voltage.

DYNAMIC CHARACTERISTICS

f_{max} **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause a change of output state with each clock pulse.

t_{HZ} **Output disable time (of a three-state output) from high level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{LZ} **Output disable time (of a three-state output) from low level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PHL} **Propagation delay time, high-to-low-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{TLH} **Transition time, low-to-high-level output**
The time between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level.

t_{THL} **Transition time, high-to-low-level output**
The time between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level.

t_w **Average pulse width**
The time between 50% amplitude points (or other specified reference points) on the leading and trailing edges of a pulse.

*Current flowing out of a terminal is a negative value.

t_h **Hold time**
The time interval for which a signal or pulse is retained at a specified input terminal after an active transition occurs at another specified input terminal.

$t_{release}$ **Release time**
The time interval between the release from a specified input terminal of data intended to be recognized and the occurrence of an active transition at another specified input terminal.

Note: When specified, the interval designated "release time" falls within the setup interval and constitutes, in effect, a negative hold time.

t_{su} **Setup time**
The time interval for which a signal is applied and maintained at a specified input terminal before an active transition occurs at another specified input terminal.

t_{ZH} **Output enable time (of a three-state output) to high level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{ZL} **Output enable time (of a three-state output) to low level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

CLASSIFICATION OF CIRCUIT COMPLEXITY

Gate equivalent circuit
A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

LSI **Large-scale integration**
A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether logical or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

MSI **Medium-scale integration**
A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

SSI **Small-scale integration**
Integrated circuits of less complexity than medium-scale integration (MSI).

*Current flowing out of a terminal is a negative value.

Metastable Characteristics of Texas Instruments Advanced Bipolar Logic Families

Robert K. Breuninger and Kevin Frank

TEXAS INSTRUMENTS

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INTRODUCTION

At some point in every system designers career, they are faced with the problem of synchronizing two digital signals operating at two different frequencies. This problem is typically solved by synchronizing one of the signals, to the local clock, through a flip-flop. However, this solution presents an awkward dilemma, the setup and hold time specifications associated with the flip-flop are sure to be violated. The metastable characteristics of the flip-flop used can influence overall system reliability. The purpose of this application report is to give the system designer a better understanding of the metastable characteristics pertaining to Texas Instruments Advanced Schottky Bipolar Logic Family.

METASTABLE DEFINITION

Whenever a flip-flops setup and hold time is violated, the flip-flops output response is uncertain. Presently, there is no circuit that can 100% guarantee its response. This is why the device manufacturer does not guarantee its operation. Specifically, the metastable state is defined as that time period when the output of a digital logic device, is not at a logic level 1 (V_{out} less than 2 V) or a logic level 0 (V_{out} greater than 0.8 V), but instead between 0.8 V and 2 V. Since the input data is changing at the time of being clocked, the system designer does not care if the flip-flop goes to either a high or low logic level, just so long as the output does not hang up in the metastable region. The metastable characteristics for a particular flip-flop will determine how long the device stays in the metastable region. This concept is illustrated in the timing diagram of Figure 1.

METASTABLE EVALUATION

Anyone who has tried to evaluate the metastable characteristics for a particular flip-flop, has probably found it is not an easy task. The number of times the output hangs up in the metastable region is extremely small when compared to total number of clock transitions. In addition, the amount of time the output is actually in the metastable region is a variable and dependent on the type of flip-flop used (LS, ALS, AS, etc.).

From the design engineers viewpoint, when using a flip-flop as a data synchronizer, they can no longer use the specified data sheet maximum for propagation delay. Instead, to guarantee reliable system operation, they need to know how long after the specified data sheet maximum they need to wait before using the data. Conventional test equipment is not designed to measure these parameters, so a special test circuit is required for characterizing MTBF (Mean Time Between Failures) and Δt (time between CLK and Q valid). With these two parameters specified, the system designer can make a rational decision about what type of flip-flop to use, and how long to wait before using the data.

Circuit Description

The circuit in Figure 2 can be used in evaluating MTBF and Δt for a selected flip-flop (DUT, Device Under Test). Two 'AS04s are used to detect whenever the Q output of the DUT is in the metastable region. This is accomplished by adjusting the input threshold to 2 V on one inverter and 0.8 V on the other. Notice that input thresholds are adjusted by referencing the ground input pins to 0.6 V and −0.6 V respectively. Therefore, whenever the Q output of the DUT

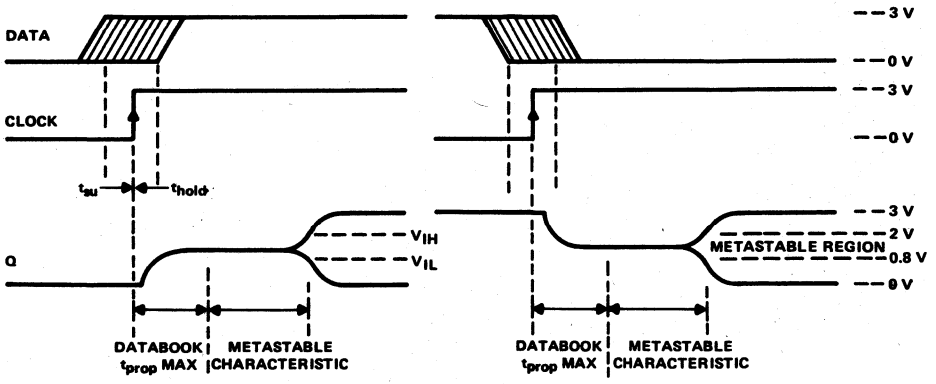


Figure 1. Metastable Timing Diagram

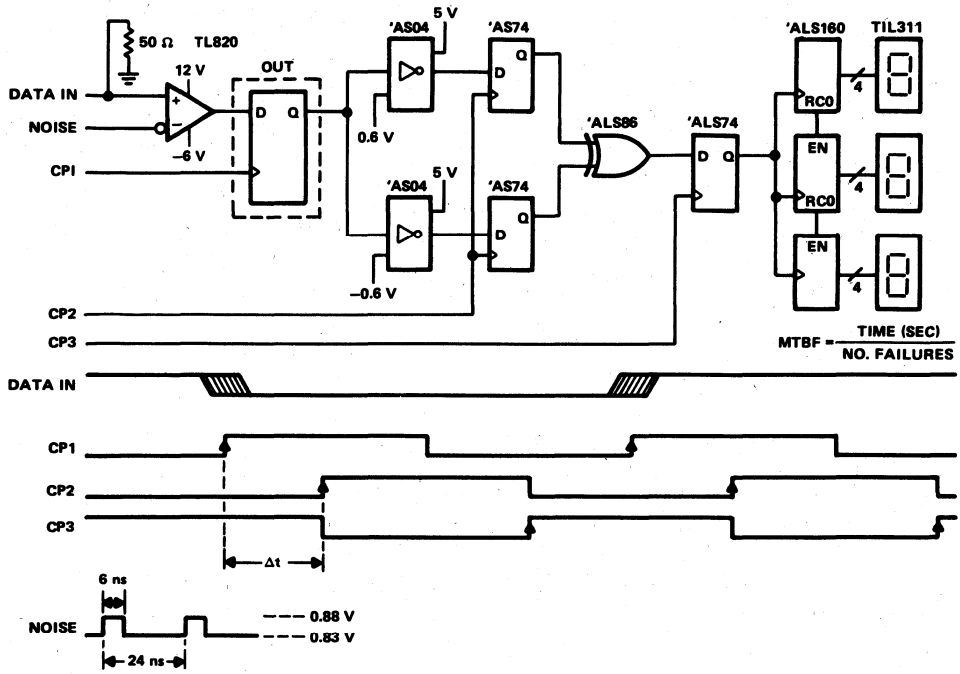


Figure 2. Metastable Evaluation Test Circuit

is between 0.8 V and 2 V, the inverters will be in opposite states. Whenever the Q output of the DUT is higher than 2 V or lower than 0.8 V, both inverters will be at the same logic level. The outputs of the 'AS04s are then clocked (CP2) into two 'AS74s a selected time (Δt) after the DUT clock (CP1). The outputs of the 'AS74s are compared through an 'ALS86 and clocked (CP3) into another 'ALS74. This guarantees against any false clocking by the evaluation circuit. The output of the 'ALS74 is then feed to a series of three 'ALS160 counters, and on into three TIL311s for counter display.

In order to maximize the possibility of forcing the DUT into a metastable state, the input data signal must jitter around the threshold of the input clock. The width of the jitter should equal, or exceed the setup and hold time specification for the device. In our evaluation circuit, this is accomplished by feeding a low level noise signal into the negative input of a TIL820 operational amplifier. The pictures shown in Figure 3 show the noise generated around the DUT clock (CP1) for both input data transitions.

It should be intuitively obvious that the worst-case condition, for any specified input data frequency, will be when the input data **always violates the data setup and hold times**. This condition is shown in the timing diagram of Figure 2. Any other relationship of CP1 to DATA IN, would provide less chance for the device to enter the metastable state. Therefore, it can be concluded that the worst-case condition for a given input data frequency, will be 0.5 times the DUT clock rate where the input data always violates the setup and hold time.

By using the described circuit, MTBF can be determined for several different values of Δt. Plotting this information on semilog paper reveals the metastable characteristics, for the selected flip-flop, at the desired input data frequency.

Test Circuit Limitations

Before we proceed to the AS/ALS test results, it is important to analyze the limitations of our test circuit. In this way, we can better understand its effects on the test results. Two major areas which can greatly affect the test results are not centering the jitter around the input clock, and propagation delay of the 'AS04s. By not centering the jitter around the input clock, the risk of entering the metastable state is reduced. Proper care must be taken to ensure that the jitter is always centered around the input clock to guarantee worst-case conditions.

The propagation delay of the 'AS04s affect the test results because they add propagation delay between the output of the DUT, and the data being clocked into the 'AS74s. For

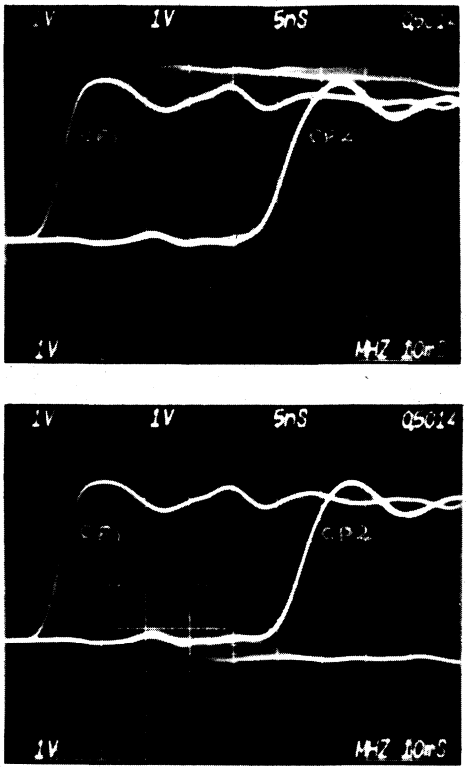


Figure 3. Test Waveforms

example, the output on the DUT may come out of the metastable region, but the 'AS04s may not switch before CP2 occurs. This causes an inappropriate reading. The typical propagation delay of the 'AS04s, **as configured in the test circuit**, is approximately 4 ns. This 4 ns delay should be considered when evaluating the test results. If inverters slower than the 'AS04s are used in the test circuit, a larger offset must be considered.

ALS/AS Test Results

Using the test circuit described in Figure 2, 'ALS74s, 'ALS273s and 'ALS374s were evaluated at several different Δt time periods. The input clock frequency used was 1 MHZ with an input data frequency of 500 kHz. The devices were allowed to run until an appropriate amount of errors were recorded. The number of errors were then divided by the total time the devices were allowed to run. This results in a MTBF for the selected Δt. The information was then recorded on semilog paper for analysis. It was found that all three device types exibited basically the same metastable characteristics within + 3 ns of each other. This was expected since all three device types come from the same technology. The same experiment was performed using AS and LS devices. The average characteristics for all three device families are shown in Figure 4. The 4-ns offset generated by the test circuit has not been subtracted from the data.

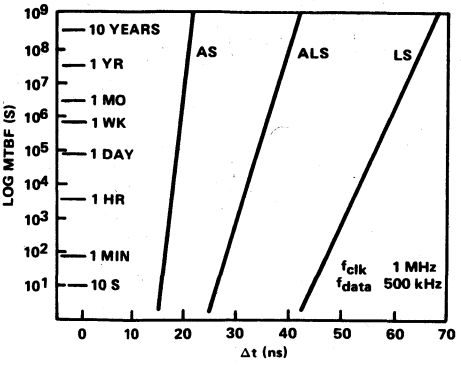


Figure 4. AS/ALS/LS Metastable Characteristics

Other Clock Frequencies

Clock frequencies other than 1 MHz will either increase or decrease the probability of the device entering the metastable state. The faster the frequency, the higher the probability of entering the metastable state. Likewise, the slower the frequency, the lower the probability of entering the metastable state. From the data taken in the above experiment, an equation can be derived for the metastable characteristics at other clock frequencies. Equation (1) relates input clock and data frequency, to metastable characteristics.

Metastable Equation

$$\frac{1}{\text{MTBF}} = f_{cp} \times f_{data} \times C1\, e^{(-C2\,\Delta t)} \qquad (1)$$

As stated earlier, the worst case situation for the test circuit shown in Figure 2, is when the data setup and hold time is always violated. Based on this assumption, the equation is reduced to the following.

$$\frac{1}{\text{MTBF}} = \frac{1}{2} f_{cp}^2 \times C1\, e^{(-C2\,\Delta t)} \qquad (2)$$

The constants C1 and C2 describe the metastable characteristics of the device. From the experimental data graphed in Figure 4, these constants can be solved for each device family. As an example, the constants are solved below for the ALS device family.

C2 is defined by the slope of the line. Picking two data points off the graph yields the following.

$$C2 = \frac{10^8 - 10^2}{40.2 - 28.2}(2.302) = \frac{6}{12}(2.302) = 1.151$$

By plugging C2 into equation 2, along with using one of the data points off the graph, C1 can be solved for.

$$\frac{1}{MTBF} = \frac{1}{2} f_{cp}^2 \times C1\, e^{(-1.51\,\Delta t)}$$

$$\frac{1}{10^8} = \frac{1}{2} (10^6)^2 \times C1\, e^{(-1.151 \times 40.2)}$$

$$C1 = 2.49$$

Inserting C1 and C2 into equation 2, yields the metastable equation for ALS.

$$\frac{1}{MTBF} = \frac{1}{2} f_{cp}^2 \times 2.49\, e^{(-1.151\,\Delta t)}$$

Given this worst-case equation, the system designer can determine the metastable characteristics for ALS when using other input clock frequencies.

The equations for AS and LS can be derived using the same procedure. They are as follows.

AS:

$$\frac{1}{MTBF} = \frac{1}{2} f_{cp}^2 \times 1.53 \times 10^7\, e^{(-2.92\,\Delta t)}$$

LS:

$$\frac{1}{MTBF} = \frac{1}{2} f_{cp}^2 \times 306\, e^{-0.783\,\Delta t)}$$

To get a feel for the effect of changing the input clock frequency, Figure 5 shows the change in the metastable characteristics from 1 MHz to 10 MHz.

METASTABLE CHARACTERISTICS OF PROGRAMMABLE LOGIC

The PAL16R4A and TIBPAL16R4-15 from the programmable logic family were also evaluated. They exhibited very similar characteristics to the ALS curve. This was expected because they utilize the same technology. One important consideration when evaluating programmable logic in the test circuit described, is positioning the jittery data a few nanoseconds before CP1. This compensates for the delay of the AND/OR array which is usually positioned in front of the flip-flop. Remember that the jittery data must be violating the setup and hold time at the input to the flip-flop, not just at the device input. Some experimentation is usually required to find the worst-case condition.

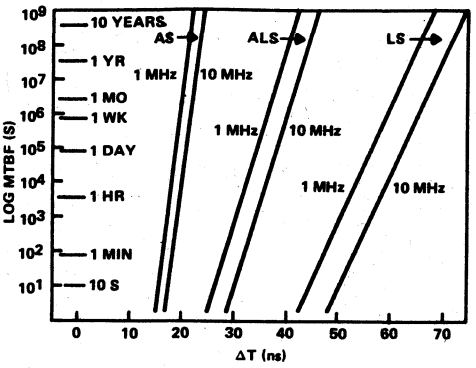


Figure 5. AS/ALS/LS Metastable Characteristics Variation with Frequency

As a general rule, a system designer can usually get a feel for the metastable characteristics of a device by simply looking at the setup and hold time specifications. Usually, the smaller the setup and hold time numbers, the better its metastable characteristics will be. However, in the case of programmable logic, the setup and hold time numbers are not reflective of metastable characteristics. This is because the setup and hold time numbers also reflect the propagation delay time of the AND/OR logic in front of the flip-flops.

SUMMARY

The metastable characteristics of a flip-flop used for data synchronization can greatly affect system reliability. Based on the information presented in this application report, the system designer can make a rational decision about what type of flip-flop to use, and what its metastable characteristics will be.

It is easy to see from the experimental data shown in Figure 4, that AS offers the best metastable characteristics. It has a much narrower setup and hold time window, and is quicker to recover once it gets into the metastable region. However, with adequate sampling time, ALS and LS will also perform well. The selection of what type of flip-flop to use must be based on the speed of the application. As a general rule, the faster the flip-flop, the better its metastable characteristics.

We at Texas Instruments believe that the graphs shown and equations derived, represent a reasonable assumption about the metastable characteristics for the device families discussed. However, we strongly recommend that when using flip-flops as data synchronizers, an adequate amount of guardband is allowed between the characteristics shown, and when the output of the flip-flop is actually sampled.

1

2

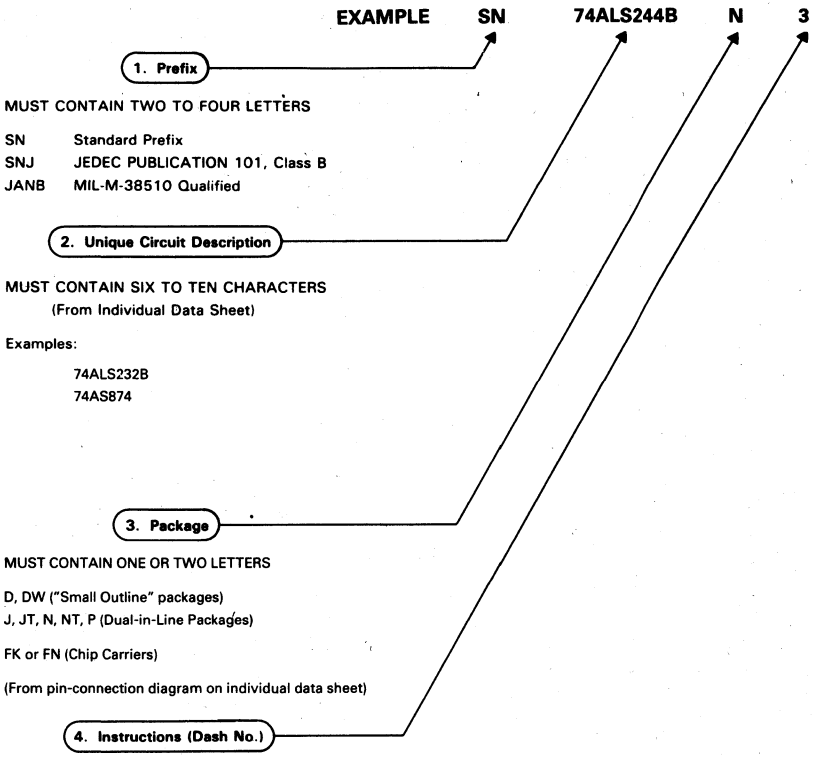
3

Mechanical Data 4

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.



†These circuits in dual-in-line and "small outline" packages are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier. Please contact your TI sales representative for the method that will best suit your particular needs.

"Small Outline" (D, DW)
Dual-in-Line (J, JT, N, NT, P)

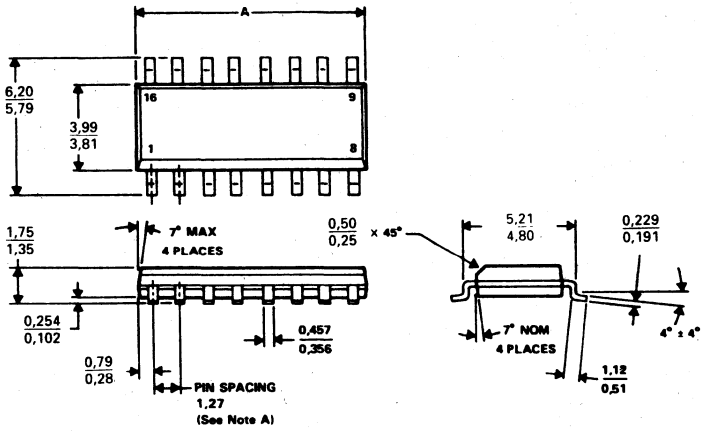
— A-Channel Plastic Tubing

— Tape and Reel

D plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D PLASTIC PACKAGE
(16-pin package used for illustration)



DIM \ PINS	8	14	16
A MIN	4,80	8,56	9,80
A MAX	5,00	8,74	10,00

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS

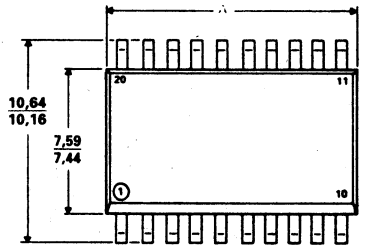
NOTES: A. Leads are within 0,25 mm radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 mm.
D. Lead tips to be planar within ± 0,051 mm exclusive of solder.

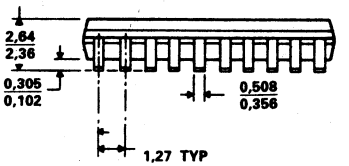
DW016, DW020, DW024 and DW028
plastic small-outline packages

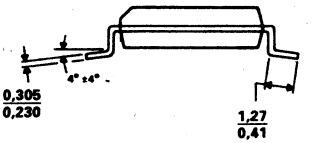
Each of these small-outline packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DW016, DW020, DW024 and DW028
(20-pin package used for illustration)

Designation per JEDEC Std 30:
R-PDSO-G16
R-PDSO-G20
R-PDSO-G24
R-PDSO-G28







DIM \ PINS	16	20	24	28
A MAX	10,41	12,95	15,49	18,03
A MIN	10,16	12,70	15,24	17,78

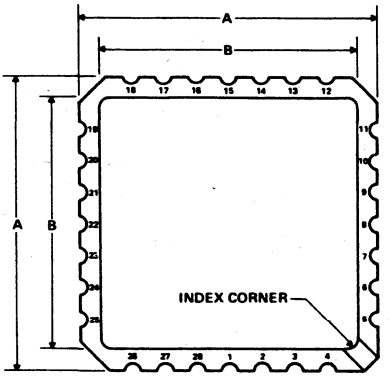
NOTES: A. All linear-dimensions are in millimeters.
B. Leads are within 0,127 radius of true position at maximum material conditions.
C. Lead tips are coplanar within 0,102.
D. Body dimensions do not include mold flash or protrusion.
E. Mold protrusion shall not exceed 0,15.
F. Interlead flash controlled by TI Statistical Process Control (additional information available through local TI sales office).

FK ceramic chip carrier packages

Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers. terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC Standards 1 and 2.

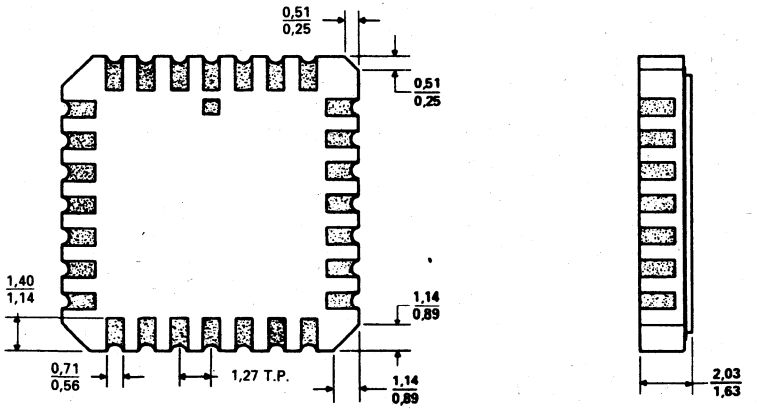
FK CERAMIC CHIP CARRIER PACKAGES
(28-terminal package shown)



CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX
MS004CB	20	8,69	9.09	7,80	9,09
MS004CC	28	11,23	11,63	10,31	11,63

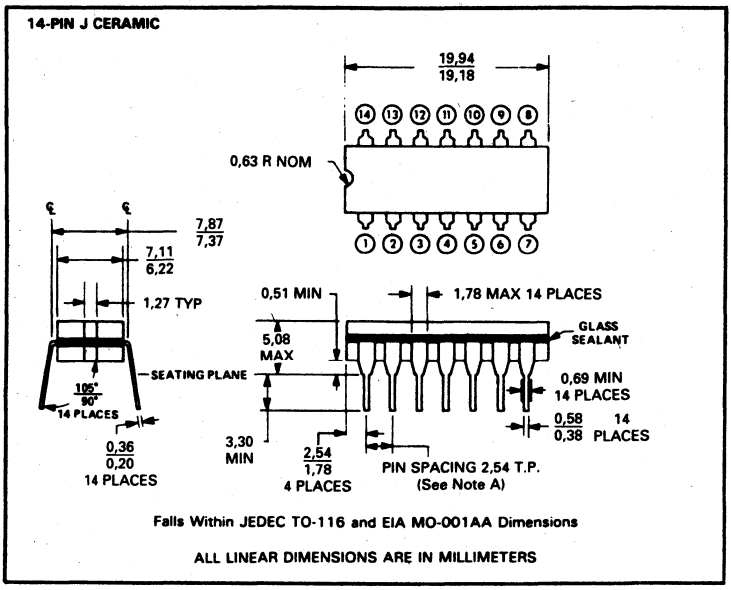
*All dimensions and notes for the specified JEDEC outline apply.



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS

J ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

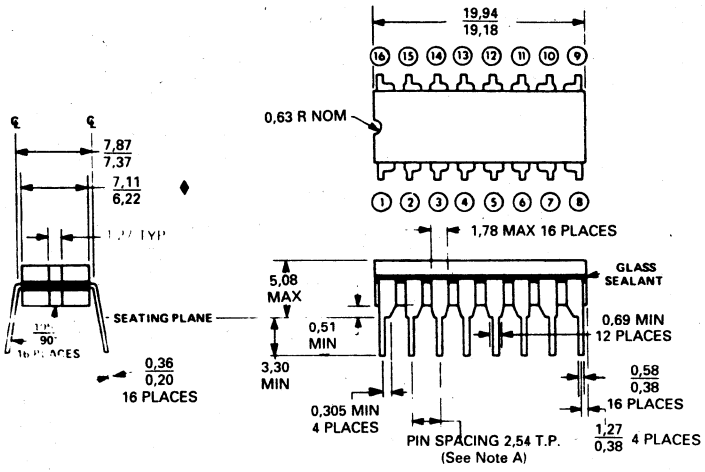


NOTE A: Each pin centerline is located within 0,25 of its true longitudinal position.

J ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

16-PIN J CERAMIC



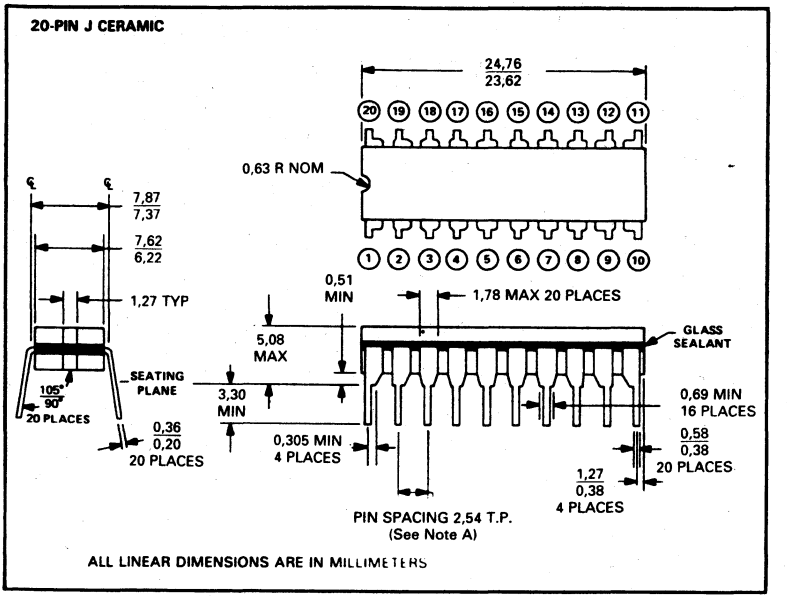
♦ For memories of 64 bits and up, a few MSI/LSI products in Series 54/74 and Series 54/74 and Series 54S/74S that are derived from memory circuit bars and complex HCMOS parts, this maximum is 7.62. All other dimensions apply without modification.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS

NOTE A: Each pin centerline is located within 0,25 of its true longitudinal position.

J ceramic dual-in-line package

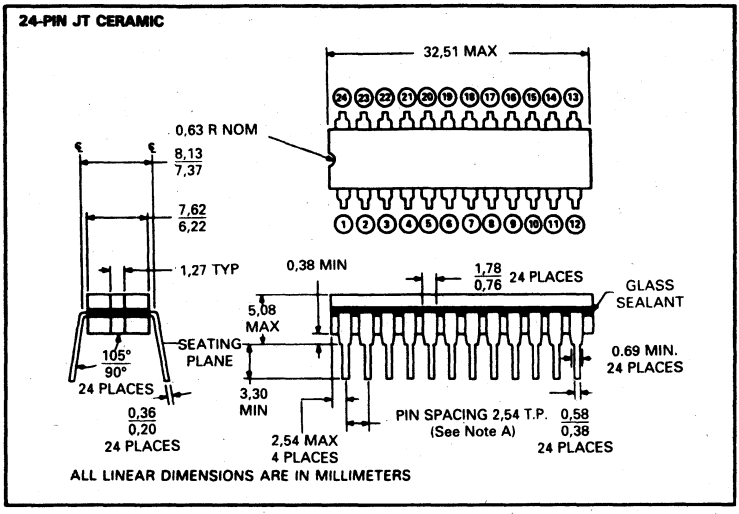
This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.



NOTE A: Each pin centerline is located within 0,25 of its true longitudinal position.

JT024 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.



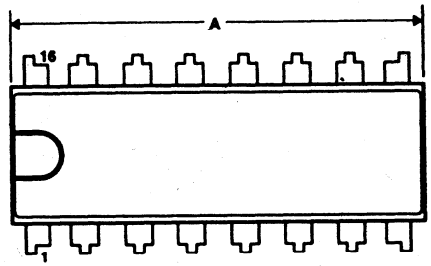
NOTE A: Each pin centerline is located within 0,25 of its true longitudinal position.

N014, N016 and N020
300-mil plastic dual-in-line packages

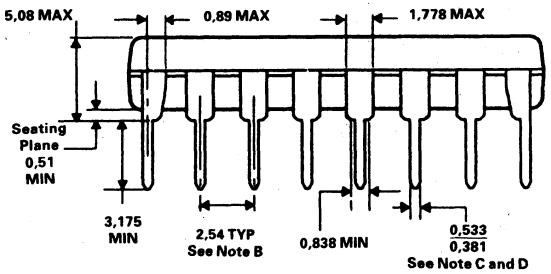
These dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 7,62 centers (see Note B). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

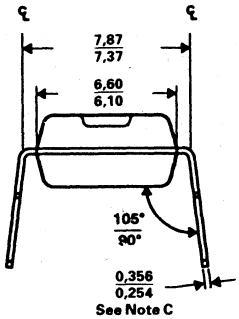
N014, N016 and N020
(16-pin package used for illustration)

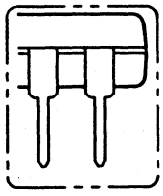
Designation per JEDEC Std 30:
R-PDIP-T14
R-PDIP-T16
R-PDIP-T20



DIM \ PINS	14	16	18
A MAX	19,69	19,69	24,77
A MIN	18,92	18,92	23,88







End Pin Detail – 14 Pin

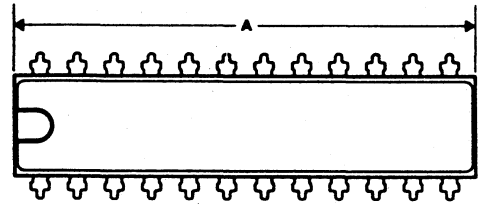
NOTES: A. All linear dimensions are in millimeters.
B. Each pin centerline is located within 0,254 of its true longitudinal position.
C. This dimensions does not apply for solder-dipped leads.
D. When solder dip is specified, dipped area of the lead extends from the lead tip to at least 0,51 above seating plane.

NT024 and NT028
600-mil plastic dual-in-line packages

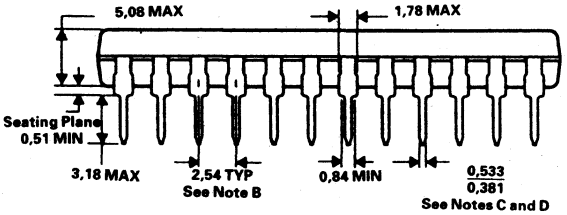
These dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 7,62 centers (see Note B). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

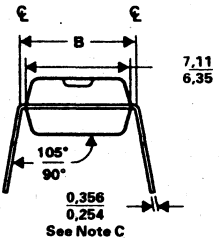
NT024 and NT028
(24-pin package used for illustration)

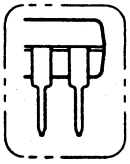
Designation per JEDEC Std 30:
R-PDIP-T24
R-PDIP-T28



DIM \ PINS	24	28
A MAX	32,04	36,20
A MIN	31,24	35,18
B MAX	7,87	8,00
B MIN	7,37	7,49







Alternate Standoff Design

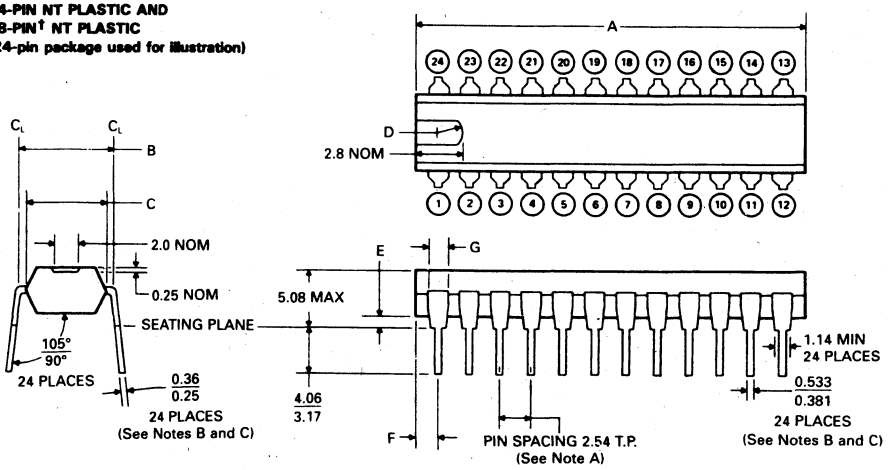
NOTES: A. All linear dimensions are in millimeters.
B. Each pin centerline is located within 0,254 of its true longitudinal position.
C. This dimension does not apply for solder-dipped leads.
D. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 above seating plane.

NT plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7.62 version is designated NT; the 15.24 version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15.24 row-spacing.

24-PIN NT PLASTIC AND
28-PIN† NT PLASTIC
(24-pin package used for illustration)



DIM / DESIGNATION	A MIN	A MAX	B	C MAX	D R NOM	E MIN	F MIN	F MAX	G MIN	G MAX
NT024	28.6	31.8	7.62 ± 0.25	7.1	2.4	0.38	0.71	2.16	1.14	1.78
NT028†	34.0	37.1	7.88 ± 0.25	6.86	1.02	0.51	0.51	2.03	1.02	1.78

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS

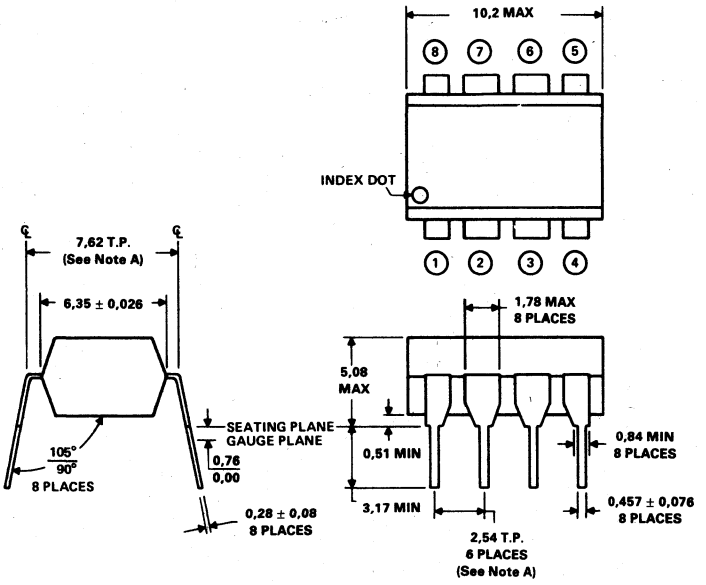
† The 28-pin package drawing is presently classified as Advance Information.

NOTES: A. Each pin centerline is located within 0.25 mm of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0.51 mm above seating plane.

P dual-in-line plastic package

This dual-in-line package consists of a circuit mounted on an 8-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62-mm centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Solder-plated leads require no additional cleaning or processing when used in solder assembly.

8-PIN P PLASTIC



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS

NOTE: A. Each pin is within 0,13 radius of true position (TP) at the gauge plane with maximum material condition and unit installed.

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